1981 CATALOG

NEC Electronics (Europe) GmbH

NEC



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NEW IN THE 1981 CATALOG: NEC MICROCOMPUTERS BOARD PRODUCTS

SEE SECTION 10.

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MEMORIES 2

MEMORY SELECTION GUIDE

DEVICE	SIZE	PROCESS	ACCESS TIME	CYCLE	SUPPLY VOLTAGE	PACKAGE MATERIAL	PACKAGE PINS
DYNAMIC RANDOM ACCESS MEMORIES							
μPD411	4K x 1 TS	NMOS	150 ns	380 ns	+12, +5, -5	D	22
μPD411-4	4K x 1 TS	NMOS	135 ns	320 ns	+15, +5, -5	D	22
μPD411A	4K x 1 TS	NMOS	200 ns	400 ns	+12, +5, -5	C	22
μPD416	16K x 1 TS	NMOS	120 ns	320 ns	+12, +5, -5	C/D	16
μPD2118	16K x 1 TS	NMOS	100 ns	235 ns	+5	C/D	16
μPD4164	64K x 1 TS	NMOS	150 ns	270 ns	+5	C/D	16
STATIC RANDOM ACCESS MEMORIES							
μPD5101L	256 x 4 TS	CMOS	450 ns	450 ns	+5	C	22
μPD444/6514	1K x 4 TS	CMOS	200 ns	200 ns	+5	C	18
μPD445L	1K x 4 TS	CMOS	450 ns	450 ns	+5	C	20
μPD446	2K x 8 TS	CMOS	120 ns	120 ns	+5	C/D	24
μPD447	2K x 8 TS	CMOS	120 ns	120 ns	+5	C/D	24
μPD4104	4K x 1 TS	NMOS	200 ns	310 ns	+5	C/D	18
μPD2114L	1K x 4 TS	NMOS	150 ns	150 ns	+5	C/D	18
μPD2147	4K x 1 TS	NMOS	45 ns	45 ns	+5	D	18
μPD2149	1K x 4 TS	NMOS	35 ns	35 ns	+5	D	18
μPD421	1K x 8 TS	NMOS	150 ns	150 ns	+5	D	22
μPD2167	16K x 1 TS	NMOS	55 ns	55 ns	+5	D	20
MASK PROGRAMMED READ ONLY MEMORIES							
μPD2308A	1K x 8 TS	NMOS	450 ns	450 ns	+5	C/D	24
μPD2316E	2K x 8 TS	NMOS	450 ns	450 ns	+5	C	24
μPD2316E-1	2K x 8 TS	NMOS	350 ns	350 ns	+5	C	24
μPD2332A/B	4K x 8 TS	NMOS	450 ns	450 ns	+5	C	24
μPD2332A/B-1	4K x 8 TS	NMOS	350 ns	350 ns	+5	C	24
μPD2364	8K x 8 TS	NMOS	450 ns	450 ns	+5	C	24
μPD23128	16K x 8 TS	NMOS	250 ns	250 ns	+5	C	28
FIELD PROGRAMMABLE READ ONLY MEMORIES							
(Bipolar)							
μPB406	1K x 4 OC	BIPOLAR	50 ns	50 ns	+5	C/D	18
μPB426	1K x 4 TS	BIPOLAR	50 ns	50 ns	+5	C/D	18
μPB409	2K x 8 OC	BIPOLAR	50 ns	50 ns	+5	C/D	24
μPB429	2K x 8 TS	BIPOLAR	50 ns	50 ns	+5	C/D	24
(Bipolar Logic Array)							
μPB450	9216 bit	BIPOLAR	200 ns	200 ns	+5	D	48
(U.V. Erasable)							
μPD2716	2K x 8 TS	NMOS	450 ns	450 ns	+5	D	24
μPD2732	4K x 8 TS	NMOS	450 ns	450 ns	+5	D	24

Notes: O.C. = Open Collector
C – Plastic Package
D – Hermetic Package
TS – 3-State

MEMORY ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
AMD	2716	2K x 8 EPROM	μPD2716
	27S33	1K x 4 PROM	μPB426
	8308	1K x 8 ROM	μPD2308A
	9016	16K x 1 DRAM	μPD416
	9060	4K x 1 DRAM	μPD411/411A
	9107	4K x 1 DRAM	μPD411/411A
	9114	1K x 4 SRAM	μPD2114L
	9124	1K x 4 SRAM	μPD2114L
	9147	4K x 1 SRAM	μPD2147
	9216	2K x 8 ROM	μPD2316E
	AM91L14	1K x 4 SRAM	μPD444/μPD6514
	AM91L24	1K x 4 SRAM	μPD444/μPD6514
EM & M	2114	1K x 4 SRAM	μPD2114L
	8108	1K x 8 SRAM	μPD421
FAIRCHILD	93453	1K x 4 PROM	μPB426
	93511	2K x 8 PROM	μPB429
	F2114	1K x 4 SRAM	μPD2114L
	F2716	2K x 8 EPROM	μPD2716
	F16K	16K x 1 DRAM	μPD416
FUJITSU	7122	1K x 4 PROM	μPB426
	7138	2K x 8 PROM	μPB429
	MBM2147	4K x 1 SRAM	μPD2147
	MBM2716	2K x 8 EPROM	μPD2716
	MBM2732	4K x 8 EPROM	μPD2732
	MB8107	4K x 1 DRAM	μPD411/μPD411A
	MB8114	1K x 4 SRAM	μPD2114L
	MB8116	16K x 1 DRAM	μPD416
	MB8216	16K x 1 DRAM	μPD416
	MB8264	64K x 1 DRAM	μPD4164
	MB8308	1K x 1 ROM	μPD2308A
	MB8414	1K x 4 SRAM	μPD444/6514
HARRIS	7643	1K x 4 PROM	μPB426
	76161	2K x 8 PROM	μPB429
	HM6501	256 x 4 SRAM	μPD5101L
	HM6514	1K x 4 SRAM	μPD444/6514
HITACHI	HM4334	1K x 4 SRAM	μPD444/6514
	HM435101	256 x 4 SRAM	μPD5101L
	HN462716	2K x 8 EPROM	μPD2716
	HN462732	4K x 8 EPROM	μPD2732
	HM472114	1K x 4 SRAM	μPD2114
	HM4716A	16K x 1 DRAM	μPD416
	HM4816	16K x 1 DRAM	μPD2118
	HM4864	16K x 1 DRAM	μPD4164
	HM4864	64K x 1 DRAM	μPD4164
	HM6116	2K x 8 SRAM	μPD446

MEMORY ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
HITACHI (CONT.)	HM6147	4K x 1 SRAM	μPD2147
	HM6148	1K x 4 SRAM	μPD444/6514
INTEL	2107	4K x 1 DRAM	μPD411/μPD411A
	2114	1K x 4 SRAM	μPD2114L
	2117	16K x 1 DRAM	μPD416
	2118	16K x 1 DRAM	μPD2118
	2141	4K x 1 SRAM	μPD4104
	2147	4K x 1 SRAM	μPD2147
	2164	64K x 1 DRAM	μPD4164
	2167	16K x 1 SRAM	μPD2167
	2308A	1K x 8 ROM	μPD2308A
	2316E	2K x 8 ROM	μPD2316E
	2332	4K x 8 ROM	μPD2332A/B
	2364	8K x 8 ROM	μPD2364
	2716	2K x 8 EPROM	μPD2716
	2732	4K x 8 EPROM	μPD2732
	3625	1K x 4 PROM	μPB426
	3636-1	2K x 8 PROM	μPB429
	5101	256 x 4 SRAM	μPD5101L
MITSUBISHI	M5K4164S	64K x 1 DRAM	μPD4164
MMI	63S1681	2K x 8 PROM	μPB429
	63S441	1K x 4 PROM	μPB426
	6353	1K x 4 PROM	μPB426
MOTOROLA	MCM2732	2K x 8 EPROM	μPD2732
	MCM4516/4517	16K x 1 DRAM	μPD2118
	MCM6665	64K x 1 DRAM	μPD4164
	7643	1K x 4 PROM	μPB426
NATIONAL	MM2732	2K x 8 EPROM	μPD2732
	NMC4164	64K x 1 DRAM	μPD4164
	NMC5295	16K x 1 DRAM	μPD2118
	74S573	1K x 4 PROM	μPB426
OKI	MSM5114	1K x 4 SRAM	μPD444/6514
RAYTHEON	29681	2K x 8 PROM	μPB429
SIGNETICS	82S137	1K x 4 PROM	μPB426
	82S191	2K x 8 PROM	μPB429
T.I.	TMS4164	64K x 1 DRAM	μPD4164
	TMS4516	16K x 1 DRAM	μPD2118
	TBP24S41	1K x 4 PROM	μPB426
	TBP28S166	2K x 8 PROM	μPB429
	74S476	1K x 4 PROM	μPB426
TOSHIBA	TMM4164	64K x 1 DRAM	μPD4164
	TC5516P	2K x 8 SRAM	μPD447

NEC

μPD411
μPD411-1
μPD411-2
μPD411-3
μPD411-4

FULLY DECODED RANDOM ACCESS MEMORY

3

DESCRIPTION

The μPD411 Family consists of six 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The μPD411 Family is designed using dynamic circuitry which reduces the standby power dissipation.

Reading information from the memory is a non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

FEATURES

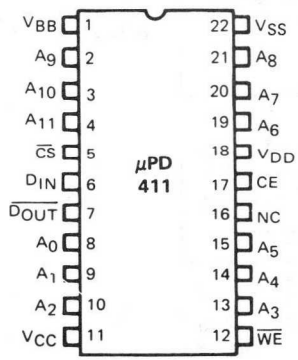
All of these products are guaranteed for operation over the 0 to 70°C temperature range.

Important features of the μPD411 family are:

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power/0.3 mW (Typ.)
- Power Supply: +12, +5, -5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Ceramic Dual-in-Line Package
- Replacement for INTEL'S 2107B, TI'S 4060 and Equivalent Devices.
- 5 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
μPD411	300 ns	470 ns	650 ns	2 ms
μPD411-1	250 ns	470 ns	640 ns	2 ms
μPD411-2	200 ns	400 ns	520 ns	2 ms
μPD411-3	150 ns	380 ns	470 ns	2 ms
μPD411-4	135 ns	320 ns	320 ns	2 ms

PIN CONFIGURATION



PIN NAMES

$A_0 - A_{11}$	Address Inputs
$A_0 - A_5$	Refresh Addresses
$\overline{CE}$	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	Power
NC	No Connection

FUNCTIONAL DESCRIPTION

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{CS}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{WE}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The $\overline{WE}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A_0–A_{11} Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

$\overline{D_{OUT}}$ Data Output

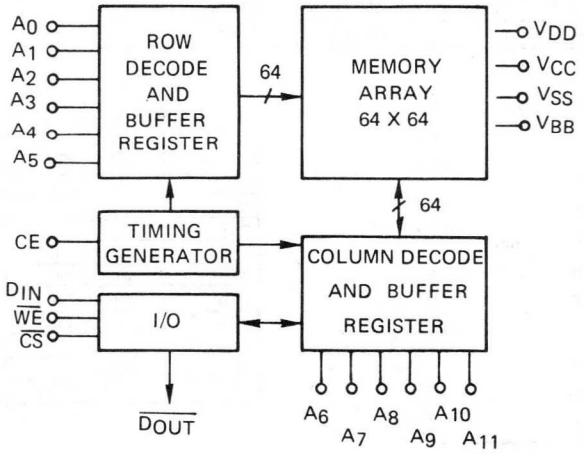
The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A_0 through A_5 or by addressing every row within any 2-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

	μPD411 FAMILY (EXCEPT 411-4)	μPD411-4
Operating Temperature	0°C to +70°C	+10°C to +55°C
Storage Temperature	−55°C to +150°C	−55°C to +150°C
All Output Voltages	−0.3 to +20 Volts	−0.3 to +25 Volts ①
All Input Voltages	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Supply Voltage V_{DD}	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Supply Voltage V_{CC}	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Power Dissipation	1.0W	1.5W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

3

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V,
Except V_{DD} = +15V ±5% for 4114.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}		0.01	10	μA	V_{IN} = V_{IL} MIN to V_{IH} MAX
CE Input Load Current	I_{LC}		0.01	10	μA	V_{IN} = V_{ILC} MIN to V_{IHC} MAX
Output Leakage Current for High Impedance State	I_{LO}		0.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DD} OFF		20	200	μA	CE = 1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DD} ON		35 ⑤	60 ④	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current						T_a = 25°C
μPD411	I_{DD} AV		37	60	mA	Cycle Time = 470 ns
μPD411-1	I_{DD} AV		37	60	mA	Cycle Time = 470 ns
μPD411-2	I_{DD} AV		37	60	mA	Cycle Time = 400 ns
μPD411-3	I_{DD} AV		41	65	mA	Cycle Time = 380 ns
μPD411-4	I_{DD} AV		55	80	mA	Cycle Time = 320 ns
V_{BB} Supply Current ②	I_{BB}		5	100	μA	
V_{CC} Supply Current during CE off ③	I_{CC} OFF		0.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	1.0		0.6	V	
Input High Voltage	V_{IH}	2.4		V_{CC}+1	V	
CE Input Low Voltage	V_{ILC}	1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD}−1	V_{DD}	V_{DD}+1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = 2.0 mA

Notes: ① Typical values are for T_a = 25°C and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage current.
③ During CE on V_{CC} supply current is dependent on output loading.
V_{CC} is connected to output buffer only.
④ 65 mA for μPD411-3
80 mA for μPD411-4
⑤ 41 mA for μPD411-3
55 mA for μPD411-4

CAPACITANCE

T_a = 0° − 70°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Capacitance, $\overline{CS}$	C_{AD}		4	6	pF	V_{IN} = V_{SS}
CE Capacitance	C_{CE}		18	27	pF	V_{IN} = V_{SS}
Data Output Capacitance	C_{OUT}		5	7	pF	V_{OUT} = 0V
D_{IN} and $\overline{WE}$ Capacitance	C_{IN}		8	10	pF	V_{IN} = V_{SS}

AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS										UNIT
		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Time Between Refresh	t_{REF}		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		100		ns
CE Off Time	t_{CC}	130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	ns
Cycle Time	t_{CY}	470		470		400		380		320		ns
CE on Time	t_{CE}	300	3000	260	3000	230	3000	210	3000	200	3000	ns
CE Output Delay	t_{CO}		280		230		180		130		115	ns
Access Time	t_{ACC}		300		250		200		150		135	ns
CE to $\overline{WE}$	t_{WL}	40		40		40		40		40		ns
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		ns

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS										UNIT
		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{CY}	470		470		400		380		320		ns
Time Between Refresh	t_{REF}		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		100		ns
CE Off Time	t_{CC}	130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	ns
CE on Time	t_{CE}	300	3000	260	3000	230	3000	210	3000	200	3000	ns
$\overline{WE}$ to CE off	t_W	180		180		150		150		65		ns
CE to $\overline{WE}$	t_{CW}	300		260		230		210		200		ns
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		0		0		ns
D_{IN} Hold Time	t_{DH}	40		40		40		40		40		ns
$\overline{WE}$ Pulse Width	t_{WP}	180		180		150		100		65		ns

Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

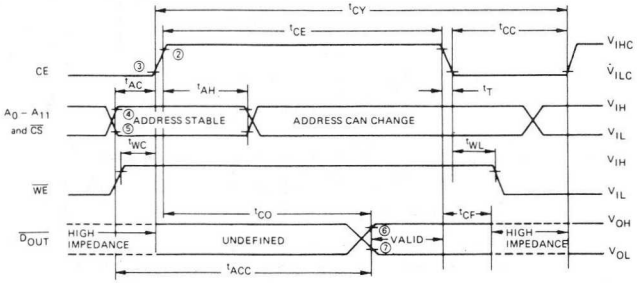
READ – MODIFY – WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = 5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS										UNIT
		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read–Modify–Write (RMW) Cycle Time	t_{RWC}	650		640		520		470		320		ns
Time Between Refresh	t_{REF}		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		100		ns
CE Off Time	t_{CC}	130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	ns
CE Width During RMW	t_{CRW}	480	3000	430	3000	350	3000	300	3000	200	3000	ns
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		ns
$\overline{WE}$ to CE off	t_W	180		180		150		150		65		ns
$\overline{WE}$ Pulse Width	t_{WP}	180		180		150		100		65		ns
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		0		ns
D_{IN} Hold Time	t_{DH}	40		40		40		40		40		ns
CE to Output Display	t_{CO}		280		230		180		130		115	ns
Access Time	t_{ACC}		300		250		200		150		135	ns

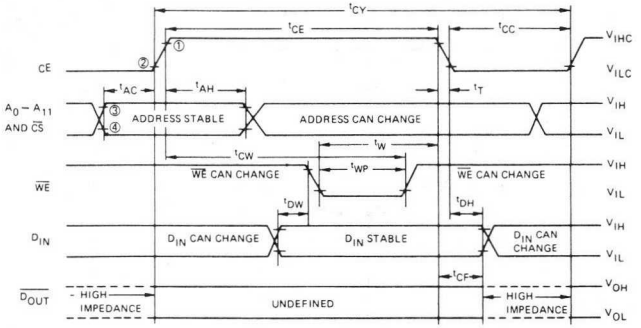
TIMING WAVEFORMS

READ CYCLE ①



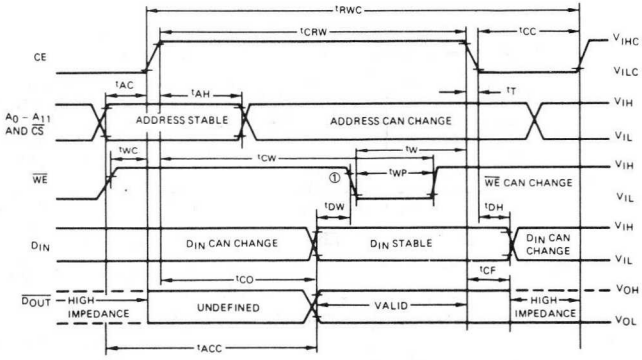
Notes ① For refresh cycle row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.
② V_{DD} -2V is the reference level for measuring timing of CE.
③ V_{SS} +2V is the reference level for measuring timing of CE.
④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
⑥ V_{SS} +2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.
⑦ V_{SS} +0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

WRITE CYCLE



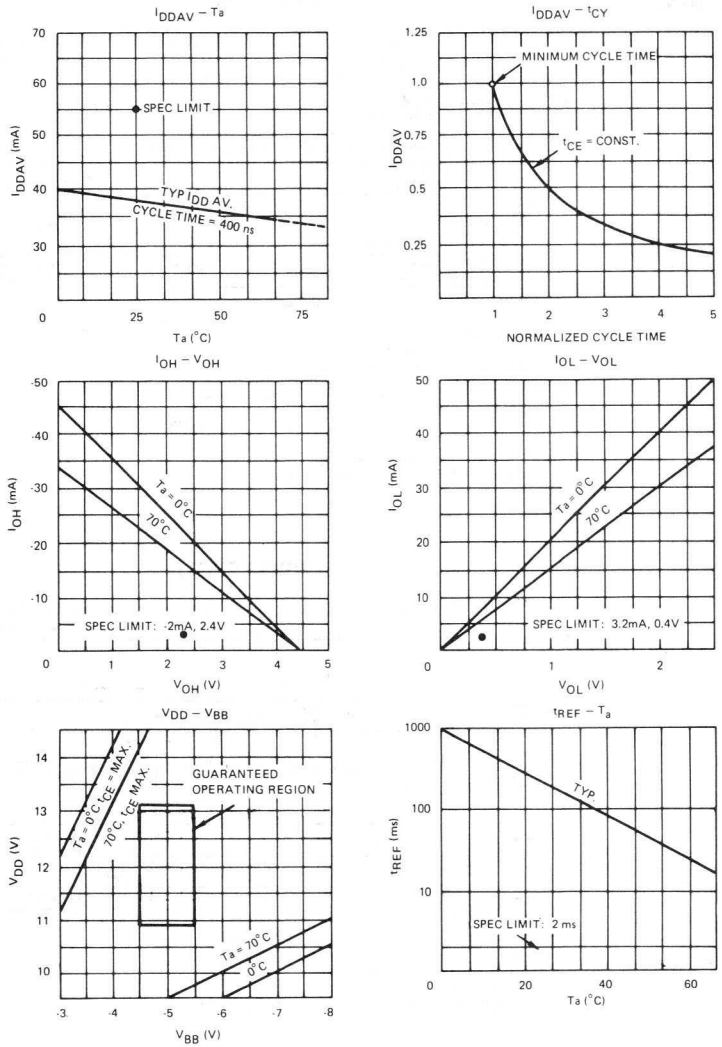
Notes ① V_{DD} -2V is the reference level for measuring timing of CE.
② V_{SS} +2V is the reference level for measuring timing of CE.
③ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
④ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

READ-MODIFY-WRITE CYCLE



Note ① $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

TYPICAL OPERATING CHARACTERISTICS (Except 411-4)



POWER CONSUMPTION

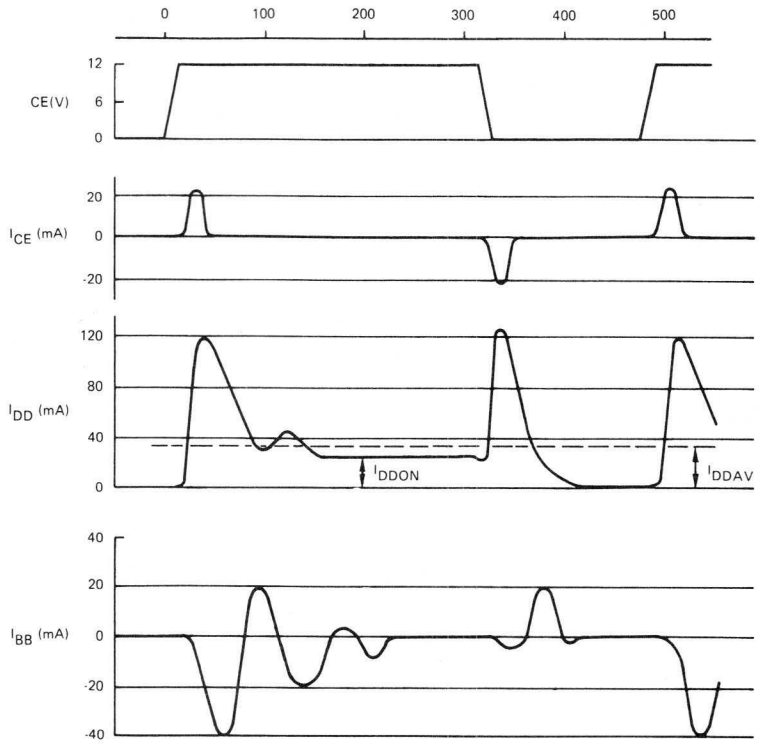
Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$.

Typical power dissiption for each product is shown below.

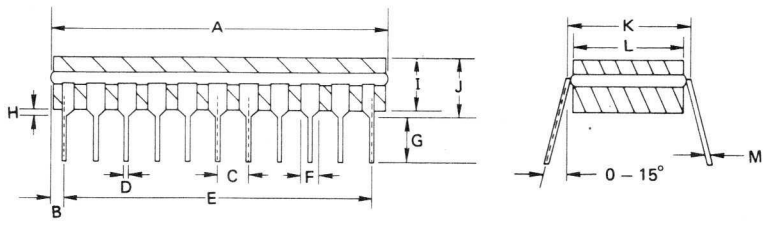
	mW (TYP.)	CONDITIONS
μPD411	450	Ta = 25° C, t_{cy} = 470ns, t_{CE} = 300ns
μPD411-1	450	Ta = 25° C, t_{cy} = 470ns, t_{CE} = 260ns
μPD411-2	450	Ta = 25° C, t_{cy} = 400ns, t_{CE} = 230ns
μPD411-3	550	Ta = 25° C, t_{cy} = 380ns, t_{CE} = 210ns
μPD411-4	660	Ta = 25° C, t_{cy} = 320ns, t_{CE} = 200ns

See above curves for power dissipation versus cycle time.

CURRENT WAVEFORMS



PACKAGE OUTLINE μPD411D



(Plastic)

ITEM	MILLIMETERS	INCHES
A	27.43 MAX	1.079 MAX
B	1.27 MAX	0.05 MAX
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 MAX	0.165 MAX
J	5.08 MAX	0.200 MAX
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

NOTES

4096 BIT DYNAMIC RAMS

DESCRIPTION

The μPD411A Family consists of four 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The μPD411A Family is designed using dynamic circuitry which reduces the standby power dissipation.

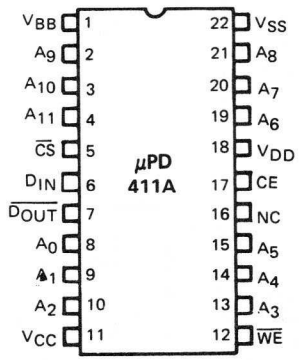
Reading information from the memory is non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

FEATURES

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power 0.7 mW (Typ.)
- Power Supply +12, +5, −5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Plastic Dual-in-Line Package
- Replacement for INTEL's 2107B, TI's 4060 and Equivalent Devices.
- 3 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
μPD411A	300 ns	470 ns	650 ns	2 ms
μPD411A-1	250 ns	430 ns	600 ns	2 ms
μPD411A-2	200 ns	400 ns	520 ns	2 ms

PIN CONFIGURATION



PIN NAMES

$A_0 - A_{11}$	Address Inputs
$A_0 - A_5$	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	(Powe. −5V)
NC	No Connection

Rev/1

FUNCTIONAL DESCRIPTION

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{CS}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{WE}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The $\overline{WE}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A_0–A_{11} Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

$\overline{D_{OUT}}$ Data Output

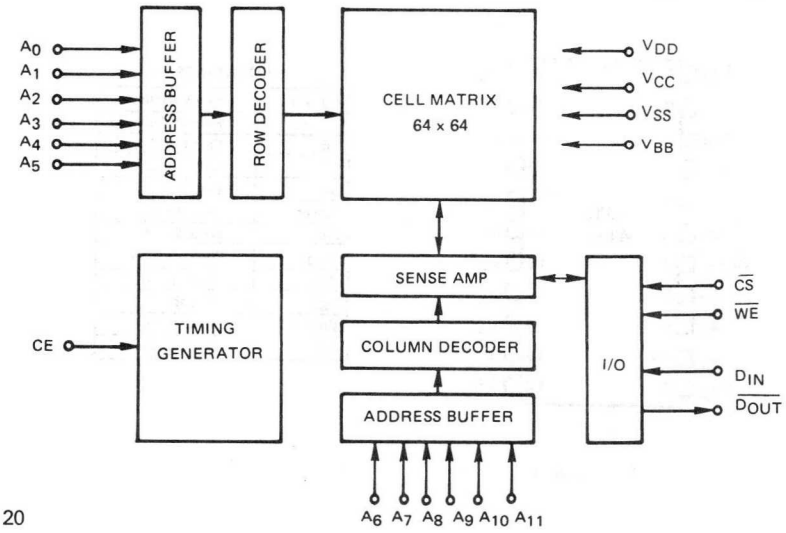
The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A_0 through A_5 or by addressing every row within any 2-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -55°C to +125°C
Output Voltage ① . . . . . +20 to -0.3 Volts
All Input Voltages ① . . . . . +20 to -0.3 Volts
Supply Voltage V_{DD} ① . . . . . +20 to -0.3 Volts
Supply Voltage V_{CC} ① . . . . . +20 to -0.3 Volts
Supply Voltage V_{SS} ① . . . . . +20 to -0.3 Volts
Power Dissipation 1.0W

Note: ① Relative to V_{BB}.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

*T_a = 25°C

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP. ①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}		0.01	10	μA	V_{IN} = V_{IL} MIN to V_{IH} MAX
CE Input Load Current	I_{LC}		0.01	10	μA	V_{IN} = V_{ILC} MIN to V_{IHC} MAX
Output Leakage Current for High Impedance State	I_{LO}		0.01	±10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DD} OFF		50	200	μA	CE = -1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DD} ON		35	50	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current						T_a = 25°C
μPD411A	I_{DD} AV		38	55	mA	Cycle Time = 470 ns
μPD411A-1	I_{DD} AV		38	55	mA	Cycle Time = 430 ns
μPD411A-2	I_{DD} AV		38	55	mA	Cycle Time = 400 ns
V_{BB} Supply Current ②	I_{BB}		5	100	μA	
V_{CC} Supply Current during CE off ③	I_{CC} OFF		0.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	-1.0		0.6	V	
Input High Voltage	V_{IH}	2.4		V_{CC} + 1	V	
CE Input Low Voltage	V_{ILC}	-1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD} - 1	V_{DD}	V_{DD} + 1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = -2.0 mA

Notes: ① Typical values are for T_a = 25°C and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage currents.
③ During CE on V_{CC} supply current is dependent on output loading.

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}			6	pF	V_{IN} = V_{SS}
$\overline{CS}$ Capacitance	C_{CS}			6	pF	V_{IN} = V_{SS}
D_{IN} Capacitance	C_{IN}			6	pF	V_{IN} = V_{SS}
$\overline{D_{OUT}}$ Capacitance	C_{OUT}			7	pF	V_{OUT} = V_{SS}
$\overline{WE}$ Capacitance	C_{WE}			7	pF	V_{IN} = V_{SS}
CE Capacitance	C_{CE1}			27	pF	V_{IN} = V_{SS}
	C_{CE2}			22	pF	V_{IN} = V_{DD}

READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A MIN	LIMITS μPD411A MAX	LIMITS μPD411A-1 MIN	LIMITS μPD411A-1 MAX	LIMITS μPD411A-2 MIN	LIMITS μPD411A-2 MAX	UNIT	TEST CONDITIONS
Time Between Refresh	t_{REF}		2		2		2	ms	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1 TTL Gate V_{ref} = 2.0 or 0.8 Volts
Address to CE Set Up Time	t_{AC}	0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		ns	
CE Off Time	t_{CC}	130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	ns	
Cycle Time	t_{CY}	470		430		400		ns	
CE on Time	t_{CE}	300	3000	260	3000	230	3000	ns	
CE Output Delay	t_{CO}		280		230		180	ns	
Access Time	t_{ACC}		300		250		200	ns	
CE to $\overline{WE}$	t_{WL}	40		40		40		ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		ns	

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A MIN	LIMITS μPD411A MAX	LIMITS μPD411A-1 MIN	LIMITS μPD411A-1 MAX	LIMITS μPD411A-2 MIN	LIMITS μPD411A-2 MAX	UNIT	TEST CONDITIONS
Cycle Time	t_{CY}	470		430		400		ns	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1 TTL Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		ns	
CE Off Time	t_{CC}	130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	ns	
CE on Time	t_{CE}	300	3000	260	3000	230	3000	ns	
$\overline{WE}$ to CE off	t_W	180		180		150		ns	
CE to $\overline{WE}$	t_{CW}	300		260		230		ns	
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		ns	
$\overline{WE}$ Pulse Width	t_{WP}	180		180		150		ns	

Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

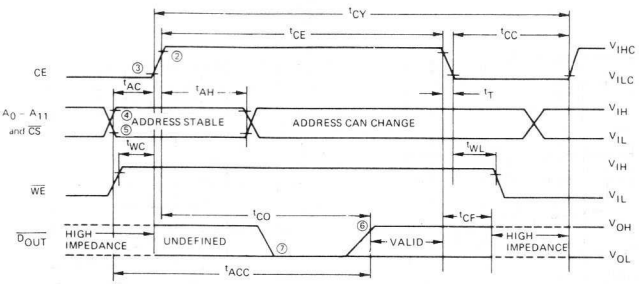
READ-MODIFY-WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

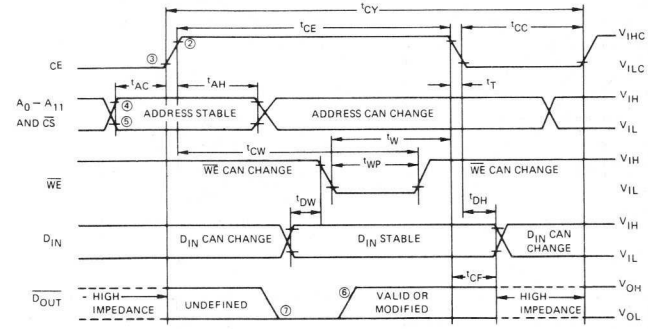
PARAMETER	SYMBOL	LIMITS μPD411A MIN	LIMITS μPD411A MAX	LIMITS μPD411A-1 MIN	LIMITS μPD411A-1 MAX	LIMITS μPD411A-2 MIN	LIMITS μPD411A-2 MAX	UNIT	TEST CONDITIONS
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	650		600		520		ns	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1 TTL Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		ns	
CE Off Time	t_{CC}	130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	ns	
CE Width During RMW	t_{CRW}	480	3000	430	3000	350	3000	ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		ns	
$\overline{WE}$ to CE off	t_W	180		180		150		ns	
$\overline{WE}$ Pulse Width	t_{WP}	180		180		150		ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		ns	
CE to Output Delay	t_{CO}		280		230		180	ns	
Access Time	t_{ACC}		300		250		200	ns	

TIMING WAVEFORMS

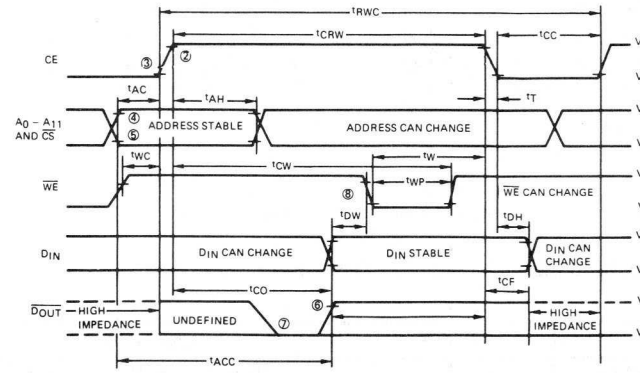
READ AND REFRESH CYCLE ①



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:

① For refresh cycle, row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.

② V_{DD} – 2V is the reference level for measuring timing of CE.

③ V_{SS} + 2V is the reference level for measuring timing of CE.

④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

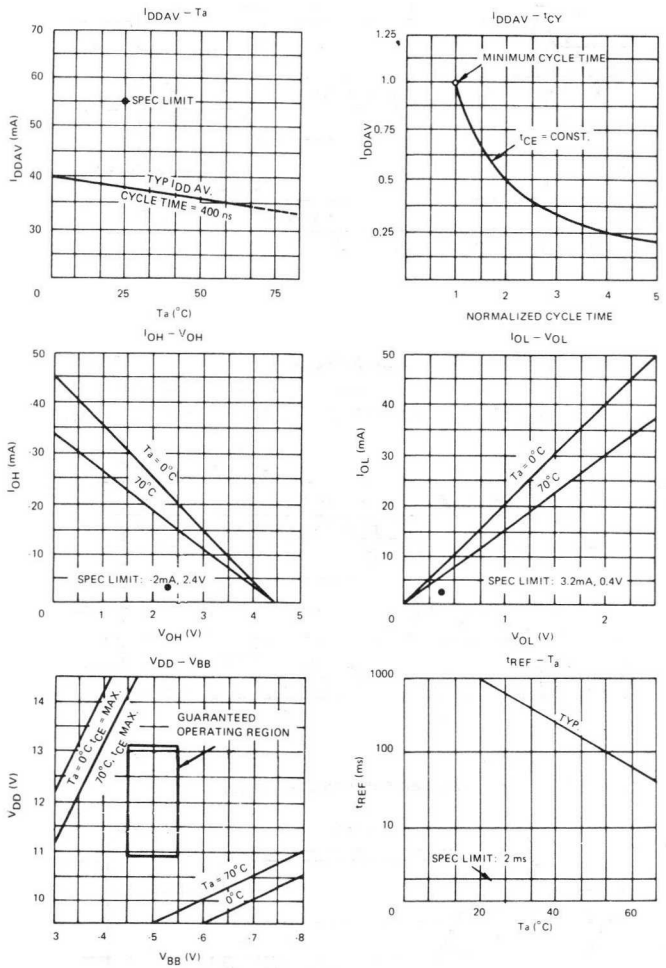
⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

⑥ V_{SS} + 2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑦ V_{SS} + 0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑧ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

TYPICAL OPERATING CHARACTERISTICS



POWER CONSUMPTION

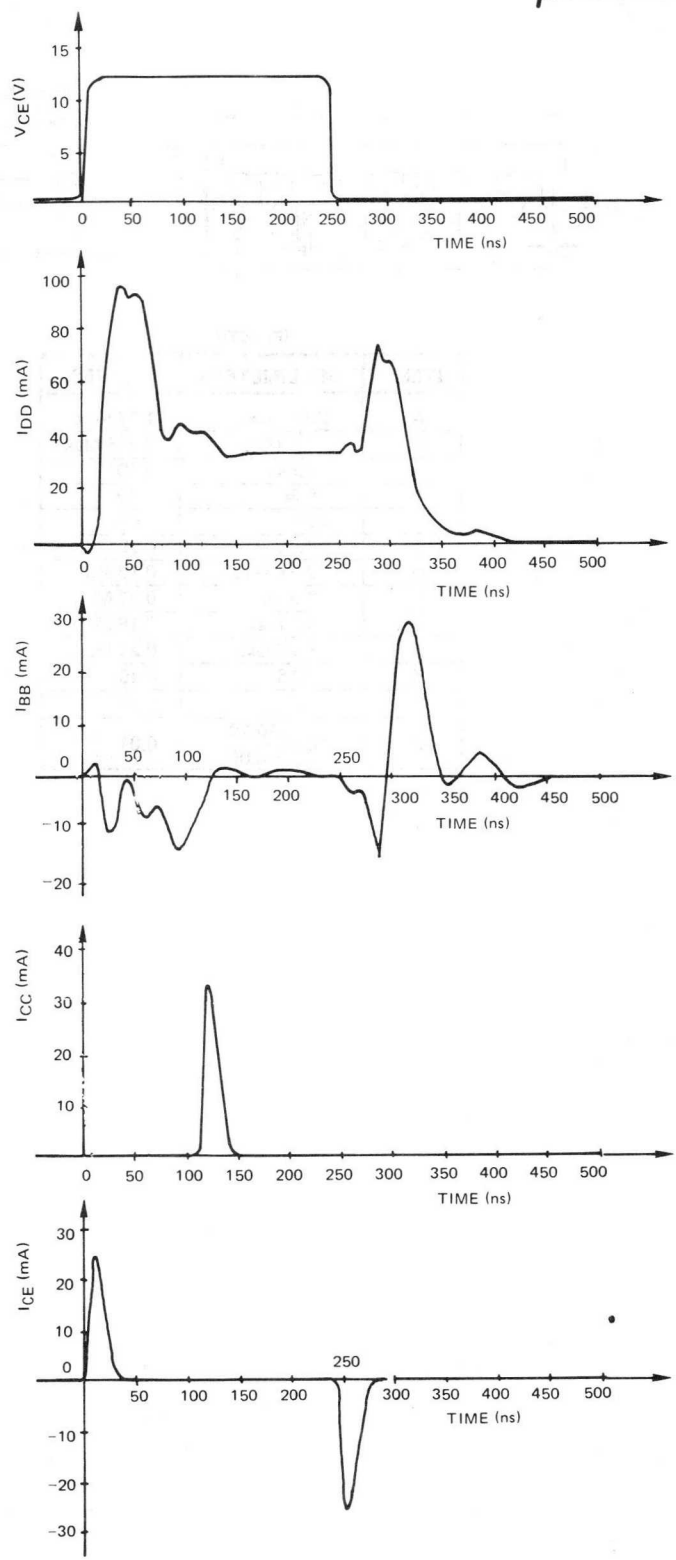
Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$

Typical power dissipation for each product is shown below.

	mW (TYP.)	CONDITIONS
μPD411A	460 mW	$T_a = 25°C$, $t_{cy} = 470$ ns, $t_{CE} = 300$ ns
μPD411A-1	460 mW	$T_a = 25°C$, $t_{cy} = 430$ ns, $t_{CE} = 260$ ns
μPD411A-2	460 mW	$T_a = 25°C$, $t_{cy} = 400$ ns, $t_{CE} = 230$ ns

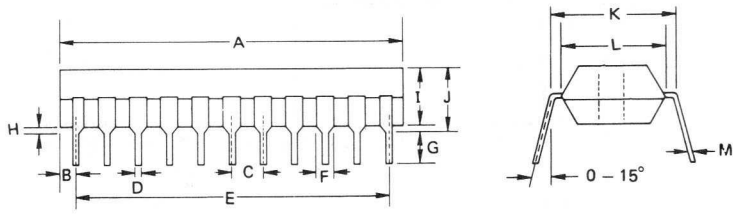
See curve above for power dissipation versus cycle time.

CURRENT WAVEFORMS ①



Note: ① V_{DD} = 12V, V_{BB} = −5.0V, V_{CC} = 5.0V

PACKAGE OUTLINE
μPD411AC



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The NEC μPD416 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

The μPD416 is fabricated using a double-poly-layer N channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

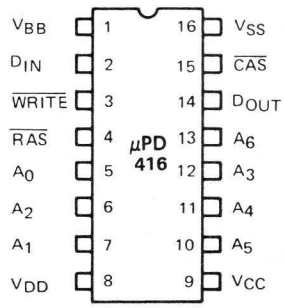
Multiplexed address inputs permit the μPD416 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FEATURES

- 16384 Words x 1 Bit Organization
- High Memory Density – 16 Pin Ceramic and Plastic Packages
- Multiplexed Address Inputs
- Standard Power Supplies +12V, -5V, +5V
- Low Power Dissipation; 462 mW Active (MAX), 40 mW Standby (MAX)
- Output Data Controlled by $\overline{CAS}$ and Unlatched at End of Cycle
- Read-Modify-Write, $\overline{RAS}$-only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Capacitance
- 128 Refresh Cycles
- 5 Performance Ranges:

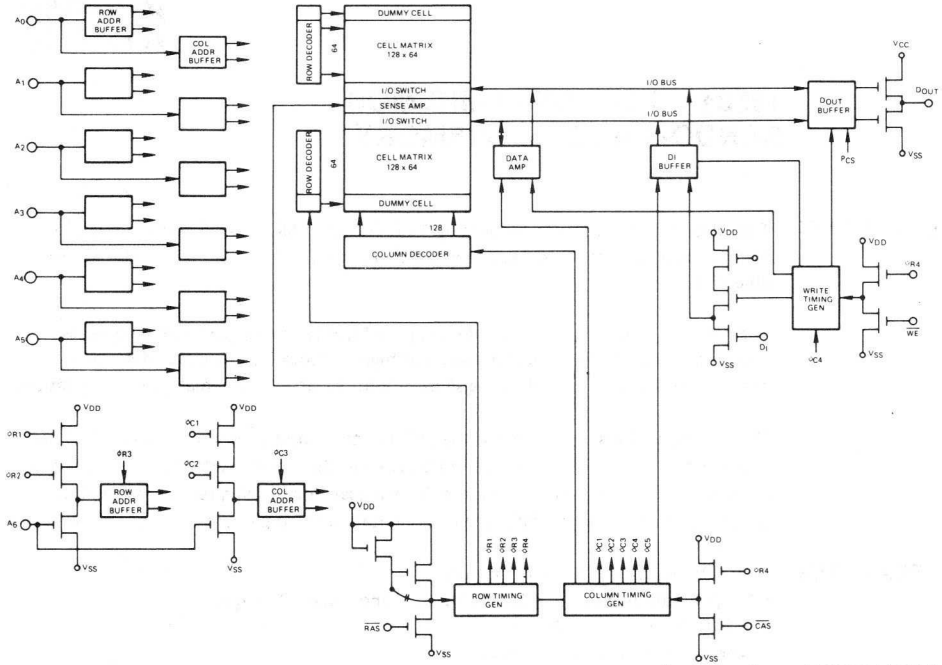
	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD416	300 ns	510 ns	575 ns
μPD416-1	250 ns	410 ns	465 ns
μPD416-2	200 ns	375 ns	375 ns
μPD416-3	150 ns	375 ns	375 ns
μPD416-5	120 ns	320 ns	320 ns

PIN CONFIGURATION



A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +20 Volts
All Input Voltages ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC} ②	−1.0 to +15 Volts
Short Circuit Output Current	50 mA
Power Dissipation	1 Watt

Notes: ① Relative to V_{BB}
② Relative to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%, V_{CC} = +5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}		4	5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}		8	10	pF	
Output Capacitance (D_{OUT})	C_O		5	7	pF	

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$ (1), $V_{DD} = +12V \pm 10\%$, $V_{CC} = +5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	(2)
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	(2) (3)
Supply Voltage	V_{SS}	0	0	0	V	(2)
Supply Voltage	V_{BB}	−4.5	−5.0	−5.5	V	(2)
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	(2)
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4		7.0	V	(2)
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0		0.8	V	(2)
Operating V_{DD} Current	I_{DD1}			35	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ Min. (4)
Standby V_{DD} Current	I_{DD2}			1.5	mA	$\overline{RAS} = V_{IHC}$, D_{OUT} = High Impedance
Refresh V_{DD} Current — All Speeds except μPD416-5	I_{DD3}			25	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IHC}$; $t_{RC} = 375$ ns (4)
Refresh V_{DD} Current — μPD416-5	I_{DD3}			27	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IHC}$; $t_{RC} = 375$ ns (4)
Page Mode V_{DD} Current	I_{DD4}			27	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; $t_{PC} = 225$ ns (4)
Operating V_{CC} Current	I_{CC1}				μA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = 375$ ns (5)
Standby V_{CC} Current	I_{CC2}	−10		10	μA	$\overline{RAS} = V_{IHC}$, D_{OUT} = High Impedance
Refresh V_{CC} Current	I_{CC3}	−10		10	μA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IHC}$, $t_{RC} = 375$ ns
Page Mode V_{CC} Current	I_{CC4}				μA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = 225$ ns (5)
Operating V_{BB} Current	I_{BB1}			200	μA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = 375$ ns
Standby V_{BB} Current	I_{BB2}			100	μA	$\overline{RAS} = V_{IHC}$, D_{OUT} = High Impedance
Refresh V_{BB} Current	I_{BB3}			200	μA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IHC}$, $t_{RC} = 375$ ns
Page Mode V_{BB} Current	I_{BB4}			200	μA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; $t_{PC} = 225$ ns
Input Leakage (any input)	$I_{I(L)}$	−10		10	μA	$V_{BB} = -5V$, $0V \leq V_{IN} \leq +7V$, all other pins not under test = 0V
Output Leakage	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, $0V \leq V_{OUT} \leq +5.5V$
Output High Voltage (Logic 1)	V_{OH}	2.4			V	$I_{OUT} = -5$ mA (3)
Output Low Voltage (Logic 0)	V_{OL}			0.4	V	$I_{OUT} = 4.2$ mA

Notes: (1) T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met. See Figure 1 for derating curve.

(2) All voltages referenced to V_{SS}.

(3) Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

(4) I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.

(5) I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS
		μPD416		μPD416-1		μPD416-2		μPD416-3		μPD416-5			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	510		410		375		320		320		ns	③
Read-write cycle time	t_{RWC}	575		465		375		375		320		ns	③
Page mode cycle time	t_{PC}	330		275		225		170		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		300		250		200		150		120	ns	④ ⑥
Access time from $\overline{CAS}$	t_{CAC}		200		165		135		100		80	ns	⑤ ⑥
Output buffer turn-off delay	t_{OFF}	0	80	0	60	0	50	0	40	0	35	ns	⑦
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	35	3	35	ns	②
$\overline{RAS}$ precharge time	t_{RP}	200		150		120		100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	300	10,000	250	10,000	200	32,000	150	32,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	200		165		135		100		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	200	10,000	165	10,000	135	10,000	100	10,000	80	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	40	100	35	85	25	65	20	50	15	40	ns	⑧
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	-20		-20		-20		-20		0		ns	
Row address set-up time	t_{ASR}	0		0		0		0		0		ns	
Row address hold time	t_{RAH}	40		35		25		20		15		ns	
Column address set-up time	t_{ASC}	-10		-10		-10		-10		-10		ns	
Column address hold time	t_{CAH}	90		75		55		45		40		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	190		160		120		95		80		ns	
Read command set-up time	t_{RCS}	0		0		0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		0		0		ns	
Write command hold time	t_{WCH}	90		75		55		45		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	190		160		120		95		80		ns	
Write command pulse width	t_{WP}	90		75		55		45		40		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	120		85		70		50		50		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	120		85		70		50		50		ns	
Data-in set-up time	t_{DS}	0		0		0		0		0		ns	⑨
Data-in hold time	t_{DH}	90		75		55		45		40		ns	⑨
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	190		160		120		95		80		ns	
CAS precharge time (for page mode cycle only)	t_{CP}	120		100		80		60		60		ns	
Refresh period	t_{REF}		2		2		2		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	-20		-20		20		-20		0		ns	⑩
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	140		125		95		70		80		ns	⑩
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	240		200		160		120		120		ns	⑩

Notes:

① AC measurements assume t_T = 5 ns.

② V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}

③ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured.

④ Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

⑤ Assumes that $t_{RCD} \geq t_{RCD}$ (max).

⑥ Measured with a load equivalent to 2 TTL loads and 100 pF.

⑦ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

⑧ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}

⑨ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

⑩ t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) $\geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

DERATING CURVES

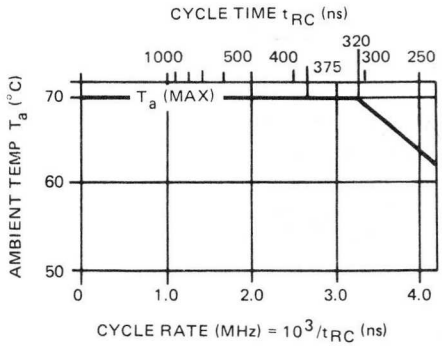


FIGURE 1

Maximum ambient temperature versus cycle rate for extended frequency operation. T_a (max) for operation at cycling rates greater than 2.66 MHz (t_{CYC} < 375 ns) is determined by T_a (max) [°C] = 70 – 9.0 x (cycle rate [MHz] –2.66). For μPD416-5, it is T_a (max) [°C] = 70 – 9.0 (cycle rate [MHz] – 3.125).

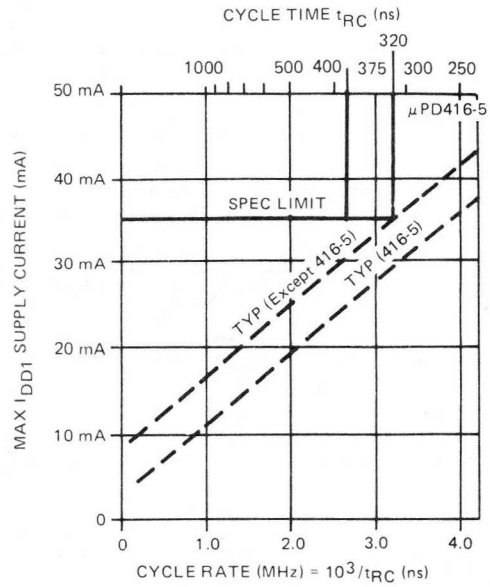


FIGURE 2

Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

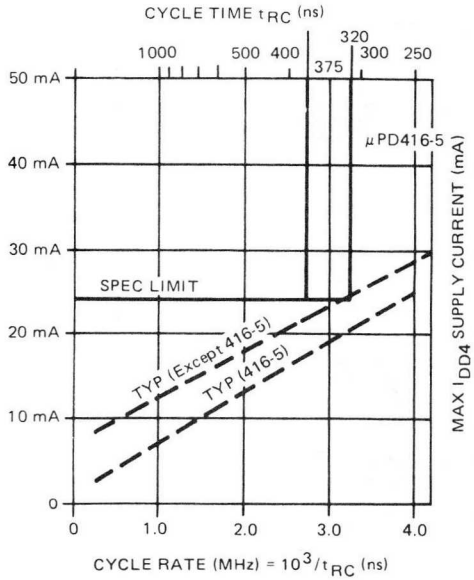


FIGURE 3

Maximum I_{DD3} versus cycle rate for device operation at extended frequencies.

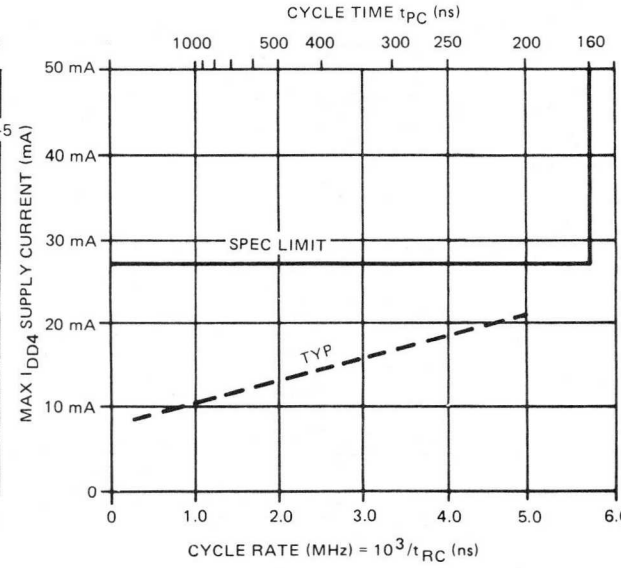
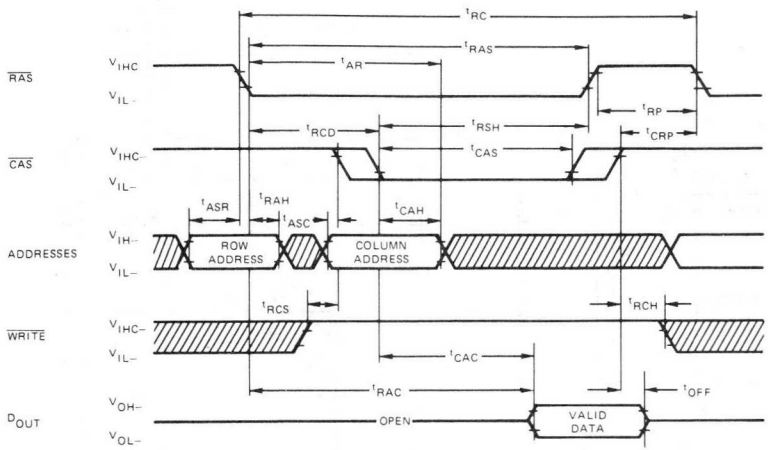


FIGURE 4

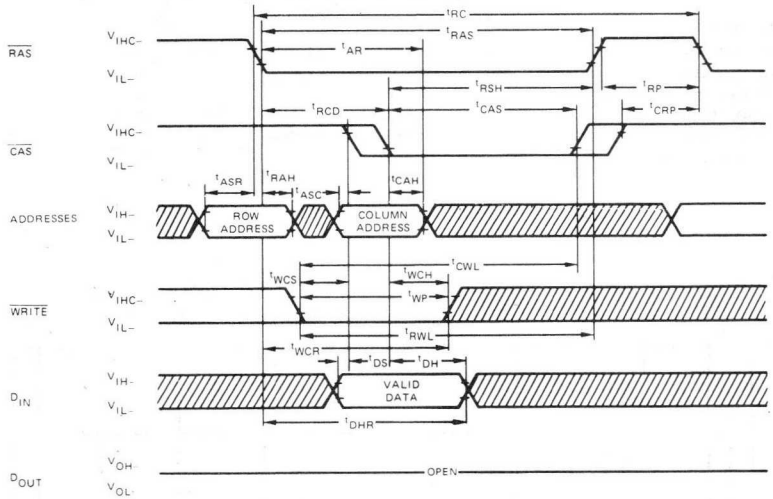
Maximum I_{DD4} versus cycle rate for device operation in page mode.

TIMING WAVEFORMS

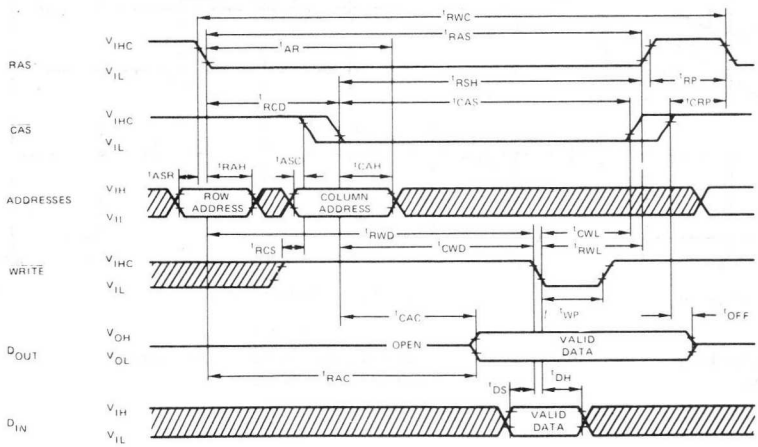
READ CYCLE



WRITE CYCLE

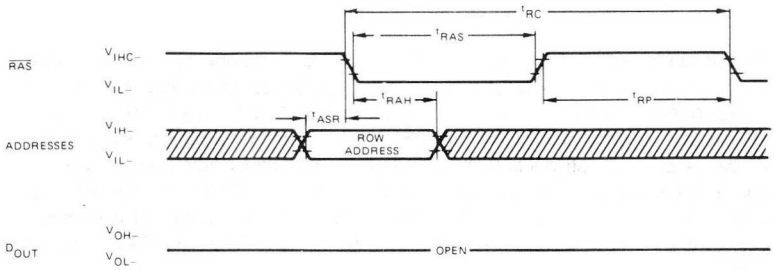


READ-WRITE/READ-MODIFY–WRITE CYCLE



TIMING WAVEFORMS (CONT.)

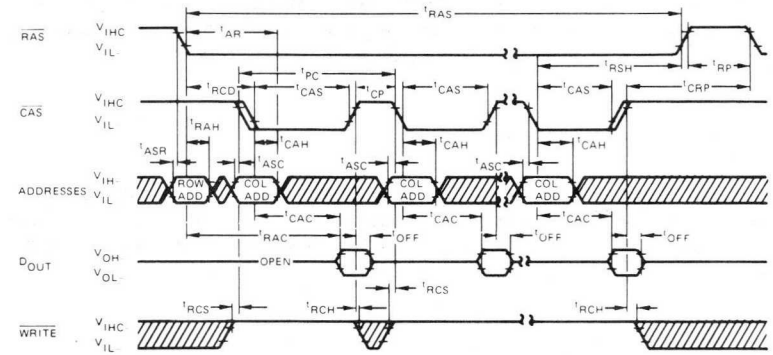
"$\overline{RAS}$-ONLY" REFRESH CYCLE



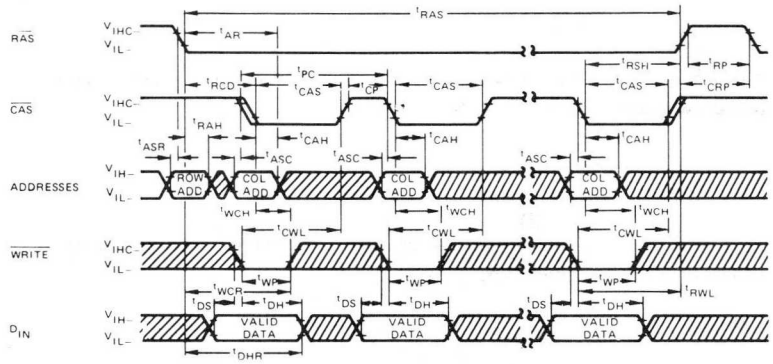
Note $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care

3

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ADDRESSING

The 14 address bits required to decode 1 of 16,384 bit locations are multiplexed onto the 7 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{RAS}$), and the Column Address Strobe ($\overline{CAS}$). The 7 bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the 7 bit column address is applied and $\overline{CAS}$ is brought low. Since the column address is not needed internally until a time of t_{CRD} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{CRD} MAX. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, this is an "early WRITE" cycle and data out will remain in the high impedance state throughout the cycle. For a READ, WRITE, OR READ-MODIFY-WRITE cycle, the data output will contain the data in the selected cell after the access time. Data out will assume the high impedance state anytime that $\overline{CAS}$ goes high.

PAGE MODE

The page mode feature allows the μPD416 to be read or written at multiple column addresses for the same row address. This is accomplished by maintaining a low on $\overline{RAS}$ and strobing the new column addresses with $\overline{CAS}$. This eliminates the setup and hold times for the row address resulting in faster operation.

REFRESH

Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 128 row addresses every 2 milliseconds or less. Because data out is not latched, "$\overline{RAS}$ only" cycles can be used for simple refreshing operation.

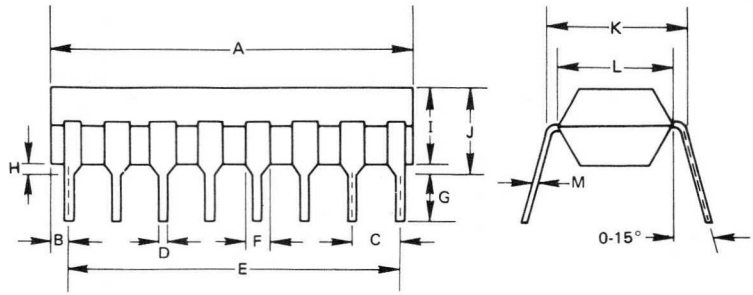
CHIP SELECTION

Either $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded for chip select function. Unselected chip outputs will remain in the high impedance state.

POWER SEQUENCING

In order to assure long term reliability, V_{BB} should be applied first during power up and removed last during power down.

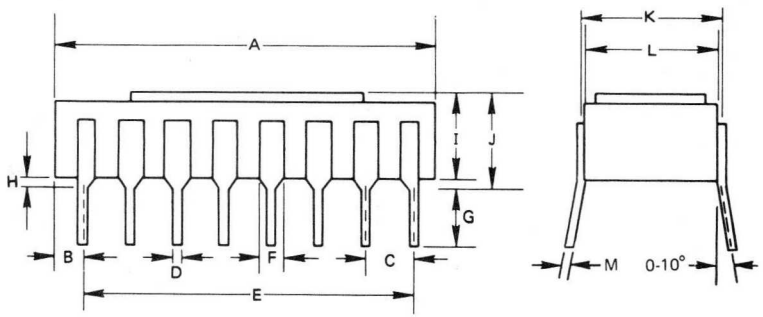
PACKAGE OUTLINE
μPD416C



(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

μPD416D



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.8	0.30
L	7.3	0.29
M	0.27	0.01

NOTES

NEC
μPD2118
μPD2118-2
μPD2118-3
PRELIMINARY

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD2118 is a single +5V power supply, 16384 word by 1 bit Dynamic MOS RAM. The μPD2118 achieves high speed with low power dissipation by the use of single transistor dynamic storage cell design and advanced dynamic circuitry. This circuit design results in the minimizing of current transients typical of dynamic RAMS. This in turn results in high noise immunity of the μPD2118 in a system environment. By using a multiplexing technique, the μPD2118 can be packaged in an industry standard 16-Pin Dip utilizing 7 address input pins for the 14 address bits required. The two 7 bit address words are referred to as the ROW and COLUMN address. Two TTL clocks, ROW address strobe ($\overline{RAS}$) and COLUMN address strobe ($\overline{CAS}$) latch these two words into the μPD2118. Non-critical timing requirements for $\overline{RAS}$ and $\overline{CAS}$ permit high systems performance without placing difficult constraints upon the multiplexing control circuitry.

The μPD2118 has a three-state output controlled by $\overline{CAS}$, independent of $\overline{RAS}$. Following a valid read or read-modify-write cycle, data will be held in the output by holding $\overline{CAS}$ low. Returning $\overline{CAS}$ to a high state will result in the data out pin reverting to the high impedance mode. Use of this $\overline{CAS}$ controlled output means that the μPD2118 can perform hidden refresh by holding $\overline{CAS}$ low to maintain latch data output while using $\overline{RAS}$ to execute $\overline{RAS}$-only-refresh cycles.

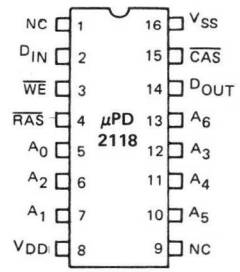
The use of single transistor storage cell circuitry requires that data be periodically refreshed. Refreshing can be accomplished by performing $\overline{RAS}$-only-refresh cycles, hidden refresh cycles or normal read or write cycles on each of the 128 address combinations of A0 through A6 during a 2 ms period. The write cycle will refresh stored data on all bits of the selected row, except that the bit which is addressed will be modified to reflect the data input.

FEATURES

- Single +5V Supply, ±10% Tolerance
- Low Power: 138 mW Max Operating
  16 mW Max Standby
- Low VDD Current Transients
- All Inputs, Including Clocks, TTL Compatible
- Non-Latched Output is Three-State
- $\overline{RAS}$-Only-Refresh
- 128 Refresh Cycles Required
- Page Mode Capability
- $\overline{CAS}$ Controlled Output Allows Hidden Refresh

P/N	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD2118	150 ns	320 ns	410 ns
μPD2118-2	120 ns	270 ns	345 ns
μPD2118-3	100 ns	235 ns	295 ns

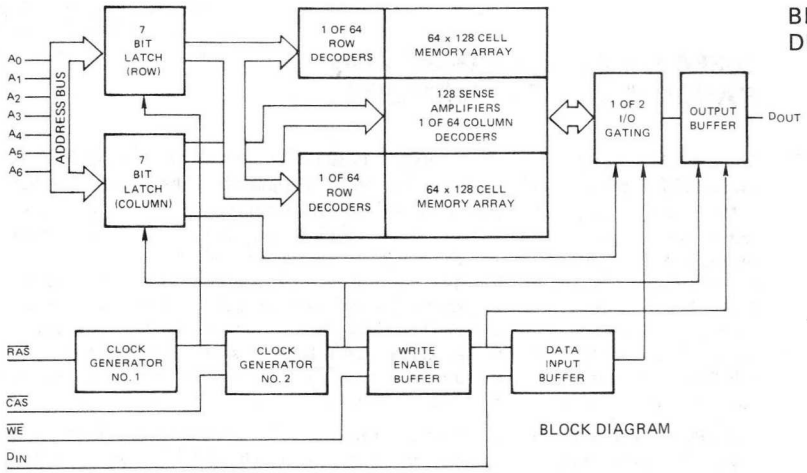
PIN CONFIGURATION



PIN NAMES

A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
$\overline{RAS}$	ROW ADDRESS STROBE
V_{DD}	POWER (+5V)
V_{SS}	GROUND

BLOCK DIAGRAM



BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin Relative to VSS	−2.0 to +7.5V
Data Out Current	50 mA
Power Dissipation	1.0W

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS READ, WRITE, AND READ MODIFY WRITE CYCLES ①

T_a = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER		SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS	NOTES
Input Load Current		I_{LI}		10	μA	V_{IN} = V_{SS} to V_{DD}	
Output Leakage Current for High Impedance State		I_{LO}		10	μA	Chip Deselected $\overline{CAS}$ at V_{IH}, V_{OUT} = 0 to 5.5V	
V_{DD} Supply Current (Standby)		I_{DD1}		3	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}	
V_{DD} Supply Current (Operating)	μPD2118-3	I_{DD2}		25	mA	TRC = TRC Min	②
	μPD2118-2	I_{DD2}		22	mA		
	μPD2118-0	I_{DD2}		22	mA		
V_{DD} Supply Current (RAS-Only Cycle)	μPD2118-3	I_{DD3}		20	mA	TRC = TRC Min	②
	μPD2118-2	I_{DD3}		18	mA		
	μPD2118-0	I_{DD3}		18	mA		
V_{DD} Supply Current Page Mode, Maximum t_{PC} Minimum t_{CAS}	μPD2118-3	I_{DD4}		20	mA		②
	μPD2118-2	I_{DD4}		17	mA		
	μPD2118-0	I_{DD4}		15	mA		
V_{DD} Supply Current (Standby, Output Enabled)		I_{DD5}		4	mA	$\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH}	②
Input Low Voltage		V_{IL}	−2.0	0.8	V		
Input High Voltage		V_{IH}	2.4	7.0	V		
Output Low Voltage		V_{OL}		0.4	V	I_{OL} = 4.2 mA	
Output High Voltage		V_{OH}	2.4			I_{OH} = −5 mA	

Notes: ① All voltages referenced to V_{SS}.

② I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} Max is measured with the output open.

CAPACITANCE ①

T_a = 25°C, VDD = 5V ± 10%, VSS = 0V, unless otherwise noted.

SYMBOL	PARAMETER	TYP	MAX	UNIT
CI1	Address, Data In	3	5	pF
CI2	$\overline{RAS}$, $\overline{WE}$	4	7	pF
CI3	$\overline{CAS}$	6	10	pF
CO	Data Out	4	7	pF

NOTES: ① Capacitance measured with Boonton meter or effective capacitance calculated from the Equation C = I ΔT/ΔV with ΔV equal to 3V and power supplies at nominal levels.

AC CHARACTERISTICS①②③*

T_a = 0°C to 70°C; V_{DD} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.

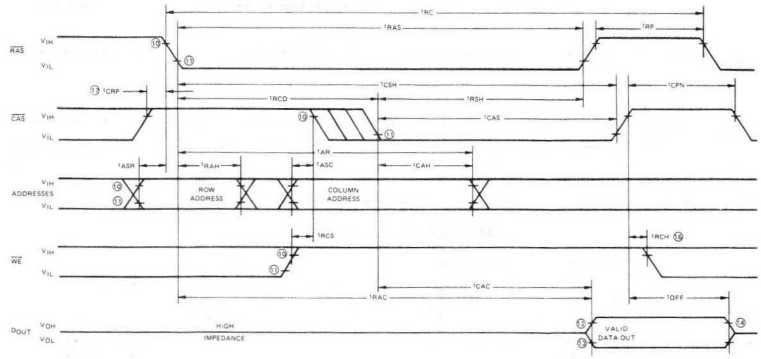
READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

SYMBOL	PARAMETER	μPD2118-3		μPD2118-2		μPD2118-0		UNIT	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RAC}	Access Time From $\overline{RAS}$		100		120		150	ns	④ ⑤
t_{CAC}	Access Time From $\overline{CAS}$		50		65		80	ns	④ ⑤ ⑥
t_{REF}	Time Between Refresh		2		2		2	ms	
t_{RP}	$\overline{RAS}$ Precharge Time	110		120		135		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time (non-page-mode cycles)	50		55		70		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	55	25	70	ns	⑦
t_{RSH}	$\overline{RAS}$ Hold Time	65		85		105		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	110		135		165		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	10		10		15		ns	
t_{ASC}	Column Address Set-Up Time	0		0		0		ns	
t_{CAH}	Column Address Hold Time	15		15		20		ns	
t_{AR}	Column Address Hold Time, to $\overline{RAS}$	65		70		90		ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	⑧
t_{OFF}	Output Buffer Turn Off Delay	0	45	0	50	0	60	ns	
	READ AND REFRESH CYCLES								
t_{RC}	Random Read Cycle Time	235		270		320		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	115	10,000	140	10,000	175	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	80	10,000	95	10,000	ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
	WRITE CYCLE								
t_{RC}	Random Write Cycle Time	235		270		320		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	115	10,000	140	10,000	175	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	80	10,000	95	10,000	ns	
t_{WCS}	Write Command Set-Up Time	0		0		0		ns	⑨
t_{WCH}	Write Command Hold Time	30		35		45		ns	
t_{WCR}	Write Command Hold Time, to $\overline{RAS}$	80		90		115		ns	
t_{WP}	Write Command Pulse Width	35		40		50		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	70		90		110		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	65		85		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		ns	
t_{DH}	Data-In Hold Time	30		35		45		ns	
t_{DHR}	Data-In Hold Time, to $\overline{RAS}$	80		90		115		ns	
	READ-MODIFY-WRITE CYCLE								
t_{RWC}	Read-Modify-Write Cycle Time	295		345		410		ns	
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	175	10,000	215	10,000	265	10,000	ns	
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	120	10,000	155	10,000	185	10,000	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100		120		150		ns	⑨
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	50		65		80		ns	⑨
	PAGE MODE CYCLE								
t_{PC}	Page Mode Read or Write Cycle	130		160		190		ns	
t_{PCM}	Page Mode Read-Modify-Write	190		235		280		ns	
t_{CP}	$\overline{CAS}$ Precharge Time, Page Cycle	60		70		85		ns	
t_{RPM}	$\overline{RAS}$ Pulse Width, Page Mode	125	10,000	150	10,000	175	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	80	10,000	95	10,000	ns	

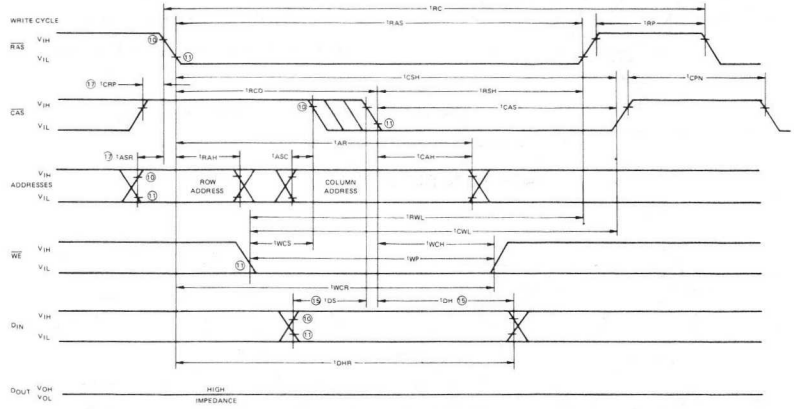
*NOTES: See page 7.

TIMING WAVEFORMS

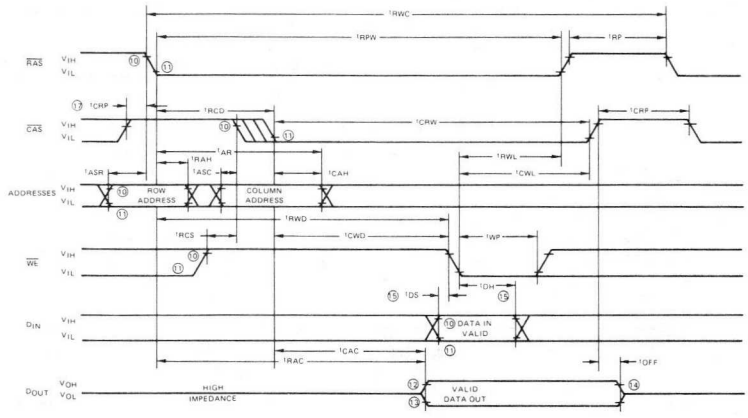
READ CYCLE



WRITE CYCLE

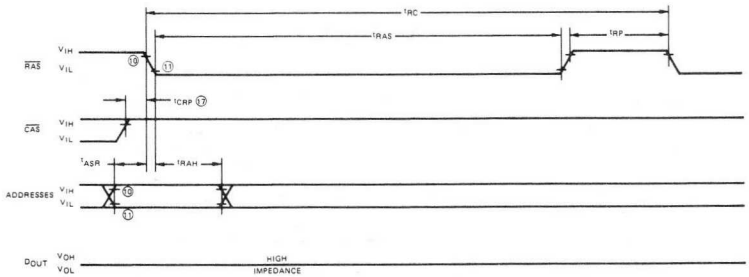


READ-MODIFY-WRITE CYCLE

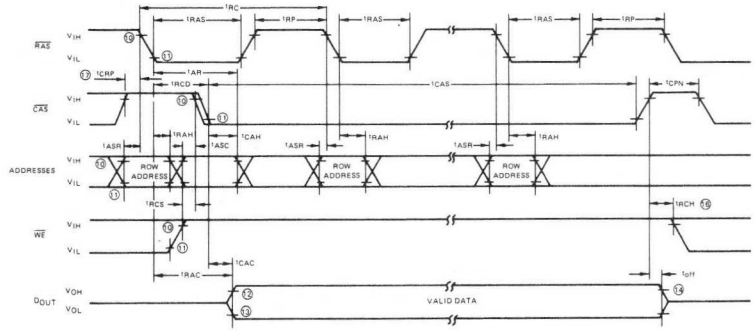


NOTES: See page 7.

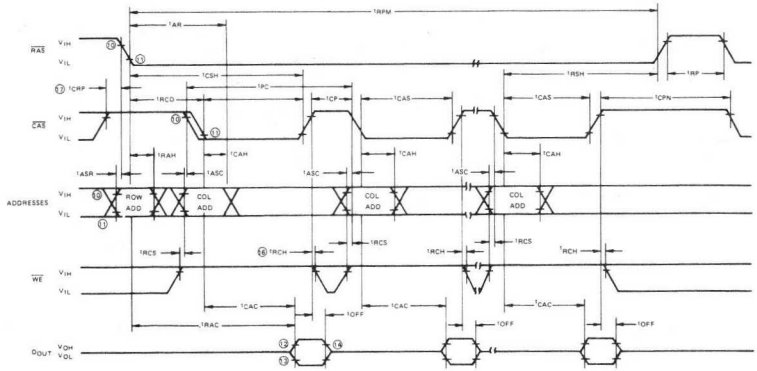
$\overline{RAS}$-ONLY REFRESH CYCLE



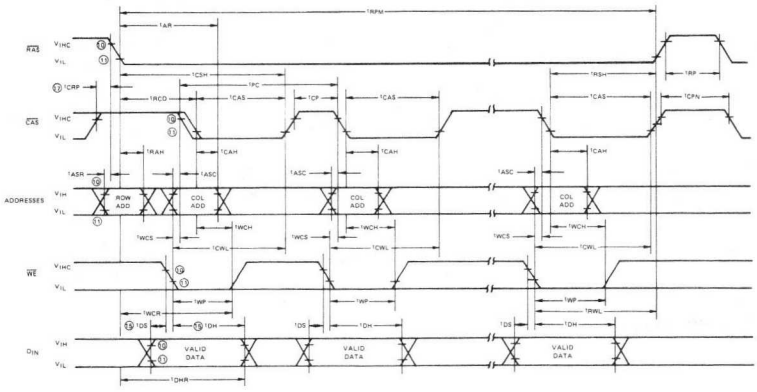
HIDDEN REFRESH CYCLE



PAGE MODE READ CYCLE

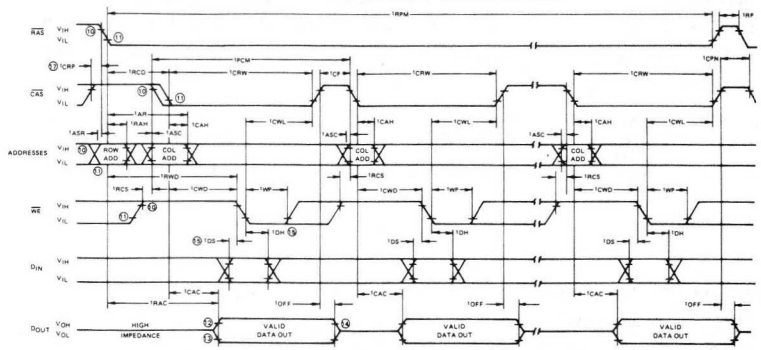


PAGE MODE WRITE CYCLE



TIMING WAVEFORMS (CONT.)

PAGE MODE READ-MODIFY-WRITE CYCLE



Notes:
1. All voltages referenced to V_{SS}.
2. Eight cycles are required after power-up or prolonged periods greater than 2 ms of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. AC Characteristics assume t_T = 5 ns.
4. Assume that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than t_{RCD} (max), then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max).
5. Load = 2 TTL loads and 100pF.
6. Assumes $t_{RCD} \geq t_{RCD}$ (max).
7. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is less than t_{RCD} (max) access time is t_{RAC}. If t_{RCD} is greater than t_{RCD} (max) access time is $t_{RCD} + t_{CAC}$.
8. measured between V_{IH} (min) and V_{IL} (max).
9. t_{CWD} and t_{RWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an early cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
10. 11. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals.
12. 13. V_{OH} min and V_{OL} max are reference levels for measuring timing of D_{OUT}.
14. t_{OFF} is measured to $|I_{OUT}| < |I_{LO}|$.
15. t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
16. t_{RCH} is referenced to the trailing edge of $\overline{CAS}$ or $\overline{RAS}$, whichever occurs first.
17. t_{CRP} requirements is only applicable for $\overline{RAS}/\overline{CAS}$ cycles preceeded by a CAS-only cycle (i.e., for systems where CAS has not been decoded with RAS).

READ CYCLE

A Read cycle is performed by maintaining Write Enable ($\overline{WE}$) high during a $\overline{RAS}/\overline{CAS}$ operation. The output pin of a selected device will remain in a high impedance state until valid data appears at the output at access time. Device access time, t_{ACC}, is the longer of the two calculated intervals $t_{ACC} = t_{RAC}$ or $t_{ACC} = t_{RCD} + t_{CAC}$.

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe delay time, t_{RCD}, are system dependent timing parameters. For example, substituting the device parameters of the μPD2118-3 yields $t_{ACC} = t_{RAC}$ = 100 nsec for 20 nsec $\leq t_{RCD} \leq$ 50 nsec, but $t_{ACC} = t_{RCD} + t_{CAC} = t_{RCD}$ + 50 for $t_{RCD} >$ 50 nsec.

Note that if 20 nsec $\leq t_{RCD} \leq$ 50 nsec device access time is determined by the first equation and is equal to t_{RAC}. If $t_{RCD} >$ 50 nsec, access time is determined by the second equation. This 30 nsec interval (shown in the t_{RCD} inequality in the first equation) in which the falling edge of $\overline{CAS}$ can occur without affecting access time is provided to allow for system timing skew in the generation of $\overline{CAS}$.

REFRESH CYCLES

Each of the 128 rows of the μPD2118 must be refreshed every 2 milliseconds to maintain data. Any memory cycle (read, write, or $\overline{RAS}$ only) refreshes the selected row as defined by the low order ($\overline{RAS}$) addresses. Any Write cycle, of course, may change the state of the selected cell. Using a Read, Write, or Read-Modify-Write cycle for refresh is not recommended for systems which utilize "wire-OR" outputs since output bus contention will occur.

A $\overline{RAS}$-only refresh cycle is the recommended technique for most applications to provide for data retention. A $\overline{RAS}$-only refresh cycle maintains the D_{OUT} in the high impedance state with a typical power reduction of 20% over a Read or Write cycle.

$\overline{RAS}/\overline{CAS}$ TIMING

$\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as defined by t_{RAS} and t_{CAS} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle once begun by bringing $\overline{RAS}$ and/or $\overline{CAS}$ low must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle can not begin until the minimum precharge time, t_{RP}, has been met.

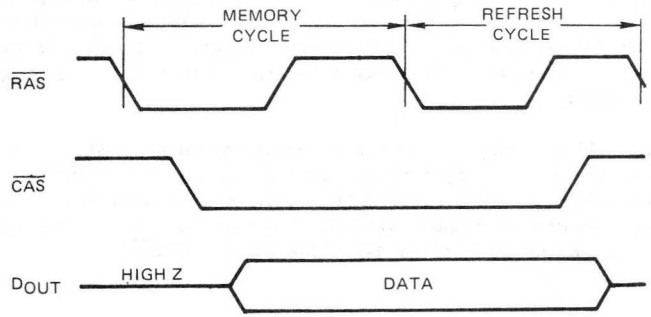
DATA OUTPUT OPERATION

Data Output (D_{OUT}), which has three-state capability, is controlled by $\overline{CAS}$. During $\overline{CAS}$ high state ($\overline{CAS}$ at V_{IH}) the output is in the high impedance state. The following table summarizes the D_{OUT} state for various types of cycles.

Type of Cycle	D_{OUT} State
Read Cycle	Data From Addressed Memory Cell
Early Write Cycle	HI-Z
$\overline{RAS}$-Only Refresh Cycle	HI-Z
$\overline{CAS}$-Only Cycle	HI-Z
Read/Modify/Write Cycle	Data From Addressed Memory Cell
Delayed Write Cycle	Indeterminate

HIDDEN REFRESH

A feature of the μPD2118 is that refresh cycles may be performed while maintaining valid data at the output pin. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}) executing a "$\overline{RAS}$-Only" refresh cycle, but with $\overline{CAS}$ held low (see Figure below).



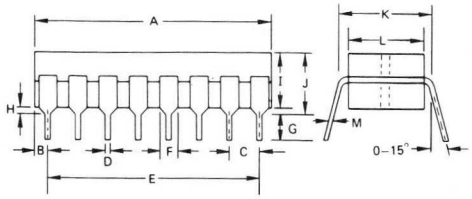
This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

POWER ON

The μPD2118 requires no power on sequence. After the application of the V_{DD} supply, or after extended periods of bias (greater than 2 ms) without clocks, the device must perform a minimum of eight (8) initialization cycles (any combination of cycles containing a $\overline{RAC}$ clock such as $\overline{RAS}$-only refresh) prior to normal operation.

The V_{DD} current (I_{DD}) requirement of the μPD2118 during power on is, however, dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If the input levels of these clocks are at V_{IH} or V_{DD}, whichever is lower, the I_{DD} requirement per device is I_{DD1} (I_{DD} standby). If the input levels for the two clocks are lower than V_{IH} or V_{DD}, the I_{DD} requirement will be greater than I_{DD1}. For large systems, this current requirement for I_{DD} could be substantially more than that for which the system has been designed. A system which has been designed assuming the majority of devices to be operating in the refresh/standby mode may produce sufficient I_{DD} loading such that the power supply might current limit. To assure that the system will not experience such loading during power on, a pullup resistor for each clock input to V_{DD} to maintain the non-selected current level (I_{DD1}) for the power supply is recommended.

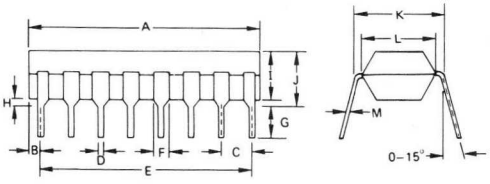
PACKAGE OUTLINE μPD2118D



Cerdip

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

μPD2118C



Plastic

ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.05 MAX	0.16 MAX
J	4.55 MAX	0.18 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

NOTES

NEC

μPD4164-1
μPD4164-2
μPD4164-3

PRELIMINARY

65,536 x 1 BIT DYNAMIC RANDOM ACCESS MEMORY

3

DESCRIPTION

The NEC μPD4164 is a 65,536 words by 1 bit Dynamic N-Channel MOS RAM designed to operate from a single +5V power supply. The negative-voltage substrate bias is internally generated — its operation is both automatic and transparent.

The μPD4164 utilizes a double-poly-layer N-channel silicon gate process which provides high storage cell density, high performance and high reliability.

The μPD4164 uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 512 sense amplifiers, which assures that power dissipation is minimized. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between Dynamic RAM generations.

The μPD4164 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The μPD4164 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$ only refresh cycles.

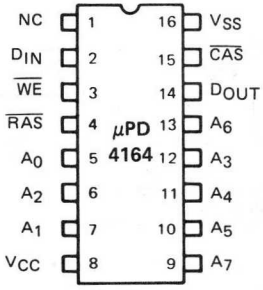
Refreshing is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of A_0 through A_6 during a 2 ms period.

Multiplexed address inputs permit the μPD4164 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

FEATURES

- High Memory Density
- Multiplexed Address Inputs
- Single +5V Supply
- On Chip Substrate Bias Generator
- Access Time: μPD4164-1 — 250 ns
  μPD4164-2 — 200 ns
  μPD4164-3 — 150 ns
- Read, Write Cycle Time: μPD4164-1 — 410 ns
  μPD4164-2 — 335 ns
  μPD4164-3 — 270 ns
- Low Power Dissipation: 250 mW (Active); 28 mW (Standby)
- Non-Latched Output is Three-State, TTL Compatible
- Read, Write, Read-Write; Read-Modify-Write, RAS Only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Input Capacitance
- 128 Refresh Cycles (A_0-A_6 Pins for Refresh Address)
- CAS Controlled Output Allows Hidden Refresh
- Available in Both Ceramic and Plastic 16 Pin Packages

PIN CONFIGURATION



PIN NAMES

A_0-A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature (Ceramic Package) . . . . . −55°C to +150°C
(Plastic Package) . . . . . −55°C to +125°C
Supply Voltages On Any Pin Except V_{CC} . . . . . −1 to +7 Volts ①
Supply Voltage V_{CC} . . . . . −0.5 to +7 Volts ①
Short Circuit Output Current . . . . . 50 mA
Power Dissipation . . . . . 1 Watt

Note: ① Relative to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0° to 70°C ① ; V_{CC} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Supply Voltage	V_{CC}		4.5	5.0	5.5	V	
	V_{SS}		0	0	0	V	
High Level Input Voltage, ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	V_{IHC}		2.4		5.5	V	All Voltages Referenced to V_{SS}
High Level Input Voltage, All Inputs Except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IH}		2.4		5.5	V	
Low Level Input Voltage, All Inputs	V_{IL}		-2.0		0.8	V	
Operating Current Average Power Supply Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC} = t_{RC} (Min.)	I_{CC1}	μPD4164-1			45	mA	②
		μPD4164-2			50		
		μPD4164-3			60		
Standby Current Power Supply Standby Current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = Hi-Impedance)	I_{CC2}				5.0	mA	
Refresh Current Average Power Supply Current, Refresh Mode; $\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = t_{RC} (Min.)	I_{CC3}	μPD4164-1			35	mA	②
		μPD4164-2			40		
		μPD4164-3			45		
Page Mode Current Average Power Supply Current, Page Mode Operation $\overline{RAS}$ = V_{IL}; $\overline{CAS}$ Cycling t_{PC} = t_{PC} (Min.)	I_{CC4}	μPD4164-1			35	mA	②
		μPD4164-2			40		
		μPD4164-3			45		
Input Leakage Current Any Input V_{IN} = 0 to +5.5 Volts, All Other Pins Not Under Test = 0V	$I_{I(L)}$		−10		10	μA	
Output Leakage Current D_{OUT} is Disabled, V_{OUT} = 0 to +5.5 Volts	$I_{O(L)}$		−10		10	μA	
Output Levels High Level Output Voltage (I_{OUT} = 5 mA)	V_{OH}		2.4		V_{CC}	V	
Low Level Output Voltage (I_{OUT} = 4.2 mA)	V_{OL}		0		0.4	V	

Notes: ① T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met.
② I_{CC1}, I_{CC3} and I_{CC4} depend on output loading and cycle rates. Specified rates are obtained with the output open.

AC CHARACTERISTICS

T_a = 0° to +70°C ①; V_{CC} = +5V ± 10%; V_{SS} = 0V ③ ④

PARAMETER	SYMBOL	LIMITS μPD4164-1 MIN	μPD4164-1 MAX	μPD4164-2 MIN	μPD4164-2 MAX	μPD4164-3 MIN	μPD4164-3 MAX	UNIT	TEST CONDITIONS
Random Read or Write Cycle Time	t_{RC}	410		335		270		ns	⑤
Read Write Cycle Time	t_{RWC}	465		335		270		ns	⑤
Page Mode Cycle Time	t_{PC}	275		225		170		ns	
Access Time from $\overline{RAS}$	t_{RAC}		250		200		150	ns	⑥ ⑧
Access Time from $\overline{CAS}$	t_{CAC}		165		135		100	ns	⑦ ⑧
Output Buffer Turn-Off Delay	t_{OFF}	0	60	0	50	0	40	ns	⑨
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	④
$\overline{RAS}$ Precharge Time	t_{RP}	150		120		100		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	250	10,000	200	10,000	150	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	165		135		100		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	165	10,000	135	10,000	100	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	250		200		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	35	85	30	65	25	50	ns	⑩
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0		0		0		ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	35		30		25		ns	
$\overline{CAS}$ Precharge Time (For Page Mode Cycle Only)	t_{CP}	100		80		60		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	0		0		0		ns	
Row Address Set-Up Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	25		20		15		ns	
Column Address Set-Up Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	75		55		45		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	160		120		95		ns	
Read Command Set-Up Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	30		25		20		ns	⑬
Read Command Hold Time	t_{RCH}	0		0		0		ns	⑬
Write Command Hold Time	t_{WCH}	75		55		45		ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	160		120		95		ns	
Write Command Pulse Width	t_{WP}	75		55		45		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	100		55		45		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	100		55		45		ns	
Data-In Set-Up Time	t_{DS}	0		0		0		ns	⑪
Data-In Hold Time	t_{DH}	75		55		45		ns	⑪
Data-In Hold Time Referenced to $\overline{RAS}$	t_{DHR}	160		120		95		ns	
Refresh Period	t_{REF}		2		2		2	ms	
$\overline{WRITE}$ Command Set-Up Time	t_{WCS}	−20		−20		−20		ns	⑫
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	115		80		60		ns	⑫
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	200		145		110		ns	⑫

Notes:
① T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.

② An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

③ AC measurements assume t_T = 5 ns.

④ V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

⑤ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle times at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured.

⑥ Assumes that $t_{RCS} \leq t_{RCD}$ (max). If t_{RCS} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

⑦ Assumes that $t_{RCD} \geq t_{RCD}$ (max).

⑧ Measured with a load equivalent to 2 TTL loads and 100 pF.

⑨ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

⑩ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

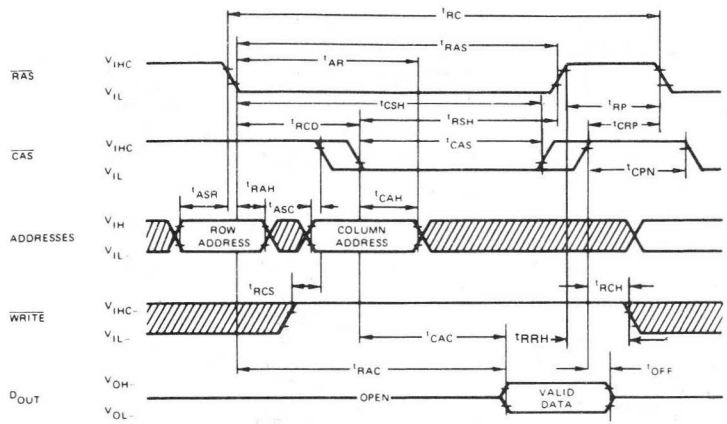
⑪ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

⑫ t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

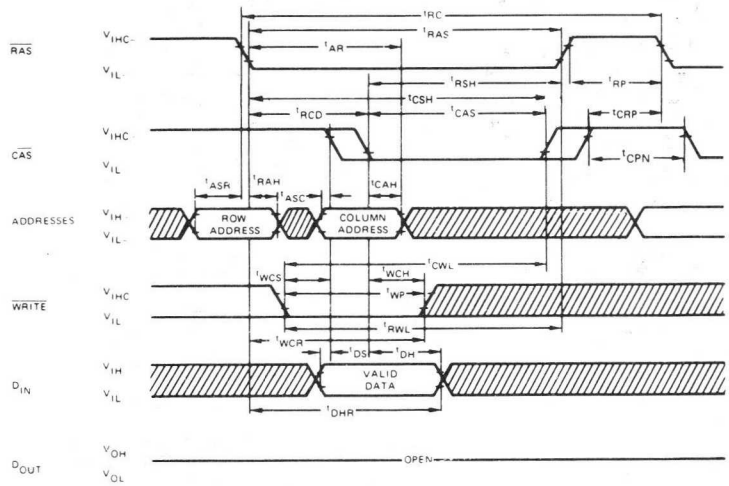
⑬ Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

TIMING WAVEFORMS

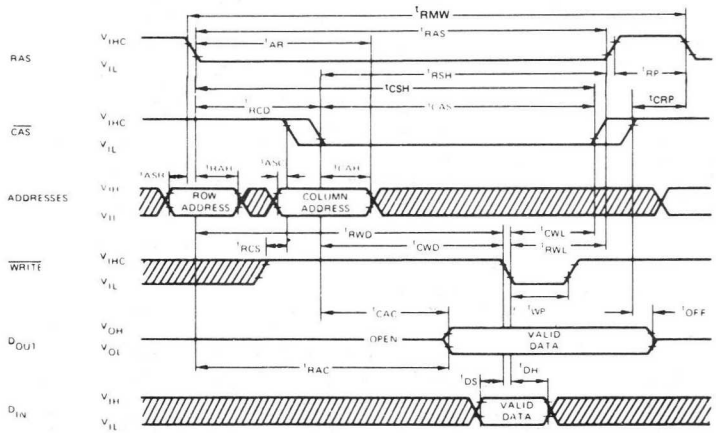
READ CYCLE



WRITE CYCLE (EARLY WRITE)

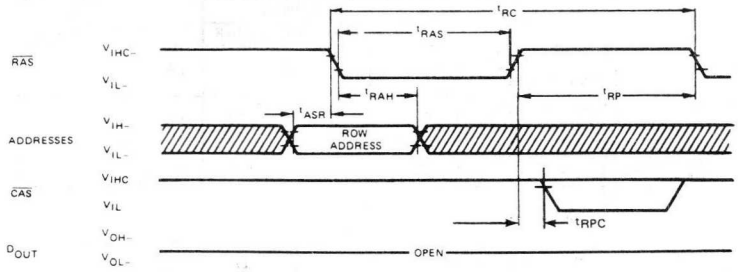


READ-WRITE/READ-MODIFY-WRITE CYCLE

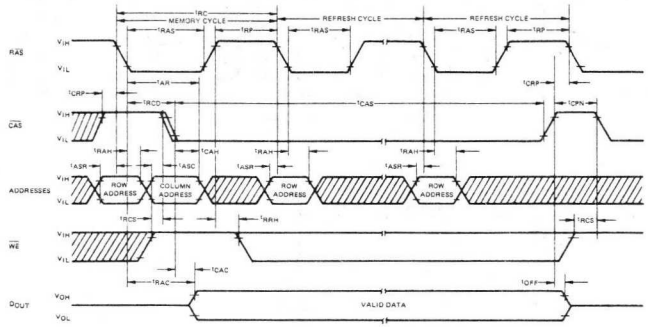


TIMING WAVEFORMS
(CONT.)

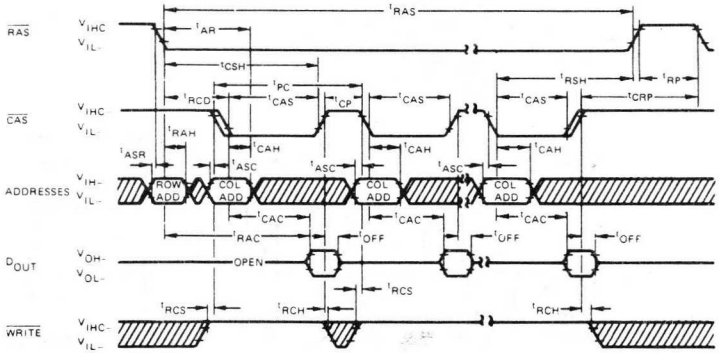
"RAS-ONLY" REFRESH CYCLE



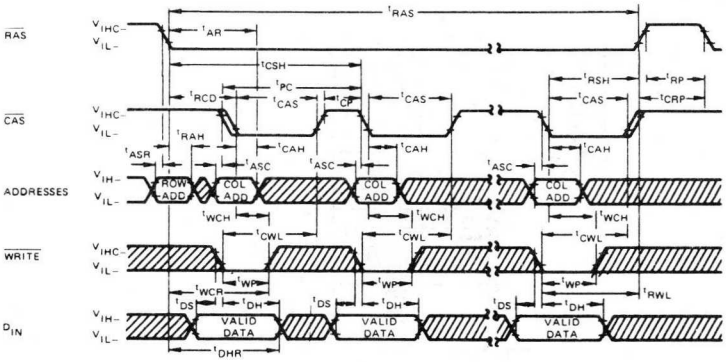
HIDDEN REFRESH CYCLE



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

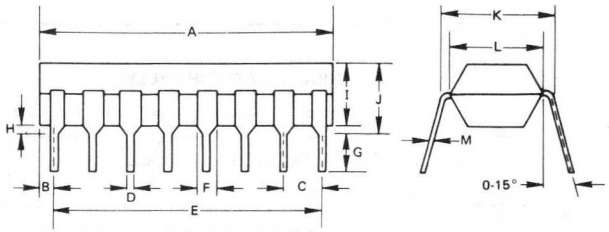


CAPACITANCE

$T_a = 0°$ to $+70°C$; $V_{CC} = +5V \pm 10\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_7), D_{IN}	C_{I1}		5	6	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}			10	pF	
Output Capacitance (D_{OUT})	C_O			7	pF	

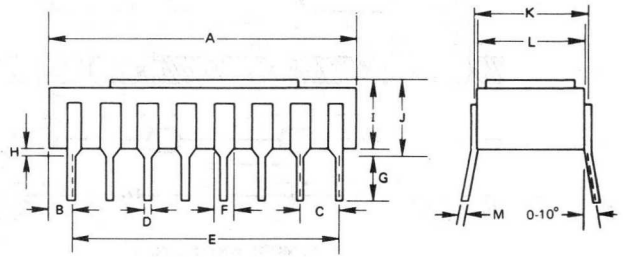
PACKAGE OUTLINES μPD4164C



Plastic

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

μPD4164D



Ceramic

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.6	0.30
L	7.3	0.29
M	0.27	0.01

4096 × 1 STATIC NMOS RAM

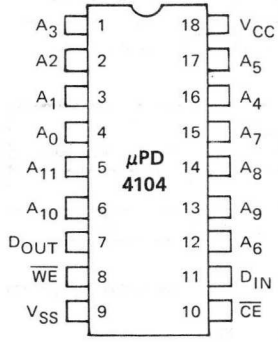
DESCRIPTION

The μPD4104 is a high performance 4K static RAM. Organized as 4096 x 1, it uses a combination of static storage cells with dynamic input/output circuitry to achieve high speed and low power in the same device. Utilizing NMOS technology, the μPD4104 is fully TTL compatible and operates with a single +5V ± 10% supply.

FEATURES

- Fast Access Time – 200 ns (μPD4104-2)
- Very Low Stand-By Power – 28 mW Max.
- Low V_{CC} Data Retention Mode to +3 Volts.
- Single +5V ±10% Supply.
- Fully TTL Compatible.
- Available in 18 Pin Plastic and Ceramic Dual-in-Line Packages.
- 3 Performance Ranges:

	ACCESS TIME	R/W CYCLE	SUPPLY CURRENT		
			ACTIVE	STANDBY	LOW V_{CC}
μPD4104	300 ns	460 ns	21 mA	5 mA	5 mA
μPD4104-1	250 ns	385 ns	21 mA	5 mA	3,3 mA
μPD4104-2	200 ns	310 ns	25 mA	5 mA	3,3 mA

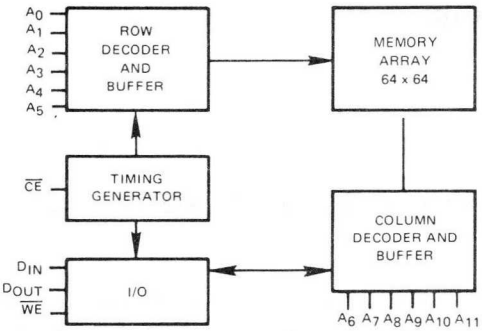


PIN NAMES

A_0-A_{11}	Address Inputs
$\overline{CE}$	Chip Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{SS}	Ground
V_{CC}	Power (+5V)
$\overline{WE}$	Write Enable

Rev/2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−1 to +7 Volts ①
Power Dissipation	1 Watt
Short Circuit Output Current	50 mA

Note: ① With respect to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS ① ⑥

T_a = 0°C to +70°C, V_{CC} = +5V ± 10%

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Supply Voltage		V_{CC}	4.5	5.0	5.5	V	①
Logic "1" Voltage All Inputs		V_{IH}	2.2	−3	7.0	V	
Logic "0" Voltage All Inputs		V_{IL}	−1.0		0.8	V	
Average V_{CC} Power Supply Current	μPD4104	I_{CC1}			21	mA	②
	μPD4104-1	I_{CC1}			21	mA	
	μPD4104-2	I_{CC1}			25	mA	
Standby V_{CC} Power Supply Current		I_{CC2}			5	mA	③
Input Leakage Current (Any Input)		I_{IL}	−10		10	μA	④
Output Leakage Current		I_{OL}	−10		10	μA	③ ⑤
Output Logic "1" Voltage I_{OUT} −500 μA		V_{OH}	2.4			V	
Output Logic "0" Voltage I_{OUT} 5mA		V_{OL}			0.4	V	

CAPACITANCE ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	6	pF	⑦
Output Capacitance	C_{OUT}		6	7	pF	⑦

Notes: ① All voltages referenced to V_{SS}

② I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} may be calculated by

$$I_{CC1}\ |ma| = (5t_p + 13\,(t_C - t_p) + 3420)\quad t_C$$

where t_p and t_C are expressed in nanoseconds. Equation is referenced to the **−2 device,** other devices derate to the same curve.

③ Output is disabled (open circuit), $\overline{CE}$ is at logic 1.

④ All device pins at 0 volts except pin under test at 0. V_{IN} = 5.5 volts.

⑤ 0V ≤ V_{OUT} ≤ +5.5V.

⑥ During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2 ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.

⑦ Effective capacitance calculated from the equation $C = \frac{\Delta t}{\Delta V}$ with ΔV equal to 3V and V_{CC} nominal.

AC CHARACTERISTICS ② ⑦

T_a = 0°C to +70°C, V_{CC} = +5V ± 10% ①

PARAMETER	SYMBOL	LIMITS 4104 MIN	4104 MAX	4104-1 MIN	4104-1 MAX	4104-2 MIN	4104-2 MAX	UNIT	TEST CONDITIONS
Read or Write Cycle Time	t_C	460		385		310		ns	⑧
Random Access	t_{AC}		300		250		200	ns	③
Chip Enable Pulse Width	t_{CE}	300	10,000	250	10,000	200	10,000	ns	
Chip Enable Precharge Time	t_P	150		125		100		ns	
Address Hold Time	t_{AH}	165		135		110		ns	
Address Set-Up Time	t_{AS}	0		0		0		ns	
Output Buffer Turn-Off Delay	t_{OFF}	0	75	0	65	0	50	ns	⑨
Read Command Set-Up Time	t_{RS}	0		0		0		ns	④
Write Enable Set-Up Time	t_{WS}	−20		−20		−20		ns	④
Data Input Hold Time Referenced to $\overline{WE}$	t_{DIH}	25		25		25		ns	
Write Enabled Pulse Width	t_{WW}	90		75		60		ns	
Modify Time	t_{MOD}	0	10,000	0	10,000	0	10,000	ns	⑤
$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	t_{WPL}	105		85		70		ns	⑥
Data Input Set-Up Time	t_{DS}	0		0		0		ns	
Write Enable Hold Time	t_{WH}	225		185		150		ns	
Transition Time	t_T	5	50	5	50	5	50	ns	
Read-Modify-Write Cycle Time	t_{RMW}	565		470		380		ns	⑩

Notes: ① All voltages referenced to V_{SS}

② During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2 ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.

③ Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.

④ If $\overline{WE}$ follows $\overline{CE}$ by more than t_{WS} then data out may not remain open circuited.

⑤ Determined by user. Total cycle time cannot exceed t_{CE} max.

⑥ Data-in set-up time is referenced to the later of the two falling clock edges $\overline{CE}$ or $\overline{WE}$.

⑦ AC measurements assume t_T = 5 ns. Timing points are taken as V_{IL} = 0.8V and V_{IH} = 2.2V on the inputs and V_{OL} = 0.4V and V_{OH} = 2.4V on the output waveform.

⑧ $t_C = t_{CE} + t_P + 2\,t_T$.

⑨ The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.

⑩ $t_{RMW} = t_{AC} + t_{WPL} + t_P + 3\,t_T + t_{MOD}$.

STANDBY CHARACTERISTICS

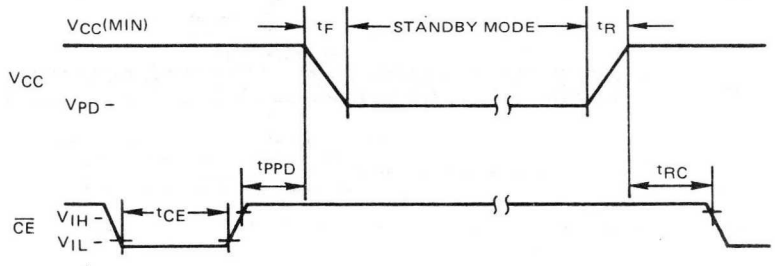
T_a = 0°C to +70°C

PARAMETER	SYMBOL	LIMITS 4104 MIN	4104 MAX	4104-1 MIN	4104-1 MAX	4104-2 MIN	4104-2 MAX	UNIT	TEST CONDITIONS
V_{CC} In Standby	V_{PD}	3.0		3.0		3.0		V	
Standby Current	I_{PD}		5.0		3.3		3.3	mA	①
Power Supply Fall Time	T_F	100		100		100		μs	
Power Supply Rise Time	T_R	100		100		100		μs	
Chip Enable Pulse $\overline{CE}$ Width	T_{CE}	300		250		200		μs	
Chip Enable Precharge to Power Down Time	T_{PPD}	150		125		100		ns	
"I" Level $\overline{CE}$ Min Level	V_{IH}	2.2		2.2		2.2		V	
Standby Recovery Time	T_{RC}	500		500		500		μs	

Note: ① Maximum value for V_{PD} minimum value (= 3 V).

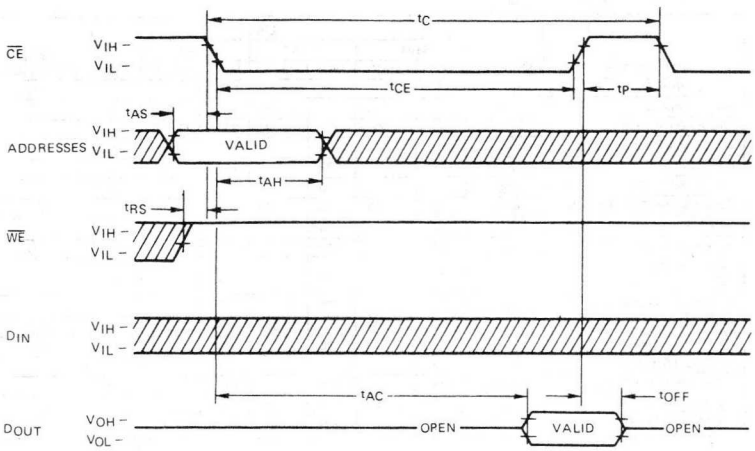
TIMING WAVEFORMS

POWER DOWN

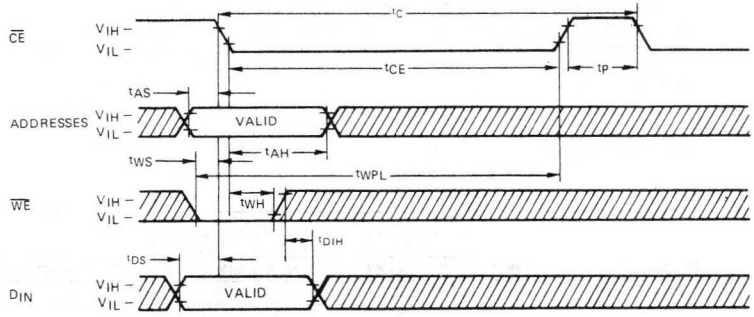


TIMING WAVEFORMS (CONT.)

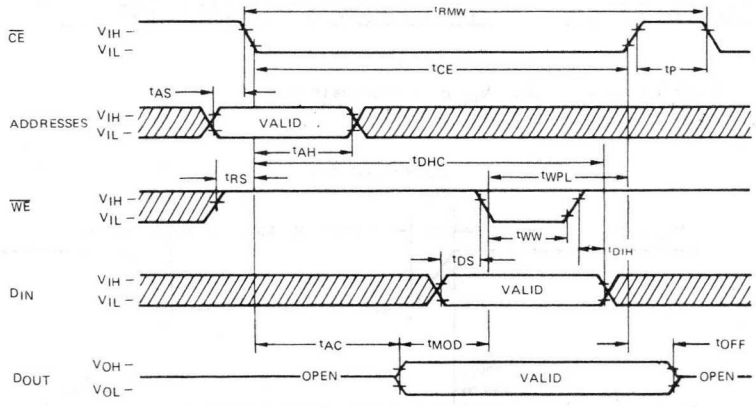
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



OPERATIONAL DESCRIPTION

READ CYCLE

The selection of one of the possible 4096 bits is made by virtue of the 12 address bits presented at the inputs. These are latched into the chip by the negative going edge of chip enable ($\overline{CE}$). If the write enable ($\overline{WE}$) input is held at a high level (V_{IH}) while the $\overline{CE}$ input is clocked to a low level (V_{IL}), a read operation will be performed. At the access time (t_{AC}), valid data will appear at the output. Since the output is unlatched by a positive transition of $\overline{CE}$, it will be in the high impedance state from the previous cycle until the access time. It will go to the high impedance state again at the end of the current cycle when $\overline{CE}$ goes high.

The address lines may be set up for the next cycle any time after the address hold time has been satisfied for the current cycle.

WRITE CYCLE

Data to be written into a selected cell is latched into the chip by the later negative transition of $\overline{CE}$ or $\overline{WE}$. If $\overline{WE}$ is brought low before $\overline{CE}$, the cycle is an "Early Write" cycle, and data will be latched by $\overline{CE}$. If $\overline{CE}$ is brought low before $\overline{WE}$, as in a Read-Modify-Write cycle, then data will be latched by $\overline{WE}$.

If the cycle is an "Early Write" cycle, the output will remain in the high impedance state. For a Read-Modify-Write cycle; the output will be active for the Modify and Write portions of the memory cycle until $\overline{CE}$ goes high. If $\overline{WE}$ is brought low after $\overline{CE}$ but before the access time, the state of the output will be undefined. The desired data will be written into the cell if data-in is valid on the leading edge of $\overline{WE}$, t_{DIH} is satisfied, and $\overline{WE}$ occurs prior to $\overline{CE}$ going high by at least the minimum lead time (t_{WPL}).

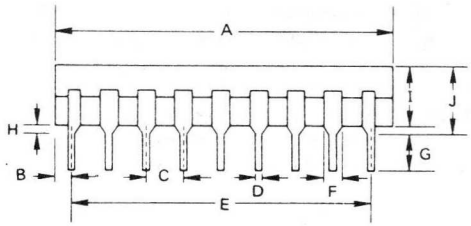
READ-MODIFY-WRITE

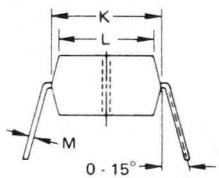
Read and Write cycles can be combined to allow reading of a selected location and then modifying that data within the same memory cycle. Data is read at the access time and modified during a period defined by the user. New data is written between $\overline{WE}$ low and the positive transition of $\overline{CE}$. Data out will remain valid until the rising edge of $\overline{CE}$. A minimum R-M-W cycle time can be calculated by $t_{RMW} = t_{AC} + t_{MOD} + t_{WPL} + t_P + 3\,t_T$; where t_{RMW} is the cycle time, t_{AC} is the access time, t_{MOD} is the user defined modify time, t_{WPL} is the $\overline{WE}$ to $\overline{CE}$ lead time, t_P is the $\overline{CE}$ high time, and t_T is one transition time.

POWER DOWN MODE

In power down, data may be retained indefinitely by maintaining V_{CC} at +3V. However, prior to V_{CC} going below V_{CC} minimum ($\leqslant$4.5V) $\overline{CE}$ must be taken high (V_{IH} = 2.2V) and held for a minimum time period t_{PPD} and maintained at V_{IH} for the entire standby period. After power is returned to V_{CC} min or above, $\overline{CE}$ must be held high for a minimum of t_{RC} in order that the device may operate properly. See power down waveforms herein. Any active cycle in progress prior to power down must be completed so that t_{CE} min is not violated.

PACKAGE OUTLINES
μPD4104C

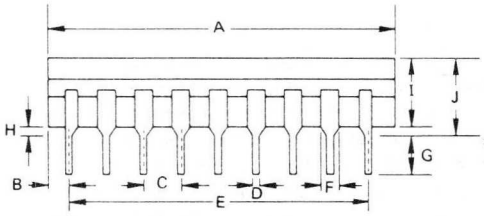


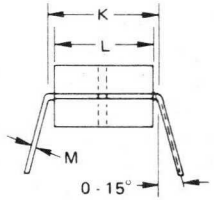


Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPD4104D





Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

NEC
μPD2114L
μPD2114L-1
μPD2114L-2
μPD2114L-3
μPD2114L-5

4096 BIT (1024 × 4 BITS) STATIC RAM

DESCRIPTION

The NEC μPD2114L is a 4096 bit static Random Access Memory organized as 1024 words by 4 bits using N-channel Silicon-gate MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding. It therefore requires no clocks or refreshing to operate and simplifies system design. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

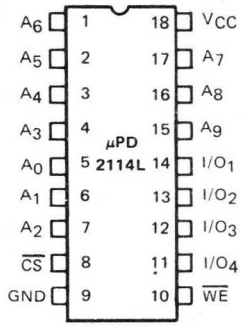
The μPD2114L is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The μPD2114L is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-Tied.

FEATURES

- Access Time: Selection from 150-450 ns
- Single +5 Volt Supply
- Directly TTL Compatible – All Inputs and Outputs
- Completely Static – No Clock or Timing Strobe Required
- Low Operating Power – Typically 0.06 mW/Bit
- Identical Cycle and Access Times
- Common Data Input and Output using Three-State Output
- High Density 18-pin Plastic and Ceramic Packages
- Replacement for 2114L and Equivalent Devices

PIN CONFIGURATION

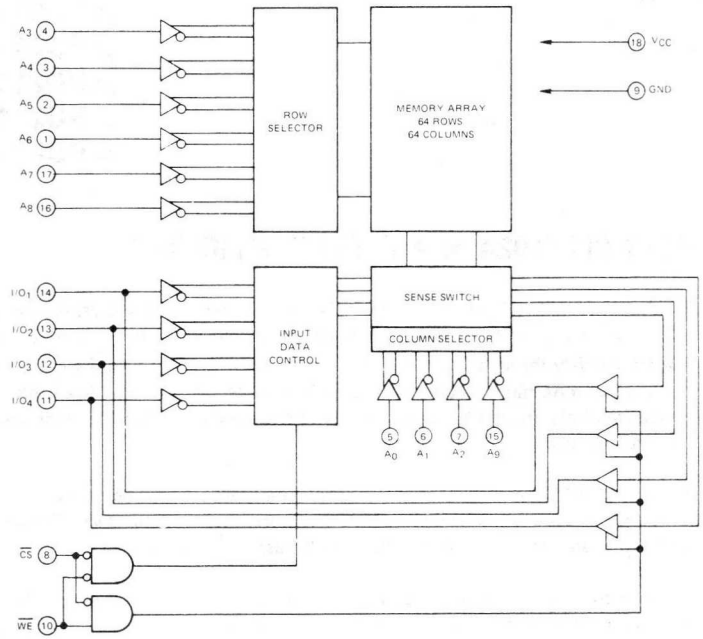


PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

Rev/1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +80°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin	-0.5 to 7 Volts 1

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 10% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			10	μA	V_{IN} = 0 to 5.5V
I/O Leakage Current	I_{LO}			10	μA	$\overline{CS}$ = 2V, $V_{I/O}$ = 0.4V to V_{CC}
Power Supply Current	I_{CC1}			65	mA	V_{IN} = 5.5V, $I_{I/O}$ = 0 mA, T_a = 25°C
Power Supply Current	I_{CC2}			70	mA	V_{IN} = 5.5V, $I_{I/O}$ = 0 mA, T_a = 0°C
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Current	I_{OL}	3.2			mA	V_{OL} = 0.4V
Output High Current	I_{OH}			-1.0	mA	V_{OH} = 2.4V, V_{CC} = 4.75V
						V_{OH} = 2.2V, V_{CC} = 4.5V

CAPACITANCE

T_a = 25°C; f = 1.0 MHz

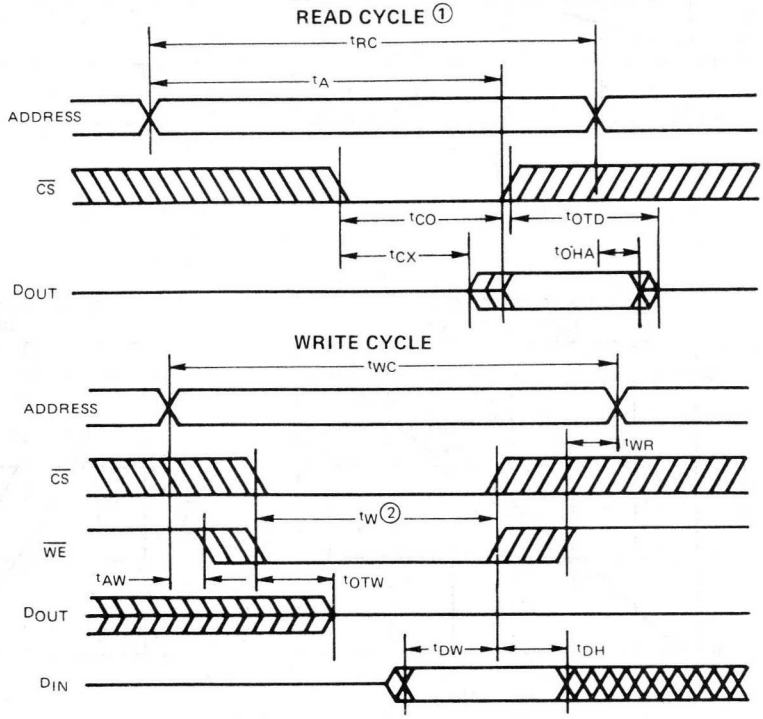
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input/Output Capacitance	$C_{I/O}$			8	pf	$V_{I/O}$ = 0V
Input Capacitance	C_{IN}			5	pf	V_{IN} = 0V

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS
		2114L		2114L-1		2114L-2		2114L-3		2114L-5			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE													
Read Cycle Time	t_{RC}	450		300		250		200		150		ns	$t_T = t_r = t_f$ = 10 ns
Access Time	t_A		450		300		250		200		150	ns	C_L = 100 pF
Chip Selection to Output Valid	t_{CO}		120		100		80		70		60	ns	Load = 1 TTL gate
Chip Selection to Output Active	t_{CX}	20		20		20		20		20		ns	Input Levels = 0.8 and 2.0V
Output 3-State from Deselection	t_{OTD}		100		80		70		60		50	ns	V_{ref} = 1.5V
Output Hold from Address Change	t_{OHA}	50		50		50		50		50		ns	
WRITE CYCLE													
Write Cycle Time	t_{WC}	450		300		250		200		150		ns	$t_T = t_r = t_f$ = 10 ns
Write Time	t_W	200		150		120		120		80		ns	C_L = 100 pF
Write Release Time	t_{WR}	0		0		0		0		0		ns	Load = 1 TTL gate
Output 3-State from Write	t_{OTW}		100		80		70		60		50	ns	Input Levels = 0.8 and 2.0V
Data to Write Time Overlap	t_{DW}	200		150		120		120		80		ns	V_{ref} = 1.5V
Data Hold from Write Time	t_{DH}	0		0		0		0		0		ns	
Address to Write Setup Time	t_{AW}	0		0		0		0		0		ns	

TIMING WAVEFORMS

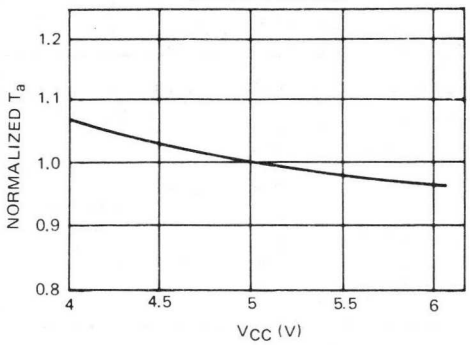


Notes: ① $\overline{WE}$ is high for Read Cycle

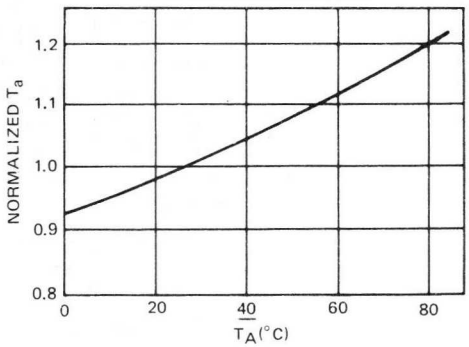
② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

TYPICAL OPERATING CHARACTERISTICS

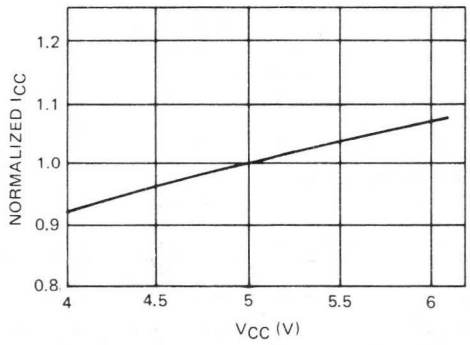
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



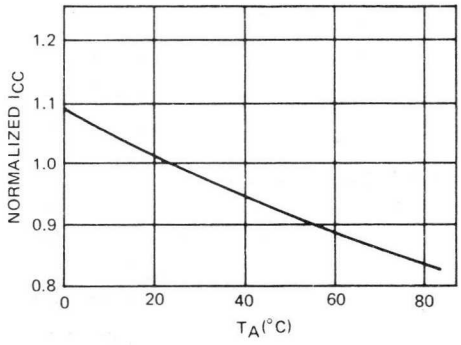
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



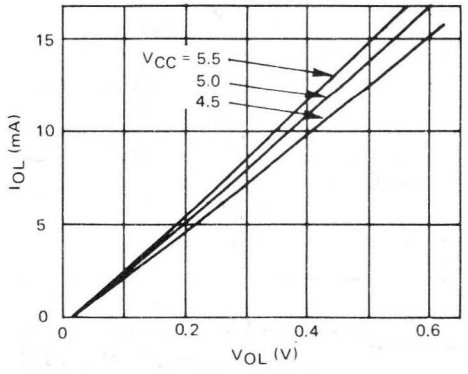
NORMALIZED POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



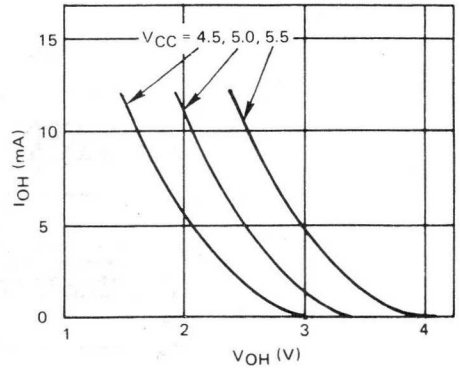
NORMALIZED POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



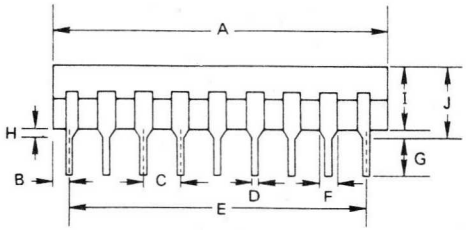
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE

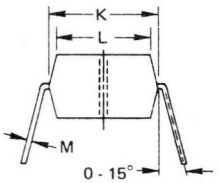


OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



PACKAGE OUTLINES
μPD2114LC

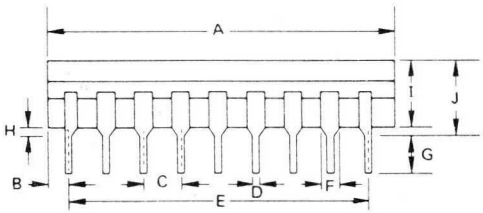


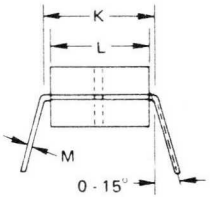


(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPD2114LD





(CERDIP)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

NOTES

4096 x 1 BIT STATIC RAM

The μPD2147 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit. Using a scaled NMOS technology, it incorporates an innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. The result is low standby power dissipation without the need for clocks, address setup and hold times. In addition, data rates are not reduced due to cycle times that are longer than access times.

$\overline{CS}$ controls the power down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the μPD2147 — the part automatically reduces its power requirements and remains in this lower power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

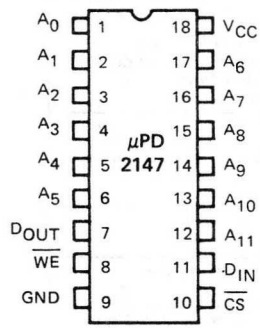
The μPD2147 is placed in an 18-pin ceramic package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out non-destructively and has the same polarity as the input data. A data input and a separate three-state output are used.

FEATURES

- Scaled NMOS Technology
- Completely Static Memory — No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Single +5V Supply
- Automatic Power-Down
- High Density 18-Pin Package
- Directly TTL Compatible — All Inputs and Outputs
- Separate Data Input and Output
- Three-State Output
- Available in a Standard 18-Pin Ceramic Package
- 2 Performance Ranges:

	MAX ACCESS TIME	SUPPLY CURRENT	
		ACTIVE	STANDBY
μPD2147-2	70 ns	160 mA	20 mA
μPD2147-3	55 ns	160 mA	20 mA
μPD2147-5	45 ns	160 mA	20 mA

PIN CONFIGURATION



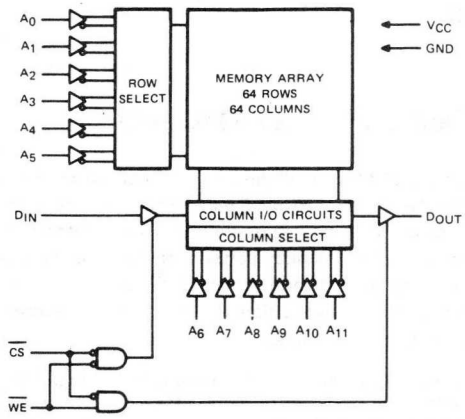
PIN NAMES

A_0-A_{11}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin . . . . . −3.5V to +7 Volts ①
DC Output Current . . . . . 20 mA
Power Dissipation . . . . . 1.2 W

Note: ① with respect to ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted. ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ②	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}		0.01	10	μA	V_{CC} = Max, V_{IN} = GND to V_{CC}
Output Leakage Current	$\lvert I_{LO} \rvert$		0.01	10	μA	$\overline{CS}$ = V_{IH}, V_{CC} = Max, V_{OUT} = GND to V_{CC}
Operating Current	I_{CC}		120	150	mA	T_a = 25°C; V_{CC} = Max, $\overline{CS}$ = V_{IL}, Outputs Open
				160	mA	T_a = 0°C; V_{CC} = Max, $\overline{CS}$ = V_{IL}, Outputs Open
Standby Current	I_{SB}		12	20	mA	V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}
Peak Power-On Current	I_{PO} ③		25	50	mA	V_{CC} = GND to V_{CC} = Min, $\overline{CS}$ = Lower of V_{CC} or V_{IH}Min
Input Low Voltage	V_{IL}	-3.0		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −4.0 mA
Output Short Circuit Current	I_{OS}	-150		+150	mA	V_{OUT} = GND to V_{CC}

Notes: ① The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
② Typical limits are V_{CC} = 5V, T_a = +25°C, and specified loading.
③ I_{CC} exceeds I_{SB} maximum during power on. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected: otherwise, power-on current approaches I_{CC} active.

CAPACITANCE

$T_a = 25°C$; f = 1.0 MHz ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			6	pF	V_{OUT} = 0V

Note: ① This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels . . . . . Gnd to 3.0 Volts
Input Rise and Fall Times . . . . . 5 ns
Input and Output Timing Reference Levels . . . . . 1.5 Volts
Output Load . . . . . See Figure 1

AC CHARACTERISTICS READ CYCLE

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$ unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD2147-5 MIN	LIMITS μPD2147-5 MAX	LIMITS μPD2147-3 MIN	LIMITS μPD2147-3 MAX	LIMITS μPD2147-2 MIN	LIMITS μPD2147-2 MAX	UNIT	TEST CONDITIONS
Read Cycle Time	t_{RC} ①	45		55		70		ns	
Address Access Time	t_{AA}		45		55		70	ns	
Chip Select Access Time	t_{ACS1}		45		55		70	ns	
Chip Select Access Time	t_{ACS2}		45		55		70	ns	
Output Hold From Address Change	t_{OH}	5		5		5		ns	
Chip Select to Output in Low Z	t_{CZ} ②	10		10		10		ns	③
Chip Deselection to Output in High Z	t_{HZ} ②	0	30	0	30	0	40	ns	④
Chip Selection to Power-Up Time	t_{PU}	0		0		0		ns	
Chip Selection to Power-Down Time	t_{PD}		20		20		30	ns	

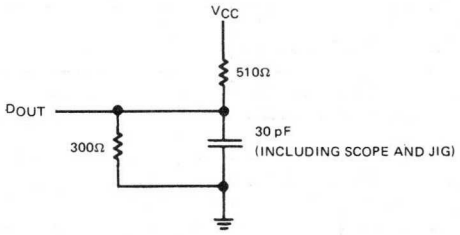
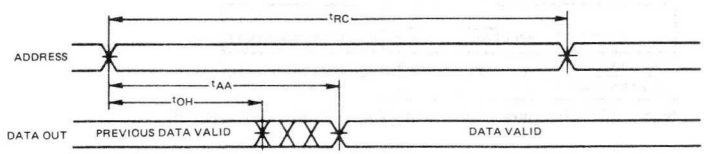


Figure 1

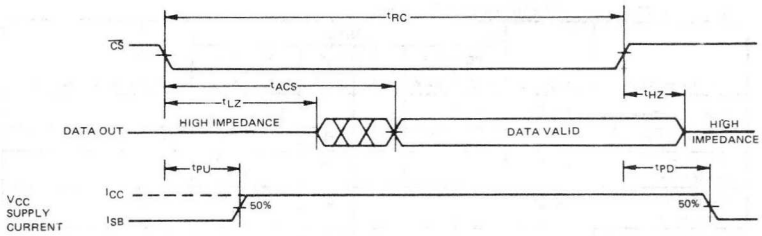
Notes: ① All Read Cycle timings are referenced from the last valid address to the first transitioning address.
② At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min. both for a given device and from device to device.
③ Transition is measured ±200 mV from steady state voltage with specified loading.
④ Transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with specified loading.

TIMING WAVEFORMS
READ CYCLE

READ CYCLE NO. 1 ⑤⑥



READ CYCLE NO. 2 ⑤⑦



AC CHARACTERISTICS
WRITE CYCLE

PARAMETER	SYMBOL	LIMITS μPD2147-5 MIN	μPD2147-5 MAX	μPD2147-3 MIN	μPD2147-3 MAX	μPD2147-2 MIN	μPD2147-2 MAX	UNIT	TEST CONDITIONS
Write Cycle Time ②	t_{WC}	45		55		70		ns	
Chip Select to End of Write	t_{CW}	45		45		55		ns	
Address Valid to End of Write	t_{AW}	45		45		55		ns	
Address Setup Time	t_{AS}	0		0		0		ns	
Write Pulse Width	t_{WP}	25		25		40		ns	
Write Recovery Time	t_{WR}	0		10		15		ns	
Data Valid to End of Write	t_{DW}	25		25		30		ns	
Data Hold Time	t_{DH}	10		10		10		ns	
Write Enabled to Output with Z	t_{WZ}	0	25	0	25	0	35	ns	③
Output Active From End of Write	t_{OW}	0		0		0		ns	④

Notes: ① All Read Cycle timings are referenced from the last valid address to the first transitioning address.

② At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min. both for a given device and from device to device.

③ Transition is measured ±200 mV from steady state voltage with specified loading.

④ Transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with specified loading.

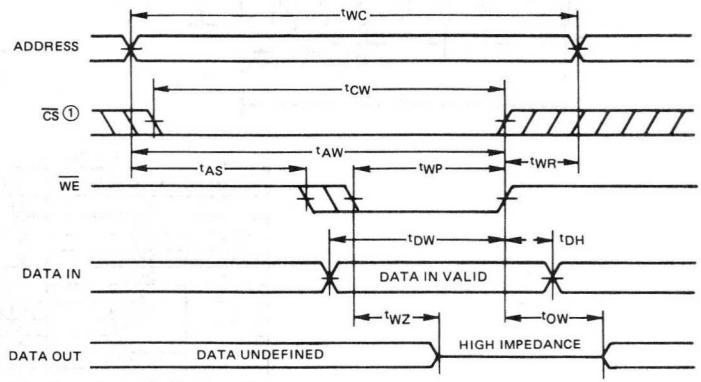
⑤ WE is high for Read Cycles.

⑥ Device is continuously selected, $\overline{CS} = V_{IL}$.

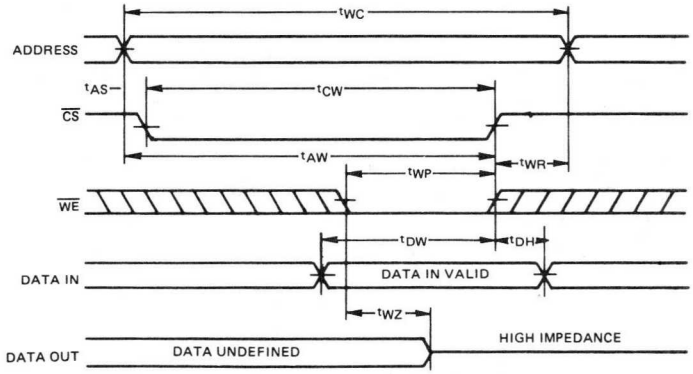
⑦ Addresses valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORMS
WRITE CYCLE

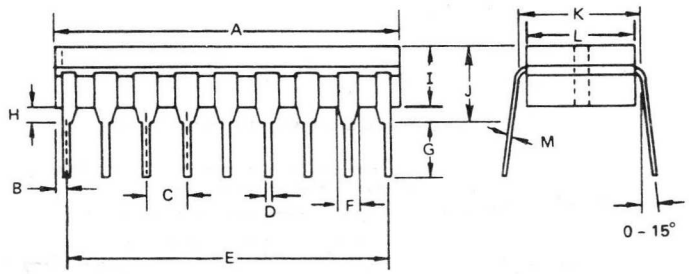
WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) ⑤



WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) ⑤



Notes: ① If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
② All Write Cycle timings are referenced from the last valid address to the first transitioning address.
③ Transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with specified loading.
④ Transition is measured ±200 mW from steady state voltage with specified loading.
⑤ $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.



PACKAGE OUTLINE
μPD2147D

Ceramic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

NEC
μPD2149
μPD2149-1
μPD2149-2
PRELIMINARY

4096 (1024x4) BIT STATIC RAM

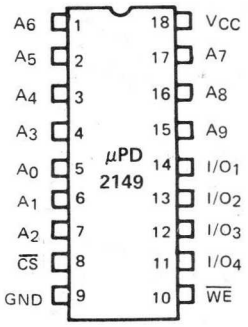
DESCRIPTION

The μPD2149 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits. Using a scaled NMOS technology, it incorporates an innovative design approach which provides the ease-of-use features associated with non-clocked static memories.

The μPD2149 is encapsulated in an 18-pin ceramic package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out non-destructively and has the same polarity as the input data.

FEATURES

- Completely Static Memory — No Clock or Timing Strobe Required
- Equal Access and Cycle Times, Faster Chip Select Access
- Single +5V Supply
- High Density 18-Pin Package
- Directly TTL Compatible — All Inputs and Outputs
- Common Input and Output
- Three-State Output
- Access Time: 35-55 ns MAX (From Address)
  15-25 ns MAX (From Chip Select)
- Power Dissipation: 180 mA MAX



PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O
H	X	Not Selected	High Z
L	L	Write	D_{IN}
L	H	Read	D_{OUT}

CAPACITANCE

$T_a = 25°C$; f = 1.0 MHz ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			7	pF	V_{OUT} = 0V

AC TEST CONDITIONS

Note: ① This parameter is sampled and not 100% tested.

Input Pulse Levels . . . . . Gnd to 3.0V
Input Rise and Fall Times . . . . . 5 ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

AC CHARACTERISTICS READ CYCLE ①

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$, unless otherwise noted.

PARAMETER	SYMBOL	2149-2 MIN	2149-2 MAX	2149-1 MIN	2149-1 MAX	2149 MIN	2149 MAX	UNIT	TEST CONDITIONS
Read Cycle Time	T_{RC}	35		45		55		ns	
Access Time	T_A		35		45		55	ns	
Chip Selection to Output Valid	T_{CO}		15		20		25	ns	
Chip Selection to Output Active	T_{CX}	0		0		0		ns	
Output 3-State From Deselection	T_{OTD}		10		15		20	ns	②
Output Hold From Address Change	T_{OH}	0		0		0		ns	

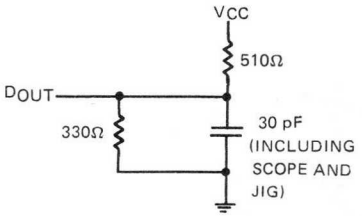


Figure 1

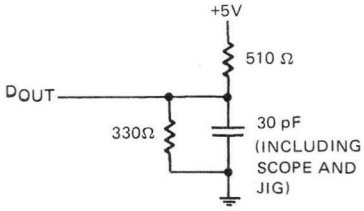
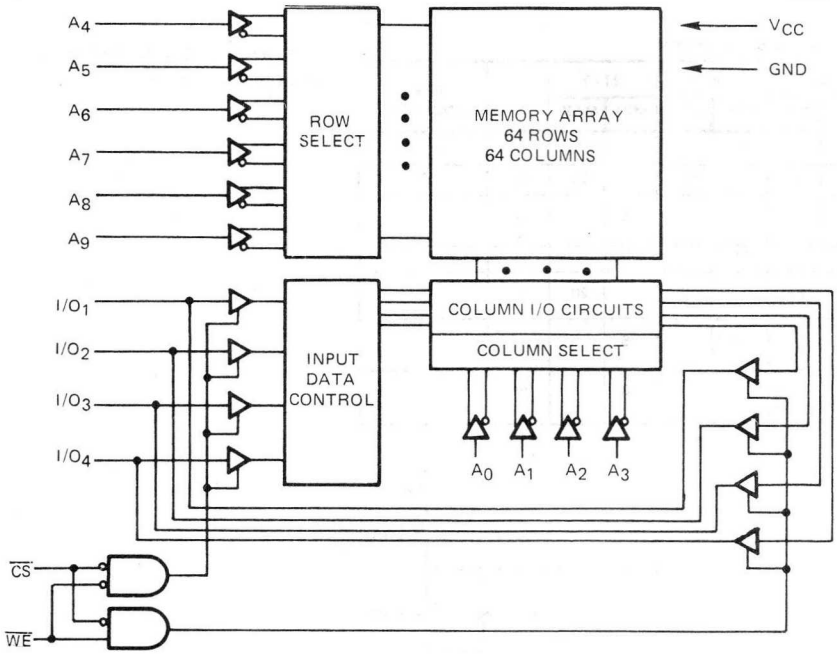


Figure 2

Notes: ① $\overline{WE}$ is high for read cycle.
② Transition is measured ±500 MV from steady state with load of Figure 2. This parameter is sampled and not 100% tested.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +85°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5V to +7V ①
DC Output Current	20 mA
Power Dissipation	1.2W

Note: ① with respect to ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted.

PARAMETER	SYMBOL	MIN	MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}	−10	+10	μA	V_{IN} = GND to V_{CC}
Ouput Leakage Current	I_{LO}	−50	+50	μA	CS = V_{IH} V_{OUT} = GND to 4.5V
Power Supply Current	I_{CC}		180	MA	V_{IN} = V_{CC}, I/O = open
Input Low Voltage	V_{IL}	−0.5	0.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC}	V	
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8 MA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −4 MA
Output Short Circuit Current	I_{OS}	TBD	TBD	MA	V_{OUT} = GND to V_{CC}

Note: The operating temperature range is guaranteed with transverse air flow exceeding 400 feet per minute.

AC CHARACTERISTICS
WRITE CYCLE

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted.

PARAMETER	SYMBOL	2149-2		2149-1		2149		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
Write Cycle Time	T_{WC}	35		45		55		ns	
Write Time	T_W		30		40		50	ns	①
Write Release Time	T_{WR}	5		5		5		ns	
Data to Write	T_{DW}	20		25		30		ns	
Output 3-State From Write	T_{OTW}		10		15		20	ns	②
Data Hold From Write Time	T_{DH}	5		5		5		ns	
Address to Write Setup Time	T_{AW}	0		0		0		ns	

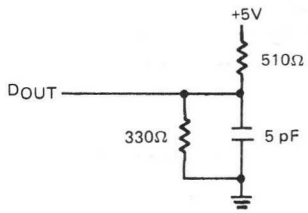


Figure 3

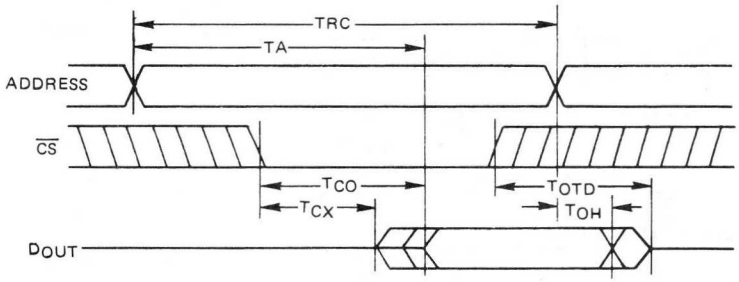
Notes: ① T_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

② Transition is measured +500 MV from steady state with load of Figure 3. This parameter is sampled and not 100% tested.

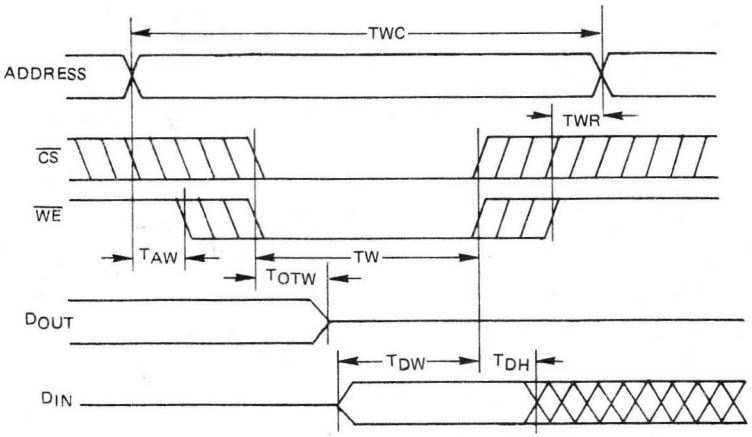
③ $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.

TIMING WAVEFORMS

READ CYCLE ① ②

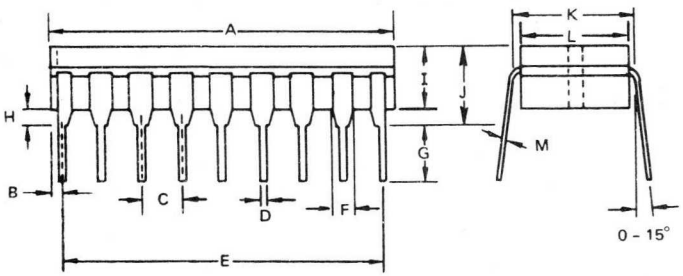


WRITE CYCLE ②



Notes: ① $\overline{WE}$ is high for read cycle.
② $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.

PACKAGE OUTLINE μPD2149D



Ceramic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

NOTES

8K BIT STATIC RAM

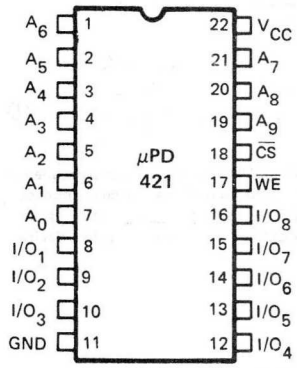
DESCRIPTION

The NEC μPD421 is a very high speed 8192 bit static Random Access Memory organized as 1024 words by 8 bits. Features include a power down mode controlled by the chip select input for an 80% power saving.

FEATURES

- 1024 x 8-bit Organization
- Very Fast Access Time: 150/200/250/300/450 ns
- Single +5V Power Supply
- Low Power Standby Mode
- N-Channel Silicon Gate Process
- Fully TTL Compatible
- 6-Device Static Cell
- Three State Common I/O
- Compatible with 8108 and Equivalent Devices
- Available in 22 Pin Ceramic Dual-in-Line Package

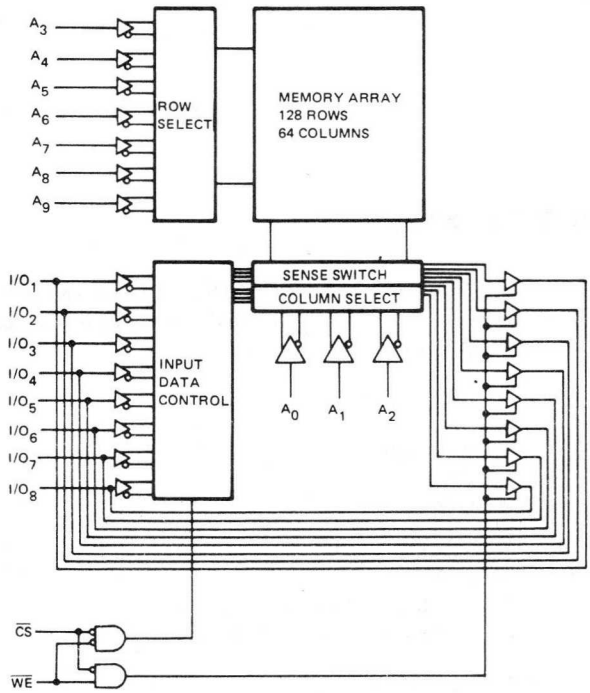
PIN CONFIGURATION



PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_8	Data Input Output
V_{CC}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin . . . . . −0.5 to +7 Volts ①

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Load Current (All Inputs Pins)	I_{LI}			10	μA	V_{IN} = 0 to +5.5V
I/O Leakage Current	I_{LO}			50	μA	
Operating Current	I_{CC}			120	mA	V_{CC} = Max; $\overline{CS}$ = V_{IL}; Outputs Open
Stand-by Current	I_{SB}			20	mA	V_{CC} = Min. to Max. $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -1 mA

CAPACITANCE $T_a = 25°C; f = 1.0$ MHz

PARAMETER	SYMBOL	LIMITS		UNIT	TEST CONDITIONS
		MIN	MAX		
Input/Output Capacitance	$C_{I/O}$		7	pF	$V_{I/O} = 0V$
Input Capitance	C_{IN}		5	pF	$V_{IN} = 0V$

AC CHARACTERISTICS

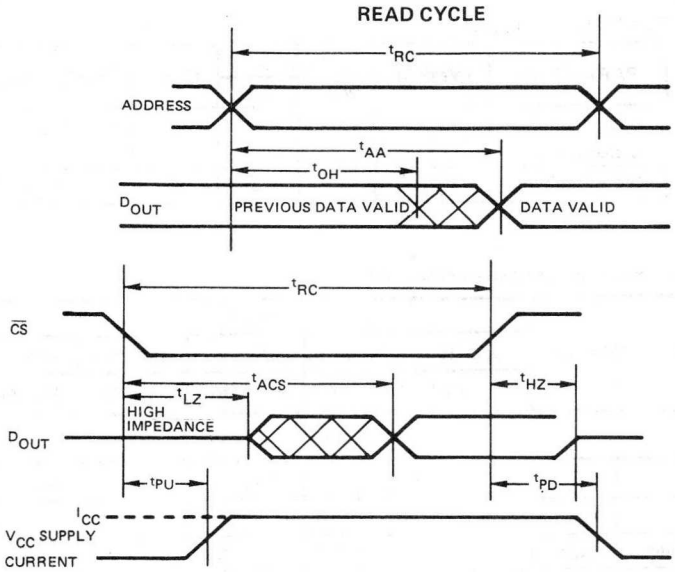
$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$, unless otherwise specified

PARAMETER	SYMBOL	LIMITS										UNIT
		μPD421		μPD421-1		μPD421-2		μPD421-3		μPD421-5		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE												
Read Cycle Time	t_{RC}	450		300		250		200		150		ns
Address Access Time	t_{AA}		450		300		250		200		150	ns
Chip Select Access Time	t_{ACS}		450		300		250		200		150	ns
Output Hold from Address Change	t_{OH}	10		10		10		10		10		ns
Chip Selection To Output in Low Z	t_{LZ}	10		10		10		10		10		ns
Chip Deselection to Output in High Z	t_{HZ}	0	100	0	80	0	70	0	60	0	50	ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		0		0		ns
Chip Deselection to Power Down Time	t_{PD}①		100		80		70		60		50	ns
WRITE CYCLE												
Write Cycle Time	t_{WC}	450		300		250		200		150		ns
Chip Selection to End of Write	t_{CW}	360		240		200		160		130		ns
Address Valid to End of Write	t_{AW}	360		240		200		160		130		ns
Address Setup Time	t_{AS}	10		10		10		10		10		ns
Write Pulse Width	t_{WP}	300		230		190		160		130		ns
Write Recovery Time	t_{WR}	10		10		10		10		10		ns
Data Valid to End of Write	t_{DW}	200		150		120		100		80		ns
Data Hold Time	t_{DH}	10		10		10		10		10		ns
Write Enabled to Output in High Z	t_{WZ}		100		80		70		60		50	ns
Output Active from End of Write	t_{OW}	10		10		10		10		10		ns

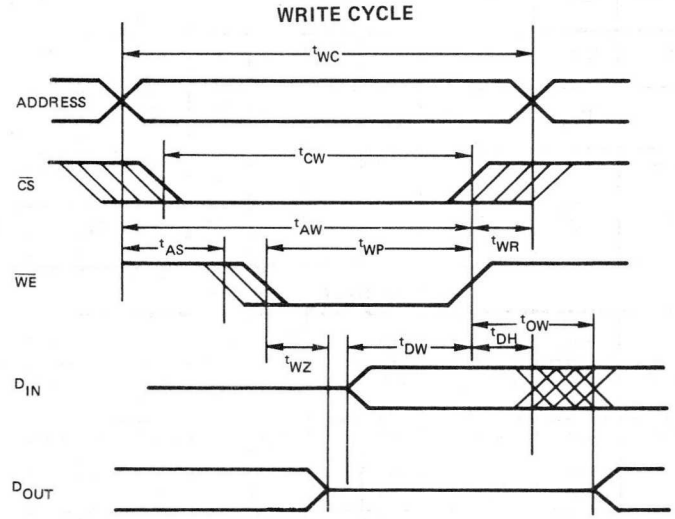
Note: ① I_{CC} ($t = t_{PD}$) = 1/2 I_{CC} Active.

TIMING WAVEFORMS

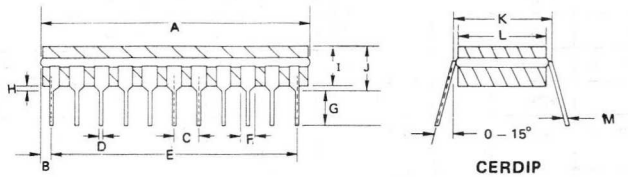
READ CYCLE



WRITE CYCLE



PACKAGE OUTLINE μPD421D



CERDIP

ITEM	MILLIMETERS	INCHES
A	27,43 Max.	1,079 Max.
B	1,27 Max.	0,05 Max.
C	2,54 ± 0,1	0,10
D	0,42 ± 0,1	0,016
E	25,4 ± 0,3	1,0
F	1,5 ± 0,2	0,059
G	3,5 ± 0,3	0,138
H	3,7 ± 0,3	0,145
I	4,2 Max.	0,165 Max.
J	5,08 Max.	0,200 Max.
K	10,16 ± 0,15	0,400
L	9,1 ± 0,2	0,358
M	0,25 ± 0,05	0,009

16,384 x 1 BIT STATIC MOS RANDOM ACCESS MEMORY

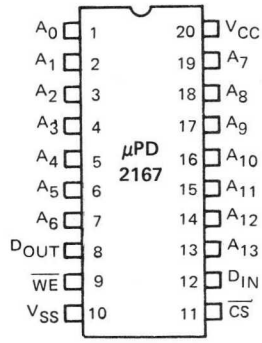
DESCRIPTION

The NEC μPD2167 is a 16,384 words by 1 bit Static MOS RAM. Fabricated with NEC's NMOS technology, it offers the user single power supply operation and fast access times in a standard 20 pin dual-in-line package. Its use of automatic power down circuitry minimizes system operating power requirements. Fully static circuitry throughout means the cycle time and access time are equal.

FEATURES

- 16,384 x 1 Organization
- Fully Static Memory — No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Single +5V Supply
- Automatic Power Down
- Directly TTL Compatible — All Inputs and Outputs
- Separate Data Input and Output
- Three-State Output
- Access Time: 55 ns Max.
- Power Dissipation: 160 mA Max. (Active)
  20 mA Max. (Standby)
- Available in a Standard 20 Pin Dual-in-line Package

PIN CONFIGURATION



PIN NAMES

$A_0 - A_{13}$	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

NOTES

1024 BIT (256x4) STATIC CMOS RAM

DESCRIPTION

The μPD5101L and μPD5101L-1 are very low power 1024 bit (256 words by 4 bits) static CMOS Random Access Memories. They meet the low power requirements of battery operated systems and can be used to ensure non-volatility of data in systems using battery backup power.

All inputs and outputs of the μPD5101L and μPD5101L-1 are TTL compatible. Two chip enables ($\overline{CE}_1$, CE_2) are provided, with the devices being selected when $\overline{CE}_1$ is low and CE_2 is high. The devices can be placed in standby mode, drawing 10 μA maximum, by driving $\overline{CE}_1$ high and inhibiting all address and control line transitions. The standby mode can also be selected unconditionally by driving CE_2 low.

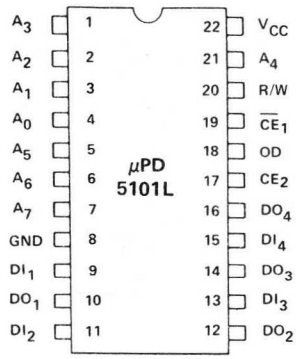
The μPD5101L and μPD5101L-1 have separate input and output lines. They can be used in common I/O bus systems through the use of the OD (Output Disable) pin and OR-tying the input/output pins. Output data is the same polarity as input data and is nondestructively read out. Read mode is selected by placing a high on the R/W pin. Either device is guaranteed to retain data with the power supply voltage as low as 2.0 volts. Normal operation requires a single +5 volt supply.

The μPD5101L and μPD5101L-1 are fabricated using NEC's silicon gate complementary MOS (CMOS) process.

FEATURES

- Directly TTL Compatible – All Inputs and Outputs
- Three-State Output
- Access Time – 650 ns (μPD5101L); 450 ns (μPD5101L-1)
- Single +5V Power Supply
- CE_2 Controls Unconditional Standby Mode
- Available in a 22-pin Dual-in-Line Package

PIN CONFIGURATION

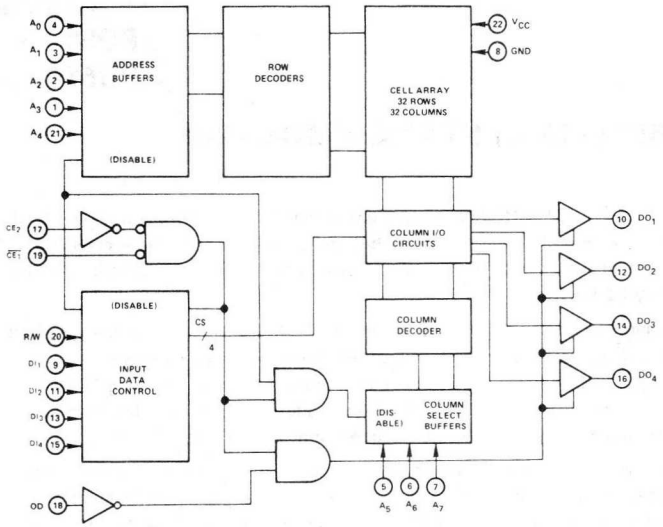


PIN NAMES

$DI_1 - DI_4$	Data Input
$A_0 - A_7$	Address Inputs
R/W	Read/Write Input
$\overline{CE}_1$, CE_2	Chip Enables
OD	Output Disable
$DO_1 - DO_4$	Data Output
V_{CC}	Power (+5V)

μPD5101L

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−40°C to +125°C
Voltage On Any Pin With Respect to Ground	−0.3 Volts to V_{CC} +0.3 Volts
Power Supply Voltage	−0.3 to +7.0 Volts

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP (1)	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Leakage	I_{LIH} (2)			1	μA	$V_{IN} = V_{CC}$
Input Low Leakage	I_{LIL} (2)			−1	μA	V_{IN} = 0V
Output High Leakage	I_{LOH} (2)			1	μA	$\overline{CE}_1$ = 2.2V, $V_{OUT} = V_{CC}$
Output Low Leakage	I_{LOL} (2)			−1	μA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 0.0V
Operating Current	I_{CC1}			22	mA	$V_{IN} = V_{CC}$ Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Operating Current	I_{CC2}			27	mA	V_{IN} = 2.2V Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Standby Current	I_{CCL} (2)			10	μA	V_{IN} = 0 to 5.25V $CE_2 \leq$ 0.2V
Input Low Voltage	V_{IL}	−0.3		0.65	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −1.0 mA
Output High Voltage	V_{OH2}	3.5			V	I_{OH} = −100 μA

Notes: (1) Typical values at T_a = 25°C and nominal supply voltage.

(2) Current through all inputs and outputs included in I_{CCL}.

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance (All Input Pins)	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0V

AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C; V_{CC} = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Read Cycle	t_{RC}	650			450			ns	Input pulse amplitude: 0,65 to 2,2 Volts
Access Time	t_A			650			450	ns	Input rise and fall times: 20 ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}			600			400	ns	Timing measurement reference level: 1,5 Volt
Chip Enable (CE_2) to Output	t_{CO2}			700			500	ns	Output load: I_{TTL}
Output Disable to Output	t_{OD}			350			250	ns	Gate and C_L = 100 pF
Data Output to High Z State	t_{DF}	0		150	0		130	ns	
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0			0			ns	
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0			0			ns	

WRITE CYCLE

T_a = 0°C to 70°C; V_{CC} = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Write Cycle	t_{WC}	650			450			ns	Input pulse amplitude: 0,65 to 2,2 Volts
Write Delay	t_{AW}	150			130			ns	
Chip Enable ($\overline{CE_1}$) to Write	t_{CW1}	550			350			ns	Input rise and fall times: 20 ns
Chip Enable (CE_2) to Write	t_{CW2}	550			350			ns	Timing measurement reference level: 1,5 Volt
Data Setup	t_{DW}	400			250			ns	Output load: I_{TTL}
Data Hold	t_{DH}	100			50			ns	Gate and C_L = 100 pF
Write Pulse	t_{WP}	400			250			ns	
Write Recovery	t_{WR}	50			50			ns	
Output Disable Setup	t_{DS}	150			130				

LOW V_{CC} DATA RETENTION CHARACTERISTICS

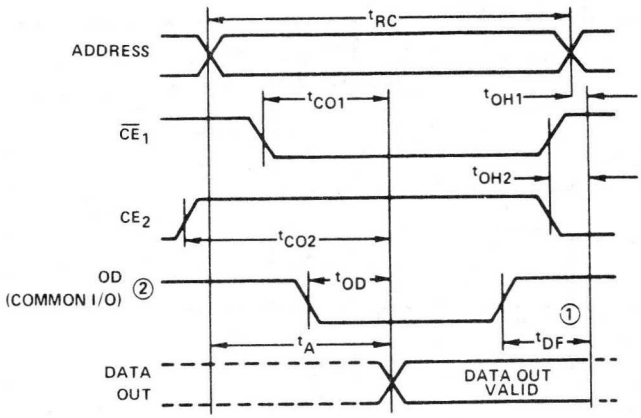
T_a = 0°C to 70°C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \geq +0.2V$
Data Retention Current	I_{CCDR}			+10	μA	V_{CCDR} = +2.0V $CE_2 \geq +0.2V$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_R	t_{RC}①			ns	

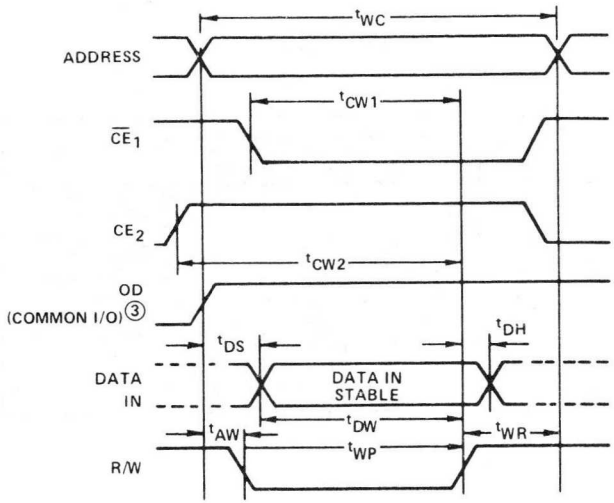
Note: ① t_{RC} = Read Cycle Time

TIMING WAVEFORMS

READ CYCLE

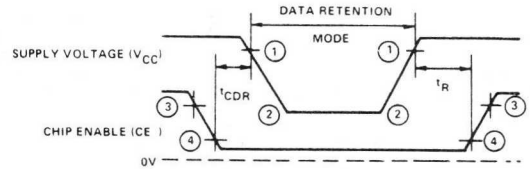


WRITE CYCLE



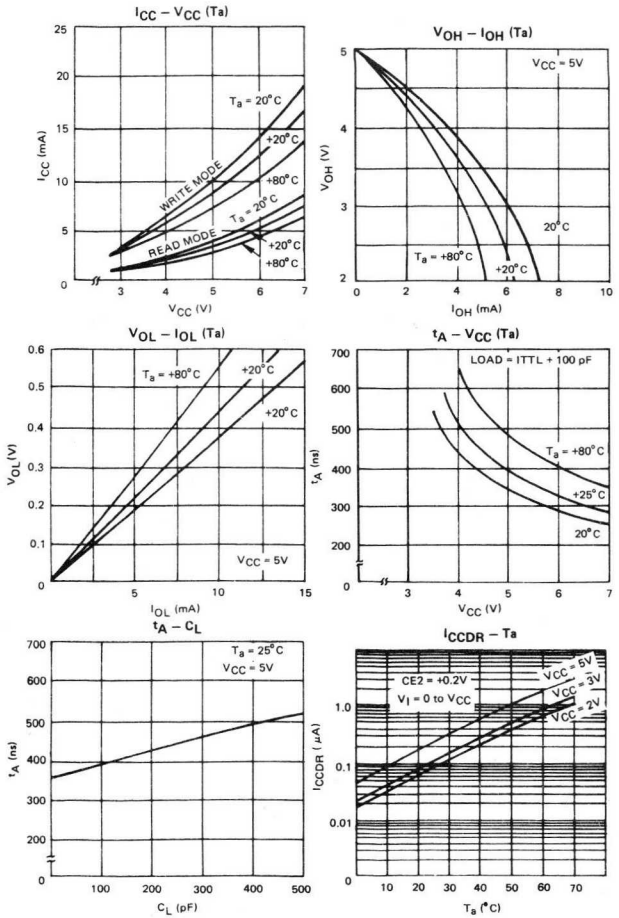
Notes: ① Typical values are for $T_a = 25°C$ and nominal supply voltage.
② OD may be tied low for separate I/O operation.
③ During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

LOW V_{CC} DATA RETENTION

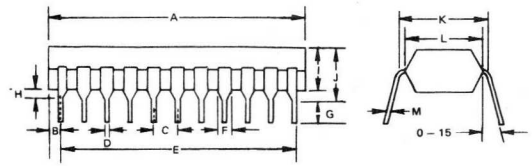


Notes: ① 4.75V
② V_{CCDR}
③ V_{IH}
④ 0.2V

TYPICAL OPERATING CHARACTERISTICS



PACKAGE OUTLINE μPD5101LC



ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50 ±0.10	0.02 ±0.004
E	25.4	1.0
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$

5101LDS-12-80-CAT

NOTES

NEC
μPD444/6514
μPD444/6514-1
μPD444/6514-2
μPD444/6514-3

1024 × 4 BIT STATIC CMOS RAM

DESCRIPTION

The μPD444/6514 is a high-speed, low power silicon gate CMOS 4096-bit static RAM organized 1024 words by 4 bits. It uses DC stable (static) circuitry throughout and therefore requires no clock or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

$\overline{CS}$ controls the power down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the μPD444/6514 — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ is high. There is no minimum $\overline{CS}$ high time for device operation, although it will determine the length of time in the power down mode. When $\overline{CS}$ goes low, selecting the μPD444/6514, the μPD444/6514 automatically powers up.

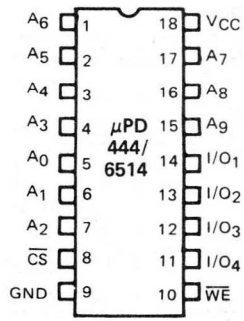
The μPD444/6514 is placed in an 18-pin plastic package for the highest possible density. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The μPD444/6514 is pin-compatible with the μPD2114L NMOS Static RAM.

Data retention is guaranteed to 2 volts on all parts. These devices are ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

FEATURES

- Low Power Standby — 5 μW Typ.
- Low Power Operation
- Data Retention — 2.0V Min.
- Capability of Battery Backup Operation
- Fast Access Time — 200-450 ns
- Identical Cycle and Access Times
- Single +5V Supply
- No Clock or Timing Strobe Required
- Completely Static Memory
- Automatic Power-Down
- Directly TTL compatible: All Inputs and Outputs
- Common Data Input and Output using Three-State Outputs
- Replacement for μPD2114L and Equivalent Devices
- Available in a Standard 18-Pin Plastic Package

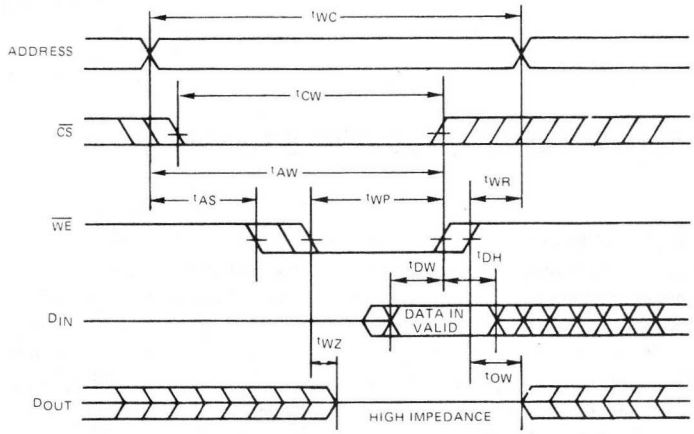
PIN CONFIGURATION



PIN NAMES

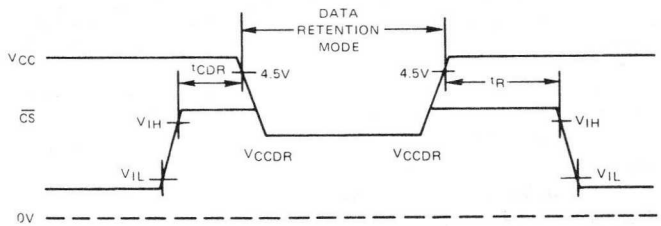
A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

WRITE CYCLE ④ ⑤ ⑥

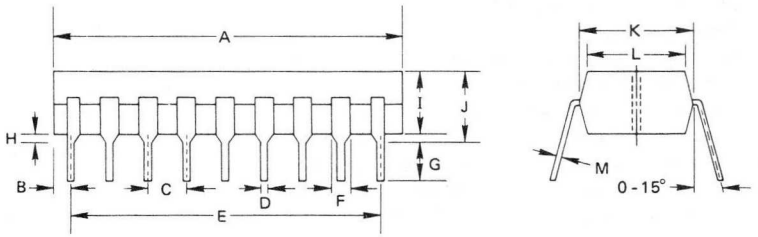


Notes: ① $\overline{WE}$ is high for Read Cycles.
② Device is continuously selected, $\overline{CS}$ = V_{IL}
③ Address valid prior to or coincident with $\overline{CS}$ transition low.
④ If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
⑤ $\overline{WE}$ must be high during all address transitions.
⑥ t_{WP} is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

LOW V_{CC} DATA RETENTION



PACKAGE OUTLINE μPD444/6514C



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.05
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

AC CHARACTERISTICS

T_a = −40 C to +85 C, V_{CC} = +5V ± 10% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS 444/6514-3 MIN	444/6514-3 MAX	444/6514-2 MIN	444/6514-2 MAX	444/6514-1 MIN	444/6514-1 MAX	444/6514 MIN	444/6514 MAX	UNIT	TEST CONDITIONS
READ CYCLE											
Read Cycle	t_{RC}	200		250		300		450		ns	Input Pulse Levels: +0.8 to +2.4 Volts Input Rise and Fall Times: 10 ns Input and Output Timing Levels: 1.5 Volt Output Load: 1 TTL Gate and C_L = 100 pF
Address Access Time	t_{AA}		200		250		300		450	ns	
Chip Select Access Time ①	t_{ACS1}		200		250		300		450	ns	
Chip Select Access Time ②	t_{ACS2}		250		300		350		500	ns	
Output Hold from Address Change	t_{OH}	50		50		50		50		ns	
Chip Selection to Output in Low Z	t_{LZ}	20		20		20		20		ns	
Chip Deselection to Output in High Z	t_{HZ}		60		70		80		100	ns	
WRITE CYCLE											
Write Cycle Time	t_{WC}	200		250		300		450		ns	Input Pulse Levels: +0.8 to +2.4 Volts Input Rise and Fall Times: 10 ns Input and Output Timing Levels: 1.5 Volt Output Load: 1 TTL Gate and C_L = 100 pF
Chip Selection to End of Write	t_{CW}	180		230		250		350		ns	
Address Valid to End of Write	t_{AW}	180		230		250		350		ns	
Address Setup Time	t_{AS}	0		0		0		0		ns	
Write Pulse Width	t_{WP}	180		210		230		300		ns	
Write Recovery Time	t_{WR}	0		0		0		0		ns	
Data Valid to End of Write	t_{DW}	120		140		150		200		ns	
Data Hold Time	t_{DH}	0		0		0		0		ns	
Write Enabled to Output in High Z	t_{WZ}		60		70		80		100	ns	
Output Active from End of Write	t_{OW}	0		0		0		0		ns	

Notes: ① Chip deselected for greater than 100 ns prior to selection.

② Chip deselected for a finite time that is less than 100 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)

LOW V_{CC} DATA RETENTION CHARACTERISTICS

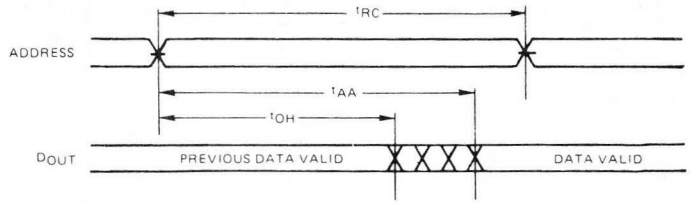
T_a = −40°C to +85°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Data Retention Supply Voltage	V_{CCDR}	2.0			V	$\overline{CS}$ = V_{CC}, V_{IN} = V_{CC} to GND
Data Retention Supply Current	I_{CCDR}		0.01	10	μA	V_{CC} = 3V, $\overline{CS}$ = V_{CC} V_{IN} = V_{CC} to GND
Chip Deselect to Data Retention Time	t_{CDR}	0			ns	
Operation Recovery Time	t_R	t_{RC} ①			ns	

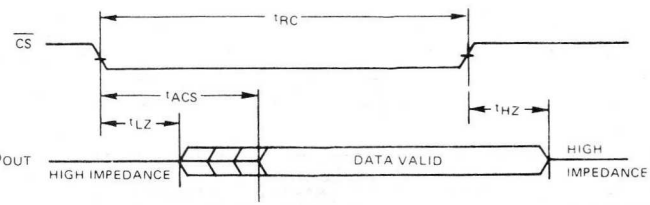
Note: ① t_{RC} = Read Cycle Time

TIMING WAVEFORMS

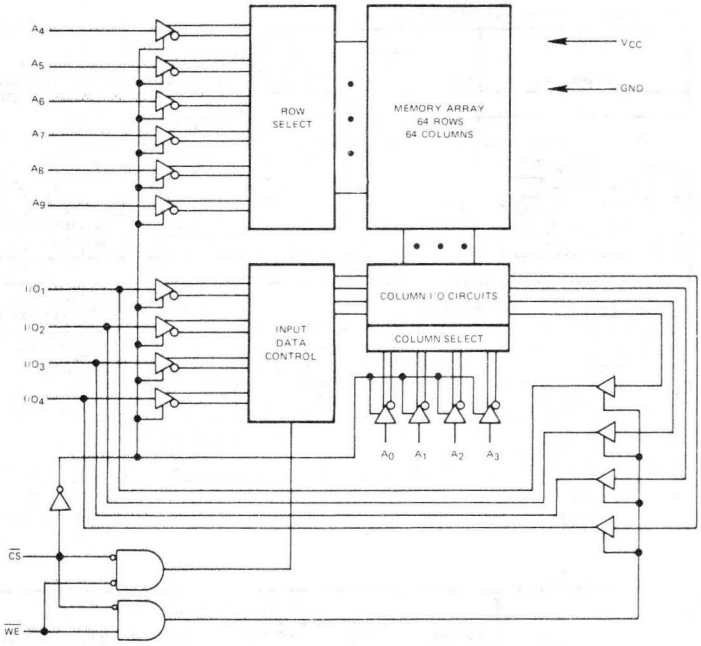
READ CYCLE ① ②



READ CYCLE ① ③



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−40°C to +85°C
Storage Temperature	−55°C to +125°C
All Input and Output Voltages	−0.3 to V_{CC} +0.3 Volts ①
Supply Voltage	+8.0 Volts

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −40°C to +85°C; V_{CC} = +5V ± 10% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS												UNIT	TEST CONDITIONS
		444/6514-3			444/6514-2			444/6514-1			444/6514				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Input Leakage Current	I_{LI}	−1.0		1.0	−1.0		1.0	−1.0		1.0	−1.0		1.0	μA	V_{IN} = GND to V_{CC}
I/O Leakage Current	I_{LO}	−1.0		1.0	−1.0		1.0	−1.0		1.0	−1.0		1.0	μA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}
Operating Supply Current	I_{CCA1}		19	35		15	35		12	35		9	35	mA	$\overline{CS}$ = V_{IL}, V_{IN} = V_{CC}, Outputs Open
Operating Supply Current	I_{CCA2}		23	40		19	40		15	40		12	40	mA	$\overline{CS}$ = V_{IL}, V_{IN} = 2.4V, Outputs Open
Average Operating Supply Current	I_{CCA3}		10	20		9	20		8	20		7	20	mA	V_{IN} = GND or V_{CC}, Outputs Open f = 1 MHz, Duty 50%
Standby Supply Current	I_{CCS}			50			50			50			50	μA	$\overline{CS}$ = V_{CC}, V_{IN} = GND to V_{CC}
Input Low Voltage	V_{IL}	−0.3		0.8	−0.3		0.8	−0.3		0.8	−0.3		0.8	V	
Input High Voltage	V_{IH}	2.4		V_{CC} + 0.3	2.4		V_{CC} + 0.3	2.4		V_{CC} + 0.3	2.4		V_{CC} + 0.3	V	
Output Low Voltage	V_{OL}			0.4			0.4			0.4			0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4			2.4			2.4			2.4			V	I_{OH} = −1.0 mA

CAPACITANCE

T_a = 25°C, f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input/Output Capacitance	$C_{I/O}$			10	pF	$V_{I/O}$ = 0V
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V

Note: This parameter is periodically sampled and not 100% tested.

FULLY DECODED 4096 STATIC CMOS RAM

3

DESCRIPTION

The μPD445L is a very low power 4,096 bit (1024 words by 4 bits) static RAM fabricated with NEC's complementary MOS (CMOS) process. It has two chip enable inputs ($\overline{CE}_1$, CE_2). Minimum standby current is drawn when $\overline{CE}_1$ is at a high level, while inhibiting all address and control line transitions or, unconditionally when CE_2 is at a low level. This device ideally meets the low power requirements of battery operated systems and battery back-up systems for non-volatility of data.

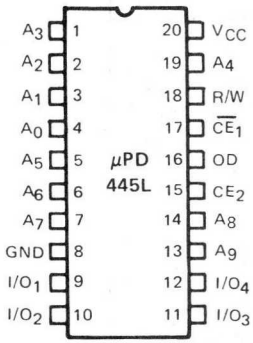
The μPD445L uses fully static circuitry requiring no clocking. Output data is read out non-destructively by placing a high on the R/W pin and has the same polarity as input data. All inputs and outputs are directly TTL compatible. The device has common input/output data busses and an OD (Output Disable) pin for use in common I/O bus systems.

The μPD445L is guaranteed to retain data with the power supply voltage as low as 2.0 volts.

FEATURES

- Single +5V Power Supply
- Ideal for Battery Operation
- Low Standby Power for Data Retention
- Simple Memory Expansion – Chip Enable Inputs
- Access Time – 650 ns Max. (μPD445L)
  450 ns Max. (μPD445L-1)
- Directly TTL Compatible – All Inputs and Outputs
- Common Data Input and Output
- Static CMOS – No Clock or Refreshing Required
- 20 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



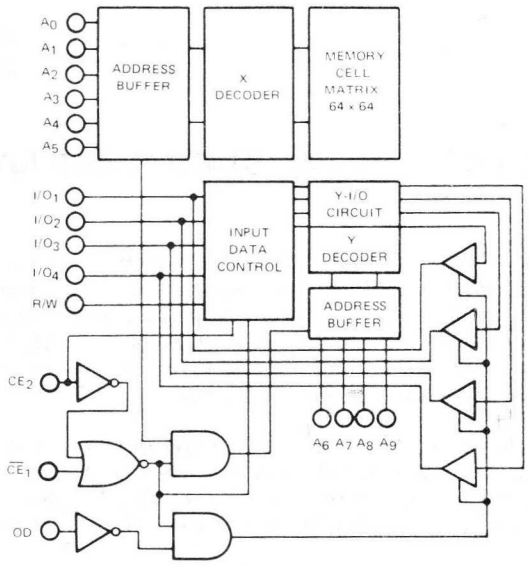
PIN NAMES

A_0-A_9	Address Input
OD	Output Disable
R/W	Read/Write
$\overline{CE}_1$	Chip Enable 1
CE_2	Chip Enable 2
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power Supply
GND	Ground

OPERATION MODES

$\overline{CE}_1$	CE_2	OD	Chip	Output Mode
0	1	0	Selected	Data Out
0	1	1		High Impedance
Others			Non-Selected	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −40°C to +125°C
All Output Voltages . . . . . −0.3 to V_{CC} +0.3 Volts
All Input Voltages . . . . . −0.3 to V_{CC} +0.3 Volts
Supply Voltage V_{CC} . . . . . −0.3 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+2.2		V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3		+ 0.65	V	
Output High Voltage	V_{OH1}	+2.4			V	I_{OH} = −1.0 mA
	V_{OH2}	+3.5			V	I_{OH} = −100 μA
Output Low Voltage	V_{OL}			+ 0.4	V	I_{OL} = +2.0 mA
Input Leakage Current High	I_{LIH}			+ 1.0	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			− 1.0	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			+ 1.0	μA	$V_O = V_{CC}$, $\overline{CE}_1$ = 2.2V
Output Leakage Current Low	I_{LOL}			1.0	μA	V_O = 0V, $\overline{CE}_1$ = 2.2V
Supply Current	I_{CC1}		12	25	mA	Outputs Open, $V_I = V_{CC}$ except $\overline{CE}_1 \leq$ 0.65V
Supply Current	I_{CC2}		16	30	mA	Outputs Open, V_I = 2.2V except $\overline{CE}_1 \leq$ 0.65V
Standby Current	I_{CCL}			40	μA	V_I = 0 to 5.25V Except $CE_2 \leq$ 0.2V

CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I		5	8	pF	V_I = 0V
Output Capacitance	C_O		8	12	pF	V_O = 0V

AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS 445L MIN	LIMITS 445L MAX	LIMITS 445L-1 MIN	LIMITS 445L-1 MAX	UNIT	TEST CONDITIONS
Read Cycle Time	t_{RC}	650		450		ns	
Access Time	t_A		650		450	ns	Input Voltage Levels
Chip Enable ($\overline{CE}_1$) to Output	t_{CO1}		600		400	ns	V = +0.65 to +2.2V
Chip Enable (CE_2) to Output	t_{CO2}		700		500	ns	Input Rise Time 20 ns
Output Enable to Output	t_{OD}		350		250	ns	Input Fall Time 20 ns
Output Disable (OD) to Floating	t_{DF}	0	150	0	130	ns	Timing Measurement Reference Level = +1.5V
Data Output Hold Time	t_{OH1}	0		0		ns	Output Load
Chip Disable to Floating	t_{OH2}	0		0		ns	1 TTL + 100 pF
Address Rise and Fall Time	t_r t_f		300		300	ns	For Address change during Chip Enabled

WRITE CYCLE

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS 445L MIN	LIMITS 445L MAX	LIMITS 445L-1 MIN	LIMITS 445L-1 MAX	UNIT	TEST CONDITIONS
Write Cycle Time	t_{WC}	650		450		ns	
Address Setup Time	t_{AW}	150		130		ns	Input Voltage Levels V_I = +0.65 to +2.2V
Chip Enable ($\overline{CE}_1$) to Write End	t_{CW1}	550		350		ns	Input Rise Time 20 ns
Chip Enable (CE_2) to Write End	t_{CW2}	550		350		ns	Input Fall Time 20 ns
Data Setup Time	t_{DW}	400		250		ns	
Data Hold Time	t_{DH}	100		50		ns	Timing Measurement
Write Pulse Width	t_{WP}	400		250		ns	Reference Level = +1.5V
Address Hold Time	t_{WR}	50		50		ns	
Output Disable Setup Time	t_{DS}	150		130		ns	
Address Rise and Fall Time	t_r t_f		300		300	ns	For Address change during Chip Enabled

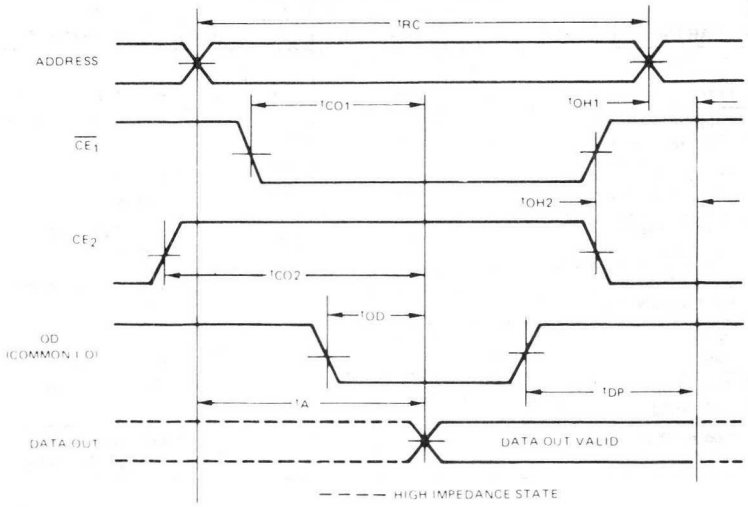
LOW V_{CC} DATA RETENTION

T_a = 0°C to +70°C

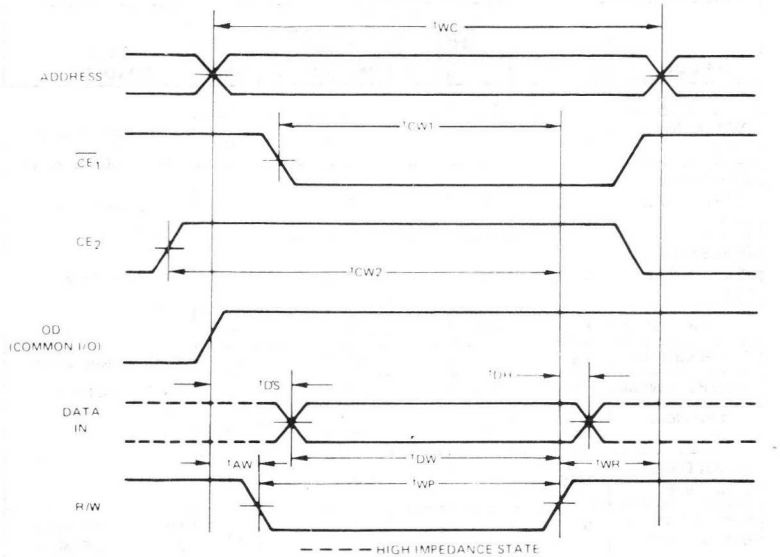
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \leqslant +0.2V$
Data Retention Current	I_{CCDR}			40	μA	V_{CCDR} = +2.0V $CE_2 \leqslant +0.2V$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_R	t_{RC} ①			ns	

Note: ① t_{RC} = Read Cycle Time

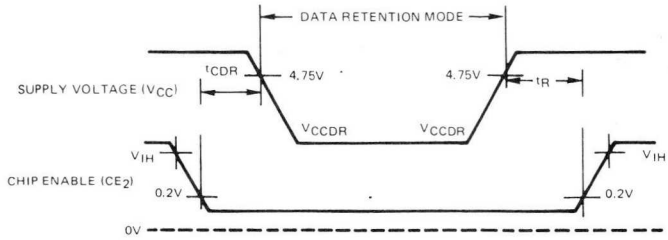
READ CYCLE



WRITE CYCLE

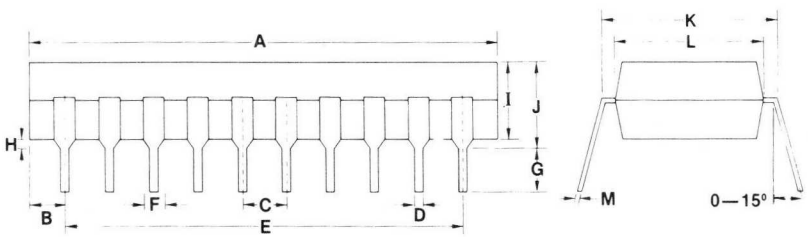


LOW V_{CC} DATA RETENTION ①



Note ① Apply less than V_{CCDR} to all inputs for data retention mode.

PACKAGE OUTLINE μPD445LC



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	27.00	1.07
B	2.07	0.08
C	2.54	0.10
D	0.50	0.02
E	22.86	0.90
F	1.20	0.05
G	2.54 MIN	0.10 MIN
H	0.50 MIN	0.02 MIN
I	4.58 MAX	0.18
J	5.08 MAX	0.20
K	10.16	0.40
L	8.60	0.39
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

NEC
μPD446
μPD446-1
μPD446-2
PRELIMINARY

2048 x 8 BIT STATIC CMOS RAM

DESCRIPTION

The μPD446 is a high speed, low power, 2048 word by 8 bit static CMOS RAM fabricated using an advanced silicon gate CMOS technology. A unique circuitry technique makes the μPD446 a very low operating power device which requires no clock or refreshing to operate. Minimum standby power current is drawn by this device when $\overline{CE}$ equals V_{CC} independently of the other input levels.

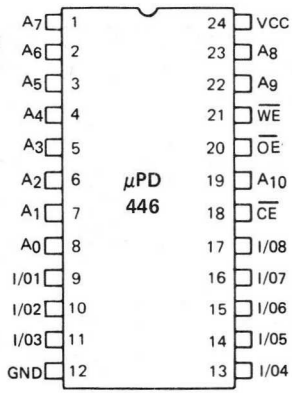
Data retention is guaranteed at a power supply voltage as low as 2V.

The μPD446 is packaged in a standard 24-pin dual-in-line package and is plug-in compatible with 16K EPROMs.

FEATURES

- Single +5V Supply
- Fully Static Operation — No Clock or Refreshing required
- TTL Compatible — All Inputs and Outputs
- Common I/O Using Three-State Output
- $\overline{OE}$ Eliminates Need for External Bus Buffers
- Max Access/Min Cycle Times Down to 120 ns
- Low Power Dissipation, 45 mA Max Active/100 μA Max Standby/ 10 μA Max Data Retention
- Data Retention Voltage — 2V Min
- Standard 24-Pin Plastic and Ceramic Packages
- Plug-in Compatible with 16K EPROMs

PIN CONFIGURATION



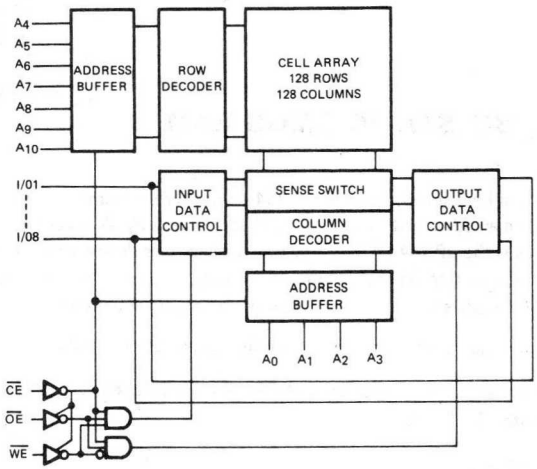
PIN NAMES

A_0-A_{10}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/O1-I/O8	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	ICC
H	X	X	NOT SELECTED	HZ	STANDBY
L	H	H	NOT SELECTED	HZ	ACTIVE
L	L	H	READ	D_{OUT}	ACTIVE
L	X	L	WRITE	D_{IN}	ACTIVE

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 7.0V
Input or Output Voltage Supplied . . . . . -0.3 to VCC + 0.3V
Storage Temperature Range . . . . . -55°C to 125°C
Operating Temperature Range . . . . . 0°C to 70°C

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0 to 70°C; V_{CC} = 5.0V ± 10%

CHARACTERISTIC	SYMBOL	μPD446-2			μPD446-1			μPD446			UNIT	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Input High Voltage	V_{IH}	2.2		V_{CC} +0.3	2.2		V_{CC} +0.3	2.2		V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.8	-0.3		0.8	-0.3		0.8	V	
Input Leakage Current	I_{LI}	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA	V_{IN} = 0~ V_{CC}
I/O Leakage Current	I_{LO}	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA	V_{CS} = V_{IH} $V_{I/O}$ = 0 ~ V_{CC}
Operating Supply Current	I_{CCA_1}		30	45		25	38		20	30	mA	V_{CS} = V_{IL} $I_{I/O}$ = 0 MIN TCYCLE
	I_{CCA_2}		5	10		5	10		5	10	mA	V_{CS} = V_{IL} $I_{I/O}$ = 0 DC CURRENT
Standby Current	I_{CCS}			100			100			100	μA	V_{CS} = V_{CC} V_{IN} = 0 ~ V_{CC}
Output High Voltage	V_{OH}	2.4			2.4			2.4			V	I_{OH} = -1.0 mA
Output Low Voltage	V_{OL}			0.4			0.4			0.4	V	I_{OL} = 2.0 mA

CAPACITANCE

T_a = 25°C, f = 1.0 MHz

PARAMETER	SYMBOL	LIMITS		UNIT	TEST CONDITIONS
		MIN	MAX		
Input Capacitance	C_{IN}		6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$		8	pF	$V_{I/O}$ = 0V

AC CHARACTERISTICS

READ CYCLE

V_{CC} = 5.0V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	LIMITS						UNIT
		μPD446-2		μPD446-1		μPD446		
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AA}		120		150		200	ns
Chip Enable Access Time	t_{ACS}		120		150		200	ns
Output Enable to Output Valid	t_{OE}		60		75		100	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns
Chip Enable to Output in LZ	t_{CLZ}	10		10		10		ns
Output Enable to Output in LZ	t_{OLZ}	10		10		10		ns
Chip Disable to Output in HZ	t_{CHZ}		60		75		100	ns
Output Disable to Output in HZ	t_{OHZ}		60		75		100	ns

WRITE CYCLE

V_{CC} = 5.0V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	LIMITS						UNIT
		μPD446-2		μPD446-1		μPD446		
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	120		150		200		ns
Chip Enable to End of Write	t_{CW}	100		125		170		ns
Address Valid to End of Write	t_{AW}	100		125		170		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Pulsewidth	t_{WP}	100		125		170		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Data Valid to End of Write	t_{DW}	60		75		100		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enable to Output in HZ	t_{WHZ}		60		75		100	ns
Output Active from End of Write	t_{OW}	20		20		20		ns

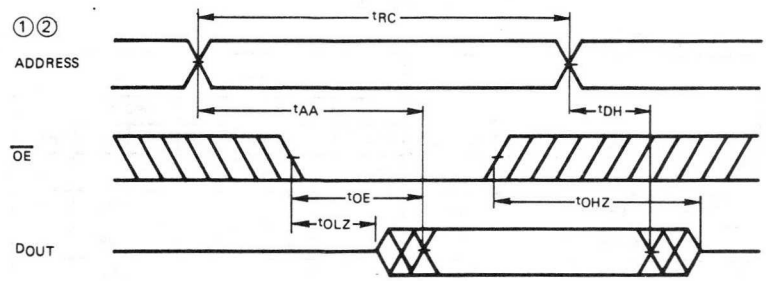
LOW V_{CC} DATA RETENTION

T_a = 0°C to 70°C

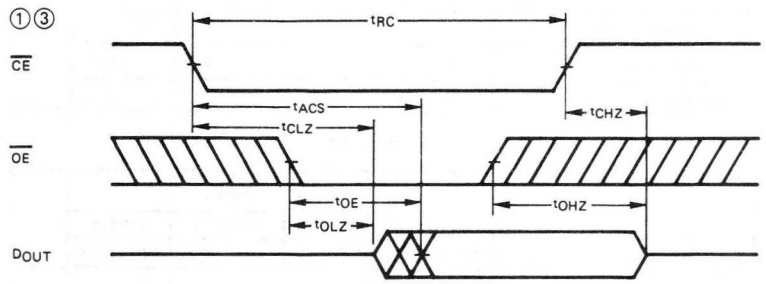
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
VCC for Data Retention	V_{CCDR}	V_{IN} = 0 ~ V_{CC}, $V_{\overline{CE}}$ = V_{CC}	2.0			V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, V_{IN} = 0 ~ V_{CC} $V_{\overline{CE}}$ = V_{CC}		0.1	10	μA
Chip Deselection to Data Retention Time	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

TIMING WAVEFORMS

READ CYCLE (1)



READ CYCLE (2)



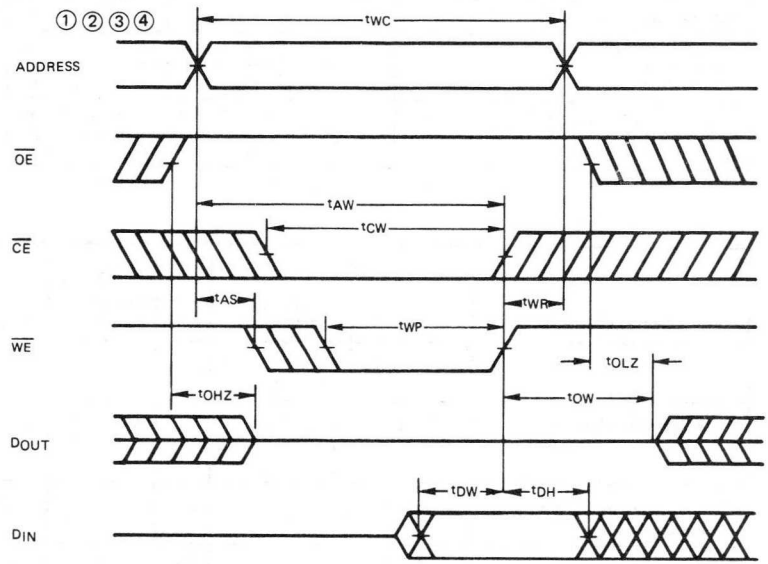
NOTES:

① $\overline{WE}$ is high for read cycles.

② Device is continuously selected, $\overline{CE} = V_{IL}$.

③ Address valid prior to or coincident with $\overline{CE}$ transition low.

WRITE CYCLE (1)



NOTES:

① $\overline{WE}$ must be high during all address transition.

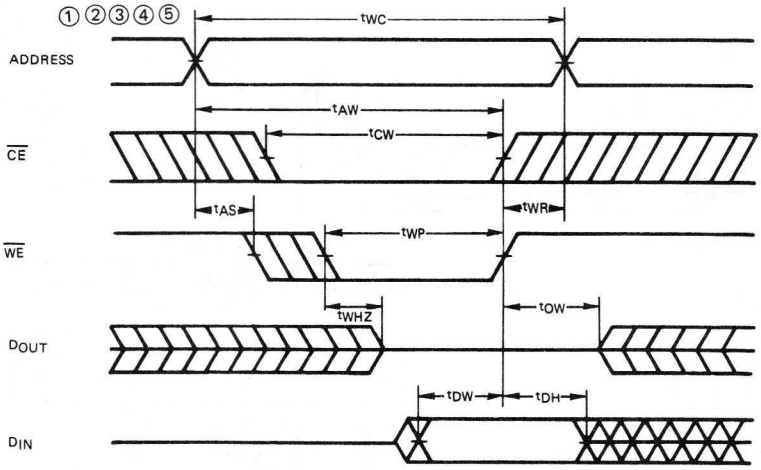
② A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.

③ t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.

④ If the CS low transition occurs simultaneously with or after the $\overline{WE}$ low transition, output buffers remain in a high impedance state.

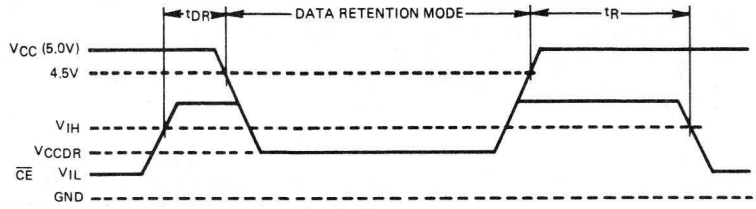
TIMING WAVEFORMS (CONT.)

WRITE CYCLE (2)



Notes:
① $\overline{WE}$ must be high during all address transition.
② A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.
③ t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
④ If the CS low transition occurs simultaneously with or after the $\overline{WE}$ low transition, output buffers remain in a high impedance state.
⑤ $\overline{OE}$ is continuously low ($\overline{OE}$ – V_{IL}).

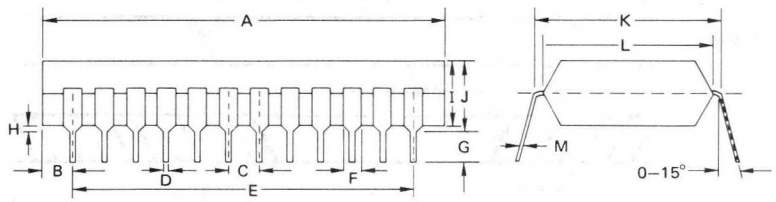
LOW V_{CC} DATA RETENTION TIMING CHART



AC TEST CONDITIONS

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL + 100 pF

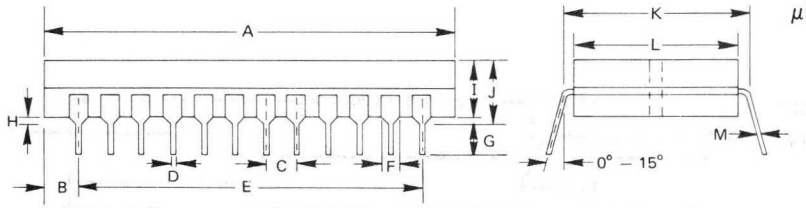
PACKAGE OUTLINE
μPD446C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPD446D



(CERDIP)

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

NEC
μPD447
μPD447-1
μPD447-2
PRELIMINARY

2048 x 8 BIT STATIC CMOS RAM

DESCRIPTION

The μPD447 is a high speed, low power, 2048 word by 8 bit static CMOS RAM fabricated using an advanced silicon gate CMOS technology. A unique circuitry technique makes the μPD447 a very low operating power device which requires no clock or refreshing to operate.

Since the device has two chip enable inputs, it is suited for battery backup applications. Minimum standby power current is drawn by this device when $\overline{CE2}$ equals V_{CC} independently of the other input levels.

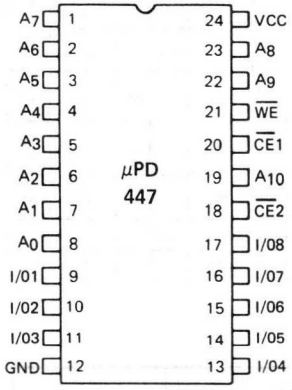
Data Retention is guaranteed at a power supply voltage as low as 2V.

The μPD447 is packaged in a standard 24-pin dual-in-line package and is plug-in compatible with 16K EPROMs.

FEATURES

- Single +5V Supply
- Fully Static Operation – No Clock or Refreshing required
- TTL Compatible – All Inputs and Outputs
- Common Data Input and Output Using Three-State Output
- Two Chip Enable Inputs for Battery Operation
- Max Access/Min Cycle Times Down to 120 ns
- Low Power Dissipation; 45 mA Max Active/100 μA Max Standby/ 10 μA Max Data Retention
- Data Retention Voltage – 2V Min
- Standard 24-Pin Plastic and Ceramic Packages
- Plug-in Compatible with 16K EPROMs

PIN CONFIGURATION



PIN NAMES

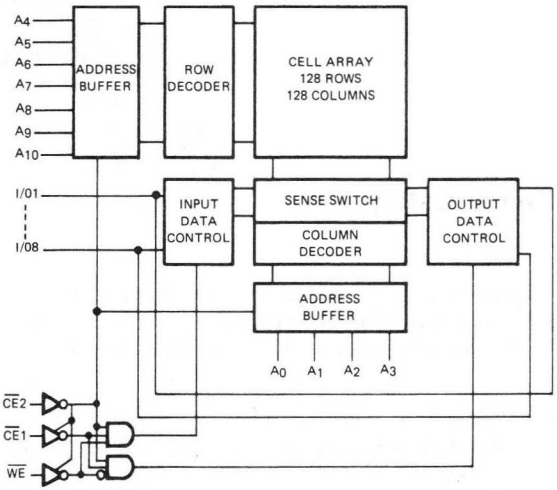
A_0-A_{10}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CE1}$-$\overline{CE2}$	Chip Enable Inputs
I/0[-I/08	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	MODE	I/O	ICC
X	H	X	NOT SELECTED	HZ	STANDBY
H	X	X	NOT SELECTED	HZ	ACTIVE
L	L	L	WRITE	D_{IN}	ACTIVE
L	L	H	READ	D_{OUT}	ACTIVE

μPD447

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 7.0V
Input or Output Voltage Supplied . . . . . -0.3 to VCC + 0.3V
Storage Temperature Range . . . . . -55°C to 125°C
Operating Temperature Range . . . . . 0°C to 70°C

COMMENT Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS μPD447-2 MIN	μPD447-2 TYP	μPD447-2 MAX	μPD447-1 MIN	μPD447-1 TYP	μPD447-1 MAX	μPD447 MIN	μPD447 TYP	μPD447 MAX	UNIT
Input High Voltage	V_{IH}		2.2		V_{CC} + 0.3	2.2		V_{CC} + 0.3	2.2		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	-0.3		0.8	-0.3		0.8	V
Input Leakage Current	I_{LI}	V_{IN} = 0 ~ V_{CC}	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA
I/O Leakage Current	I_{LO}	$V_{\overline{CE}2}$ = V_{IH} $V_{I/O}$ = 0 ~ V_{CC}	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA
Operating Supply Current	I_{CCA1}	$V_{\overline{CE}2}$ = V_{IL} $I_{I/O}$ = 0 MIN TCYCLE		30	45		25	39		20	30	mA
	I_{CCA2}	$V_{\overline{CE}2}$ = V_{IL} $I_{I/O}$ = 0 DC CURRENT		5	10		5	10		5	10	mA
Standby Current	I_{CCS}	$V_{\overline{CE}2}$ = V_{CC} V_{IN} = 0 ~ V_{CC}			100			100			100	μA
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			2.4			2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA			0.4			0.4			0.4	V

CAPACITANCE

T_a = 25°C, f = 1.0 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$		8	pF	$V_{I/O}$ = 0V

AC CHARACTERISTICS

READ CYCLE

V_{CC} = 5.0V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	LIMITS μPD447-2 MIN	LIMITS μPD447-2 MAX	LIMITS μPD447-1 MIN	LIMITS μPD447-1 MAX	LIMITS μPD447 MIN	LIMITS μPD447 MAX	UNIT
Read Cycle Time	t_{RC}	120		150		200		ns
Access Time	t_A		120		150		200	ns
Chip Enable (CE1) to Output Valid	t_{CO1}		60		75		100	ns
Chip Enable (CE2) to Output Valid	t_{CO2}		120		150		200	ns
Output Hold from Address Change	t_{OH}	20		20		20		ns
Chip Enable (CE1) to Output in LZ	t_{LZ1}	10		10		10		ns
Chip Enable (CE2) to Output in LZ	t_{LZ2}	10		10		10		ns
Chip Enable (CE1) to Output in HZ	t_{HZ1}		60		75		100	ns
Chip Enable (CE2) to Output in HZ	t_{HZ2}		60		75		100	ns

WRITE CYCLE

V_{CC} = 5.0V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	LIMITS μPD447-2 MIN	LIMITS μPD447-2 MAX	LIMITS μPD447-1 MIN	LIMITS μPD447-1 MAX	LIMITS μPD447 MIN	LIMITS μPD447 MAX	UNIT
Write Cycle Time	t_{WC}	120		150		200		ns
Chip Enable (CE1) to End of Write	t_{CW1}	100		125		170		ns
Chip Enable (CE2) to End of Write	t_{CW2}	100		125		170		ns
Address Setup Time	t_{AW}	0		0		0		ns
Write Pulsewidth	t_{WP}	100		125		170		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write Enable to Output in HZ	t_{WZ}		60		75		100	ns
Output Active from End of Write	t_{OW}	20		20		20		ns
Data Valid to End of Write	t_{DW}	60		75		100		ns
Data Hold Time	t_{DH}	0		0		0		ns

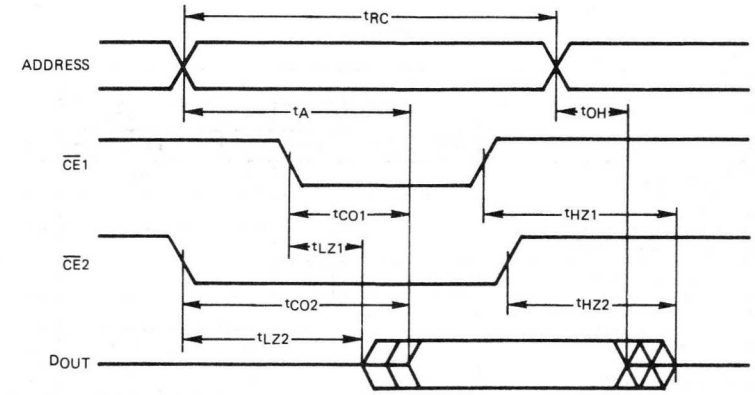
LOW VCC DATA RETENTION

T_a = 0°C to 70°C

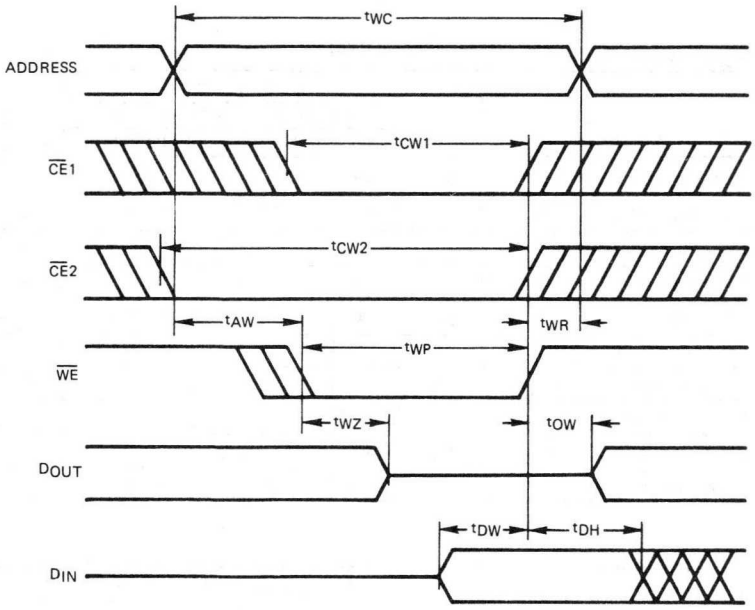
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
V_{CC} for Data Retention	V_{CCDR}	$V_{\overline{IN}} = 0 \sim V_{CC}$, $V_{\overline{CE2}} = V_{CC}$	2.0			V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, $V_{\overline{IN}} = 0 \sim V_{CC}$ $V_{\overline{CE2}} = V_{CC}$		0.1	10	μA
Chip Disable to Data Retention Time	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

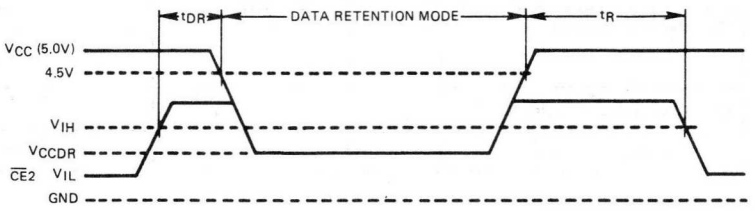
TIMING WAVEFORMS

READ CYCLE TIMING CHART



WRITE CYCLE TIMING CHART





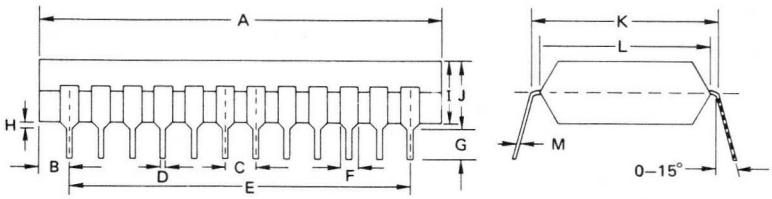
LOW VCC
DATA RETENTION
TIMING CHART

AC TEST CONDITIONS

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL + 100 pF

PACKAGE OUTLINE

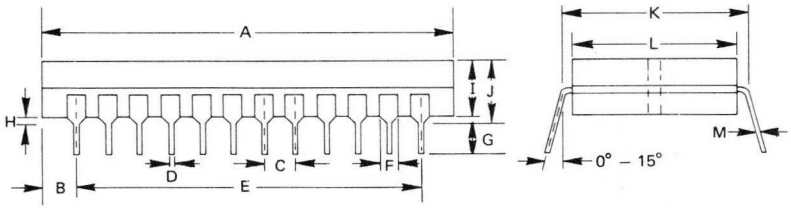
μPD447C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPD447D



(CERDIP)

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

NOTES

ROM ORDERING PROCEDURE — MEMORIES AND MICROCOMPUTERS

The following NEC products fall under the guidelines set by the ROM Ordering Procedure:

μPD2316E	μPD8021	μPD547L	μPD651
μPD2332A	μPD8022	μPD550	μPD651G
μPD2332A-1	μPD8041A	μPD550L	μPD652
μPD2332B	μPD8048	μPD552	μPD7502
μPD2332B-1	μPD80C48	μPD553	μPD7503
μPD2364	μPD8049	μPD554	μPD7507
μPD23128	μPD8355	μPD554L	μPD7520
μPD7801	μPD546	μPD557L	μPD7720
μPD7802	μPD547	μPD650	

NEC Microcomputers, Inc., is able to accept mask patterns in a variety of formats to facilitate the transferral of ROM mask information. These are intended to suit various customer needs and minimize the turnaround time. Always enclose a listing of the code and the code submittal form. The following is a list of valid media for code transferral.

- PROM/EPROM equivalent to ROM parts
- Sample ROMs or ROM-based microcomputers
- NEC μPD458 EEPROM
- Paper Tape
- Timesharing Files
- Other (Contact NEC Microcomputers, Inc., for arrangements.)

Thoroughly tested verification procedures protect against unnecessary delays or costly mistakes. NEC Microcomputers, Inc. will return the ROM mask patterns to the customer in the most convenient format. Unprogrammed EPROMs, if sent with the ROM code, can be programmed and returned for verification.

Earth satellites and the world-wide GE Mark III timesharing systems provide reliable and instant communication of ROM patterns to the factory. Customers with access to GE-TSS may further reduce the turnaround time by transferring files directly to NEC Microcomputers, Inc.

The following is an example of a ROM mask transferral procedure. The μPD8048 is used here; however, the process is the same for the other ROM-based products.

1. The customer contacts NEC Microcomputers' Sales Representative, concerning a ROM pattern for the μPD8048 that he would like to send.

2. Since an EPROM version of that part is available, the μPD8748 is proposed as a code transferral medium, or a paper tape and listing may be used.

3. Two programmed μPD8748's are sent to NEC Microcomputers, Inc. with a listing, a code submittal form, and a paper tape as back-up.

4. NEC Microcomputers, Inc. compares the media provided and enters the code into GS-TSS. The GE-TSS file is accessed at the NEC factory and a copy of the code is returned to NEC Microcomputers for verification. One of the μPD8748's is erased and reprogrammed with the customer's code as the NEC factory has it. Both μPD8748's and a listing are returned to the customer for his final verification.

5. Once the customer notifies NEC Microcomputers, Inc. in writing that the code is verified and provides the mask charge and hard copy of the purchase order, work begins immediately on developing his μPD8048s.

Please contact your local Sales Representative for assistance with all ROM-based product orders.

NOTES

FULLY DECODED 8,192 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPD2308A is a high-speed 8, 192-bit mask-programmable Read Only Memory organized as 1024 words by 8 bits. The μPD2308A is fabricated with N-channel MOS technology.

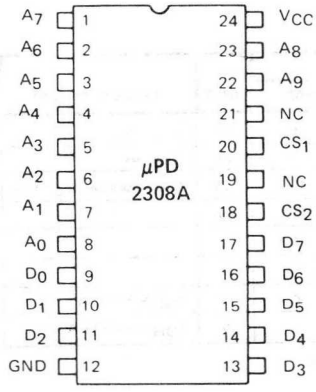
The inputs and outputs are fully TTL-compatible. The device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and desired chip select code is fixed during the masking process.

4

FEATURES

- Access Time 450 ns Max
- 1024 Words x 8 Bits Organization
- Single +5V ±10% Power Supply Voltage
- Directly TTL-Compatible – All Inputs and Outputs
- Two Programmable Chip Select Inputs for Easy Memory Expansion
- Three-State Output – OR-Tie Capability
- On-Chip Address Fully Decoded
- All Inputs Protected Against Static Charge
- Direct Replacement for 2308A
- Available in 24-pin plastic or ceramic packages

PIN CONFIGURATION



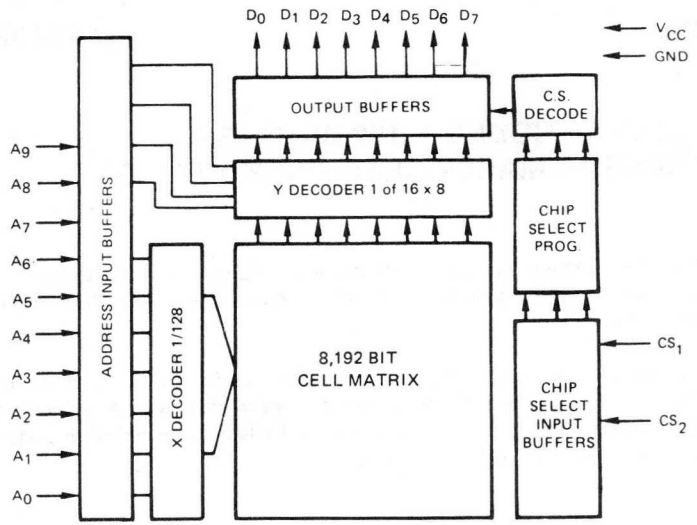
PIN NAMES

$A_0 - A_9$	Address Inputs
$D_0 - D_7$	Data Outputs
$CS_1 - CS_2$	Programmable Chip Select Inputs

Rev/1

μ PD2308A

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
Voltage on Any Pin	−0.5 to +7.0 Volts (1)

Note: (1) With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = +5 ± 5% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP (1)	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			+10	μA	$V_{IN} = V_{CC}$
				−10	μA	V_{IN} = 0V
Output Leakage Current	I_{LOH}			+10	μA	Chip Deselected, $V_O = V_{CC}$
Power Supply Current	I_{CC}		60	85	mA	
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC}	V	
Output "Low" Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA
Output "High" Voltage	V_{OH}	+2.4			V	I_{OH} = −200 μA

Note: (1) Typical values for T_a = 25°C and nominal supply voltage.

CAPACITANCE

$T_a = 25°C$; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		5	7	pf	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}		7	10	pf	All Pins Except Pin Under Test Tied to AC Ground

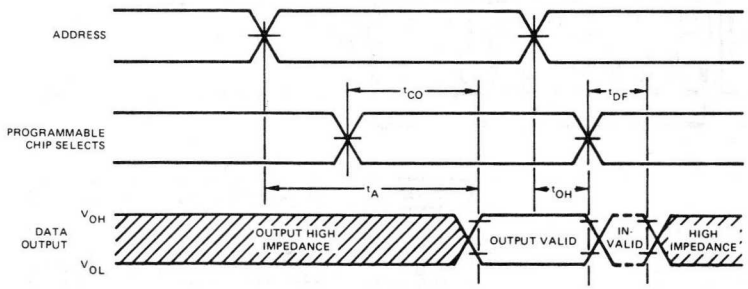
AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$ unless otherwise specified.

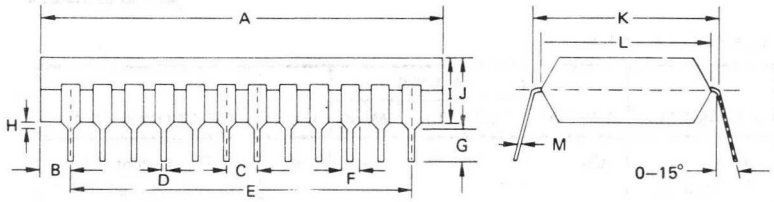
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP①	LIMITS MAX	UNIT	TEST CONDITIONS
Address to Output Delay Time	t_A		350	450	ns	$t_T = t_r = t_f = 20$ ns $V_{ref\ in} = 1V, 2.2V$ $V_{ref\ out} = 0.8V, 2V$ Output LOAD = 1 TTL GATE $C_L = 100$ pf
Chip Select to Output Enable Delay Time	t_{CO}			120	ns	
Chip Deselect to Output Data Float Delay Time	t_{DF}	10		100	ns	
Previous Data Valid After Address Change	t_{OH}	20			ns	

Note: ① $T_a = 25°C$; $V_{CC} = +5V$

TIMING WAVEFORMS



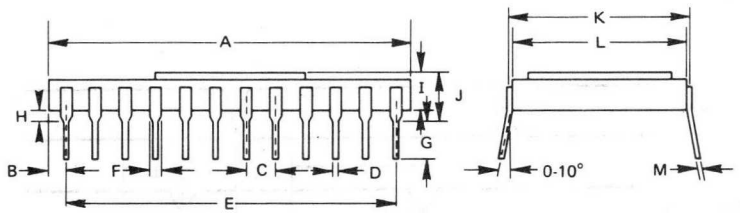
PACKAGE OUTLINES
μPD2308AC



Plastic

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.55 MAX
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPD2308AD



Ceramic

ITEM	MILLIMETERS	INCHES
A	30.78 MAX.	1.23 MAX.
B	1.53 MAX.	0.07 MAX.
C	2.54 ± 0.1	0.10 ± 0.004
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94 ± 0.1	1.10 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.125 MIN.
H	1.02 MIN.	0.04 MIN.
I	3.23 MAX.	0.13 MAX.
J	4.25 MAX.	0.17 MAX.
K	15.24 TYP.	0.60 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.010 ± 0.002

FULLY DECODED 16,384 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPD2316E is a high speed 16,384 bit mask programmable Read Only Memory organized as 2048 words by 8 bits. The μPD2316E is fabricated with N-channel MOS technology.

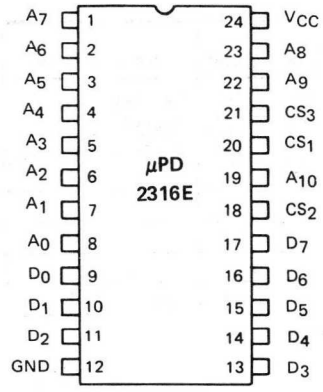
The inputs and outputs are fully TTL compatible. The device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and desired chip select code is fixed during the masking process.

4

FEATURES

- High Speed – Access Times: μPD2316E – 450 ns
  μPD2316E-1 – 350 ns
- 2048 Words x 8 Bits Organization
- Single +5V ±10% Power Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Three Programmable Chip Select Inputs for Easy Memory Expansion
- Three-State Output – OR-Tie Capability
- On-Chip Address Fully Decoded
- All Inputs Protected Against Static Charge
- Direct Replacement for 2316E
- Available in 24-pin plastic or ceramic dual-in-line packages

PIN CONFIGURATION

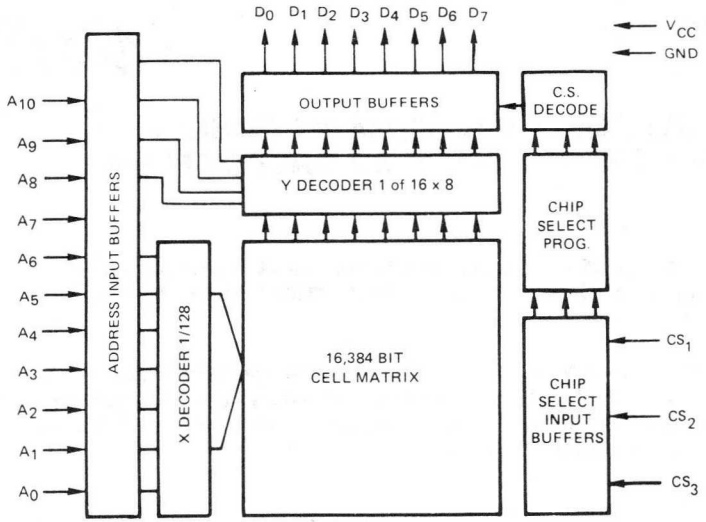


PIN NAMES

$A_0 - A_{10}$	Address Inputs
$D_0 - D_7$	Data Outputs
$CS_1 - CS_3$	Programmable Chip Select Inputs

Rev/1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Voltage on Any Pin . . . . . −0.5 to +7.0 Volts (1)

Note: (1) With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = +5V ± 10% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP (1)	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			+10	μA	$V_{IN} = V_{CC}$
				−10	μA	V_{IN} = 0V
Output Leakage Current	I_{LOH}			+10	μA	Chip Deselected, $V_O = V_{CC}$
Power Supply Current	I_{CC}		60	85	mA	
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC}	V	
Output "Low" Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA
Output "High" Voltage	V_{OH}	+2.4			V	I_{OH} = −200 μA

Note: (1) Typical values for T_a = 25°C and nominal supply voltage.

CAPACITANCE

$T_a = 25°C$; f = 1 MHz

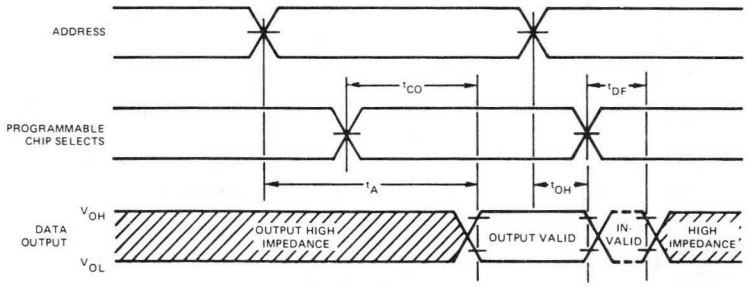
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		5	7	pf	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}		7	10	pf	All Pins Except Pin Under Test Tied to AC Ground

AC CHARACTERISTICS

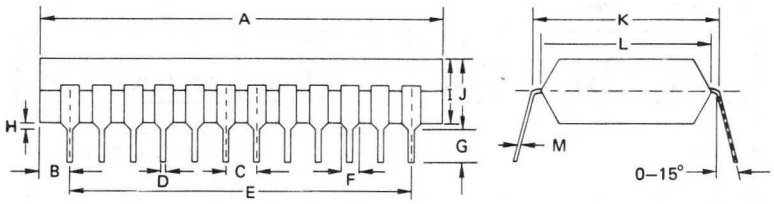
$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$; unless otherwise specified.

PARAMETER	SYMBOL	LIMITS μPD2316E MIN.	LIMITS μPD2316E MAX.	LIMITS μPD2316E-1 MIN.	LIMITS μPD2316E-1 MAX.	UNIT	TEST CONDITIONS
Address to Output Delay Time	t_{ACC}		450		350	ns	$t_T = t_r = t_f = 20$ ns
Chip Select to Output Enable Delay Time	t_{CO}		150		150	ns	$C_L = 100$ pF
Chip Deselect to Output Data Float Delay Time	t_{DF}	0	150		100	ns	Load = 1TTL gate
Output Hold Time	t_{OH}	20		20		ns	$V_{IN} = 0.8$ to 2V V_{ref} Input = 1.5V V_{ref} Output = 0.45/2.2V

TIMING WAVEFORMS



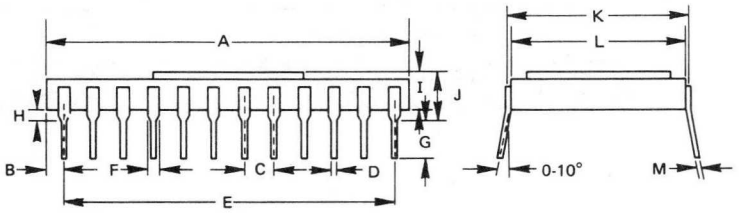
4



PACKAGE OUTLINE
μPD2316EC

(Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.55 MAX.
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPD2316ED

(Ceramic)

ITEM	MILLIMETERS	INCHES
A	30.78 MAX.	1.23 MAX.
B	1.53 MAX.	0.07 MAX.
C	2.54 ± 0.1	0.10 ± 0.004
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94 ± 0.1	1.10 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.125 MIN.
H	1.02 MIN.	0.04 MIN.
I	3.23 MAX.	0.13 MAX.
J	4.25 MAX.	0.17 MAX.
K	15.24 TYP.	0.60 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.010 ± 0.002

NEC
μPD2332A
μPD2332A-1
μPD2332B
μPD2332B-1

FULLY DECODED 32,768 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

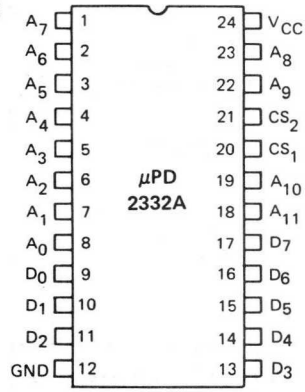
The NEC μPD2332A/B is a Fully Decoded 32,768 Bit Mask Programmable Read-Only Memory organized as 4,096 Words by 8 Bits. The μPD2332A/B has two chip select inputs and the combination of "High"/"Low" levels of these inputs is mask-programmable.

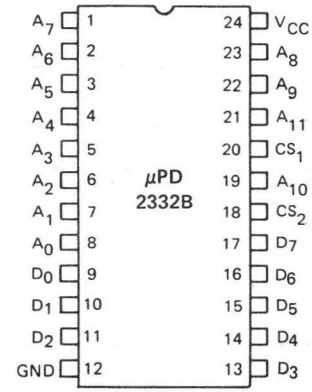
The μPD2332A/B is fabricated with sophisticated N-channel MOS technology and features high speed and TTL compatibility for simple interface with bipolar circuits.

FEATURES

- 4096 Words x 8 Bits Organization
- Directly TTL Compatible – All Inputs and Outputs
- Fully Static (No Clock or Refresh Required)
- Single +5V Power Supply
- High Speed – Access Times: μPD2332A/B – 450 ns
  μPD2332A/B-1 – 350 ns
- Three-State Output – OR-Tie Capability
- Two Programmable Chip Select Inputs for Easy Memory Expansion
- Available in Either JEDEC Pinout: μPD2332A or μPD2332B
- N-Channel MOS Technology
- Available in 24 Pin Plastic or Ceramic Dual-in-Line Package

PIN CONFIGURATIONS





PIN NAMES

$A_0 - A_{11}$	Address Inputs
$D_0 - D_7$	Data Outputs
$CS_1 - CS_2$	Programmable Chip Select Inputs

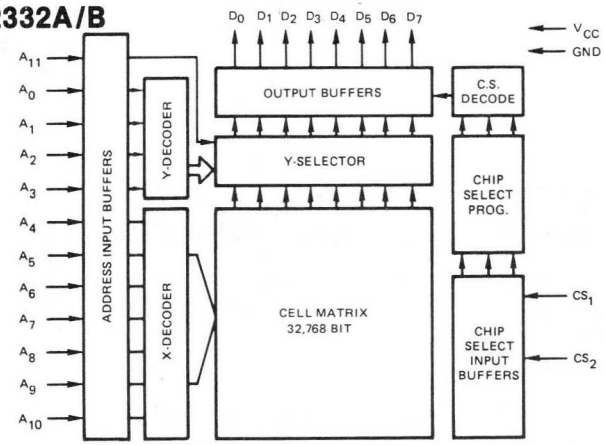
When ordering the μPD2332A/B, specify a chip select combination of CS_1 and CS_2 from the following.

CS_2	CS_1
0	0
0	1
1	0
1	1

Rev/2

μPD2332A/B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Supply Voltage On Any Pin . . . . . −0.5 to +7.0 Volts①

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = +5V ±10%; unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			10	μA	V_{IN} = 0 to +5.5V
Output Leakage Current	I_{LOH}			+10	μA	CS = 2.2V (Deselected) V_{OUT} = V_{CC}
Output Leakage Current	I_{LOL}			−10	μA	CS = 2.2V (Deselected) V_{OUT} = 0V
Power Supply Current	I_{CC}		60	90	mA	All inputs 5.25V Data Out Open
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC} + 1.0V	V	
Output "Low" Voltage	V_{OL}			0.40	V	3.2 mA
Output "High" Voltage	V_{OH}	2.4			V	−200 μA

Note: ① Typical Values for T_a = 25°C and nominal supply voltages.

CAPACITANCE

T_a = 25°C; f = 1 MHz

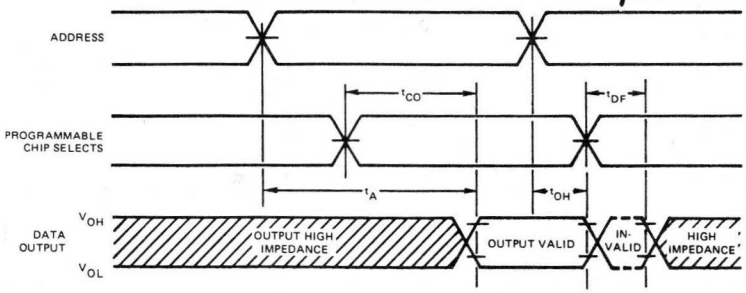
PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}			15	pF	All Pins Except Pin Under Test Tied to AC Ground

AC CHARACTERISTICS

T_a = −10°C to +70°C, V_{CC} = +5V ± 10%; unless otherwise specified.

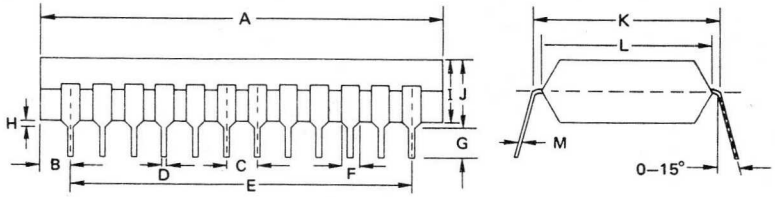
PARAMETER	SYMBOL	LIMITS μPD2332A/B MIN.	LIMITS μPD2332A/B MAX.	LIMITS μPD2332A/B-1 MIN.	LIMITS μPD2332A/B-1 MAX.	UNIT	TEST CONDITIONS
Address to Output Delay Time	t_{ACC}		450		350	ns	t_T = t_r = t_f = 20 ns
Chip Select to Output Enable Delay Time	t_{CO}		150		150	ns	C_L = 100 pF
Chip Deselect to Output Data Float Delay Time	t_{DF}	0	150		100	ns	Load = 1TTL gate
Output Hold Time	t_{OH}	20		20		ns	V_{IN} = 0.8 to 2V V_{ref} Input = 1.5V V_{ref} Output = 0.45/2.2V

TIMING WAVEFORMS



PACKAGE OUTLINE

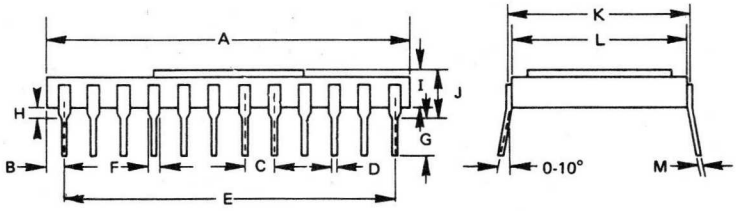
μPD2332C
μPD2332AC
μPD2332BC



Plastic

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.55 MAX
M	$0.25\ ^{+0.10}_{-0.05}$	$0.01\ ^{+0.004}_{-0.0019}$

μPD2332D
μPD2332AD
μPD2332BD



Ceramic

ITEM	MILLIMETERS	INCHES
A	30.78 MAX.	1.23 MAX.
B	1.53 MAX.	0.07 MAX.
C	2.54 ± 0.1	0.10 ± 0.004
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94 ± 0.1	1.10 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.125 MIN.
H	1.02 MIN.	0.04 MIN.
I	3.23 MAX.	0.13 MAX.
J	4.25 MAX.	0.17 MAX.
K	15.24 TYP.	0.60 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.010 ± 0.002

FULLY DECODED 65,536 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPD2364 is a high-speed 65,536 bit mask programmable Read Only Memory organized as 8,192 words by 8 bits. The μPD2364 is fabricated with N-channel MOS technology.

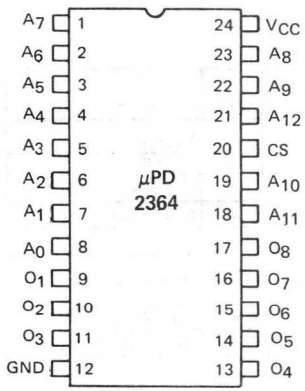
The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The chip select input is programmable. Any combination of active high or low level chip select inputs can be defined and the desired chip select code is fixed during the masking process.

4

FEATURES

- 8,192 Words x 8-Bits Organization
- Directly TTL Compatible – All Inputs and Outputs
- Single +5V Power Supply
- High Speed – Access Time 450 ns Max.
- Three-State Output – OR-Tie Capability
- One Programmable Chip Select Input for Easy Memory Expansion
- On-Chip Address Fully Decoded
- All Inputs Protected Against Static Charge
- Pin Compatible with MK36000
- Available in 24 Pin Ceramic or Plastic Dual-in-Line Package

PIN CONFIGURATION

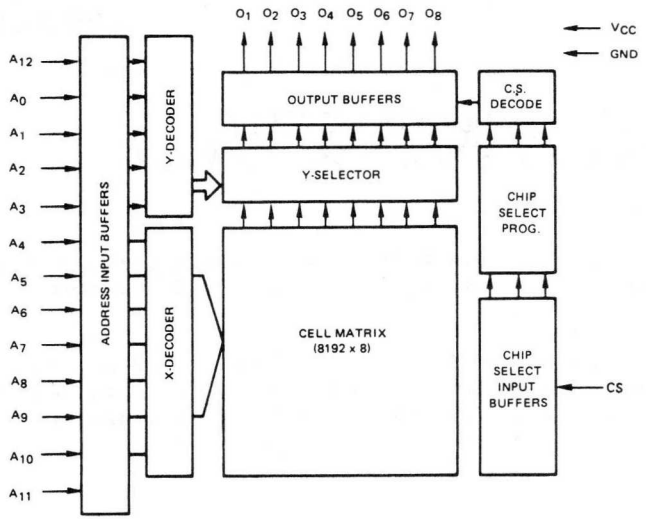


PIN NAMES

$A_0 - A_{12}$	Address Inputs
$O_1 - O_8$	Data Outputs
CS	Programmable Chip Select Input

Rev/2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Supply Voltage On Any Pin . . . . . −0.5 to +7.0 Volts (1)

Note: (1) With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{CC} = +5V ± 10%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP (1)	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			+10	μA	$V_{IN} = V_{CC}$
				−10	μA	V_{IN} = 0V
Output Leakage Current	I_{LOH}			+10	μA	Chip Deselected, $V_O = V_{CC}$
Output Leakage Current	I_{LOL}			−10	μA	Chip Deselected, V_O = 0V
Power Supply Current	I_{CC}		80	140	mA	
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC} + 1.0V	V	
Output "Low" Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output "High" Voltage	V_{OH}	2.2			V	I_{OH} = −400 μA

Note: (1) Typical Values for T_a = 25°C and nominal supply voltages.

CAPACITANCE

$T_a = 25°C$; f = 1 MHz

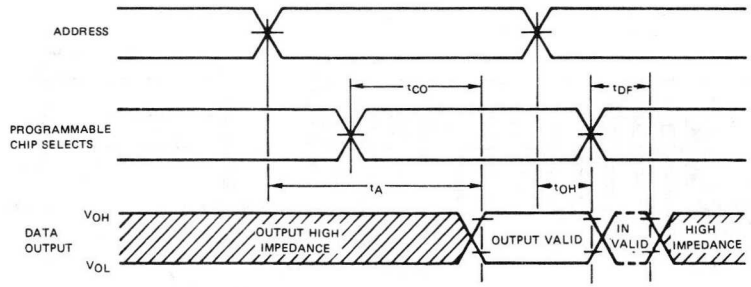
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}			15	pF	All Pins Except Pin Under Test Tied to AC Ground

AC CHARACTERISTICS

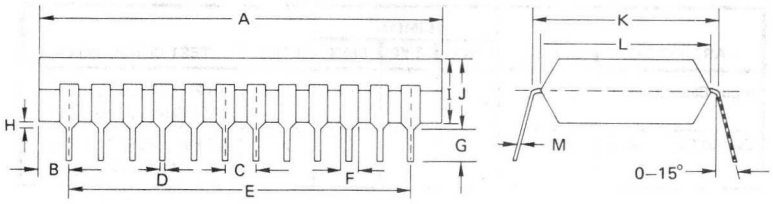
$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$ unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address to Output Delay Time	t_A			450	ns	$t_T = t_r = t_f = 20$ ns
Chip Select to Output Enable Delay Time	t_{CO}			150	ns	$C_L = 100$ pF
Chip Deselect to Output Data Float Delay Time	t_{DF}	0		150	ns	Load = 1TTL gate
Output Hold Time	t_{OH}	20			ns	$V_{IN} = 0.8$ to 2V V_{ref} Input = 1.5V V_{ref} Output = 0.8 to 2.0V

TIMING WAVEFORMS



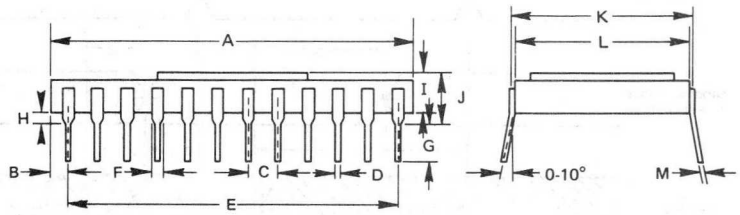
PACKAGE OUTLINE
μPD2364C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	33 MAX.	1.3 MAX.
B	2.53 MAX.	0.1 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94 ± 0.1	1.1 ± 0.004
F	1.5 MIN.	0.059 MIN.
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24 TYP.	0.6 TYP.
L	13.2 TYP.	0.52 TYP.
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPD2364D



(CERAMIC)

ITEM	MILLIMETERS	INCHES
A	30.78 MAX.	1.21 MAX.
B	1.53 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.10 ± 0.004
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94 ± 0.1	1.10 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.02 MIN.	0.04 MIN.
I	3.23 MAX.	0.13 MAX.
J	4.25 MAX.	0.17 MAX.
K	15.24 TYP.	0.60 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.010 ± 0.002

FULLY DECODED 128K BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPD23128 is a high speed 128K bit mask programmable Read Only Memory organized as 16,384 words by 8 bits. The μPD23128 is fabricated with N-channel MOS technology.

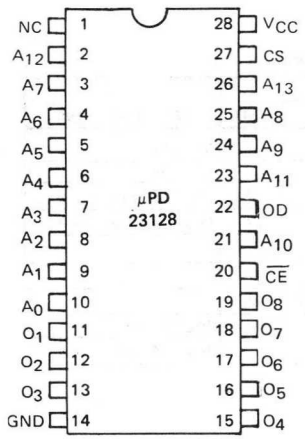
The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The chip select input is programmable. An active high or low level chip select input can be defined and is fixed during the masking process.

4

FEATURES

- 16,384 Words x 8 Bits Organization
- Directly TTL Compatible – All Inputs and Outputs
- Single +5V Power Supply
- High Speed – Access Time 250 ns Max.
- Three-State Output – OR-Tie Capability
- One Programmable Chip Select Input for Easy Memory Expansion
- On-Chip Address Fully Decoded
- All Inputs Protected Against Static Charge
- Pin Compatible with 2764
- Available in 28 Pin Ceramic or Plastic Dual-in-Line Package

PIN CONFIGURATION



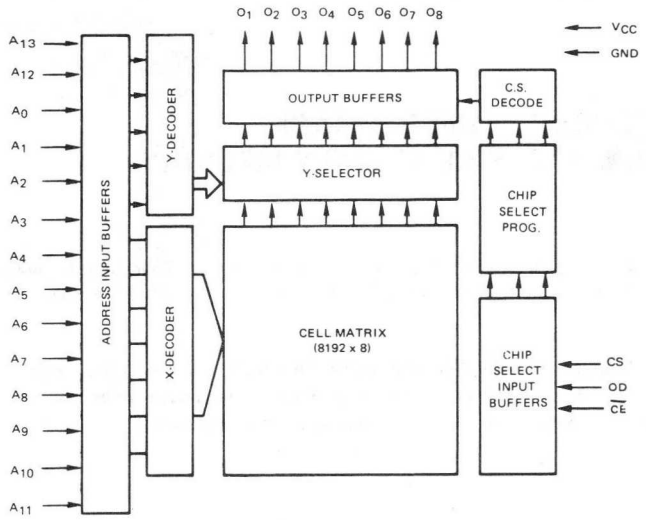
PIN NAMES

$A_0 - A_{13}$	Address Inputs
$O_1 - O_8$	Data Outputs
CS	Programmable Chip Select
OD	Output Disable
$\overline{CE}$	Chip Enable

Rev/1

μPD23128

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Supply Voltage On Any Pin . . . . . −0.5 to +7.0 Volts (1)

Note: (1) With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{CC} = +5V ± 10%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP (1)	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			+10	μA	$V_{IN} = V_{CC}$
				−10	μA	V_{IN} = 0V
Output Leakage Current	I_{LOH}			+10	μA	Chip Deselected, $V_O = V_{CC}$
Output Leakage Current	I_{LOL}			−10	μA	Chip Deselected, V_O = 0V
Power Supply Current	I_{CC}			100	mA	
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC} + 1.0V	V	
Output "Low" Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output "High" Voltage	V_{OH}	2.2			V	I_{OH} = −400 μA

Note: (1) Typical Values for T_a = 25°C and nominal supply voltages.

CAPACITANCE

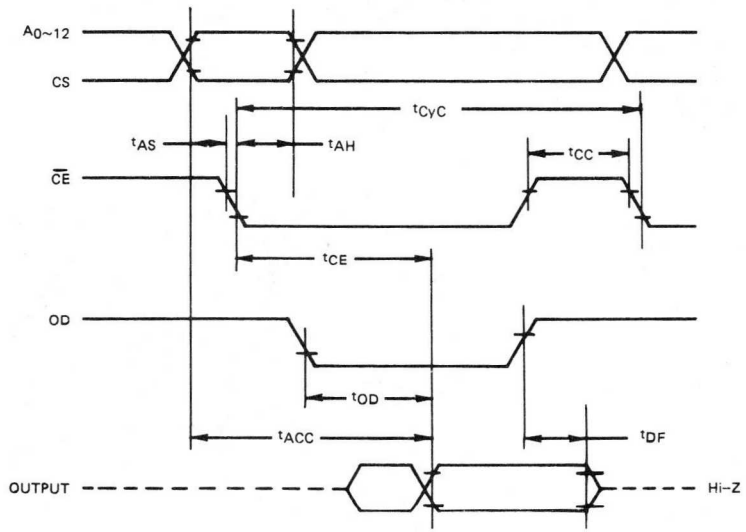
T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}			15	pF	All Pins Except Pin Under Test Tied to AC Ground

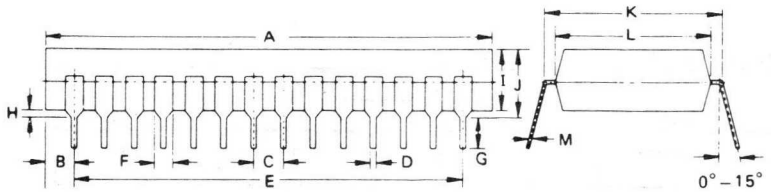
AC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Cycle Time	t_{CYC}	350			ns	
Address Setup Time Referenced to $\overline{CE}$	t_{AS}	0			ns	
Address Hold Time Referenced to $\overline{CE}$	t_{AH}	50			ns	
$\overline{CE}$ Pulse Width	t_{CE}			250	ns	
OD Pulse Width	t_{OD}			120	ns	
Access Time	t_{ACC}			250	ns	t_{AS} = 0 ns
$\overline{CE}$ Precharge Time	t_{CC}	100			ns	
Output Turn-Off Delay	t_{DF}	0		70	ns	

TIMING WAVEFORMS



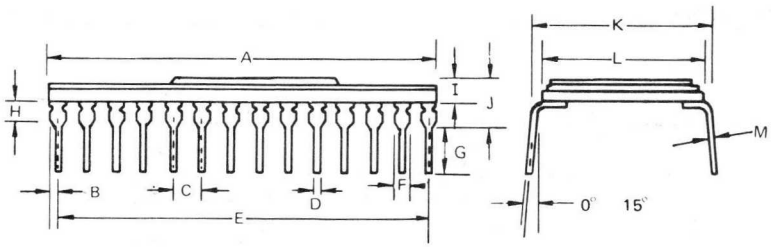
PACKAGE OUTLINE
μPD23128C



Plastic

ITEM	MILLIMETERS	INCHES
A	33 MAX.	1.3 MAX.
B	2.53 MAX.	0.1 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94 ± 0.1	1.1 ± 0.004
F	1.5 MIN.	0.059 MIN.
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24 TYP.	0.6 TYP.
L	13.2 TYP.	0.52 TYP.
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPD23128D



Ceramic

ITEM	MILLIMETERS	INCHES
A	30.78 MAX.	1.21 MAX.
B	1.53 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.10 ± 0.004
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94 ± 0.1	1.10 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.02 MIN.	0.04 MIN.
I	3.23 MAX.	0.13 MAX.
J	4.25 MAX.	0.17 MAX.
K	15.24 TYP.	0.60 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.010 ± 0.002

4096-BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

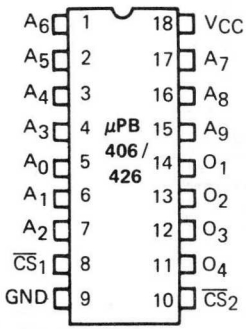
DESCRIPTION

The μPB406 and μPB426 are high-speed, electrically programmable, fully-decoded 4096-bit TTL read-only memories. On-chip address decoding, two chip-enable inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB406 and μPB426 are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 1024 WORD X 4 BIT Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time: 50 ns max. (μPB406-2, μPB426-2)
- Medium Power Consumption: 500 mW TYP.
- Two Chip Select Inputs for Memory Expansion
- Open-Collector Output (μPB406)/Three-State Outputs (μPB426)
- Ceramic and Plastic 18-Lead Dual In-Line Packages
- Fast Programming Time: 200 μs/bit TYP.
- Compatibility with: HPROM HM-7642/7643 type and Equivalent Devices (as a ROM)
- A.I.M. (Avalanche Induced Migration) Technology

PIN CONFIGURATION



PIN NAMES

A_0-A_9	Address Inputs
O_1-O_4	Data Outputs
$\overline{CS_1}$, $\overline{CS_2}$	Chip Selects
V_{CC}	Power (+5V)
GND	Ground

OPERATION

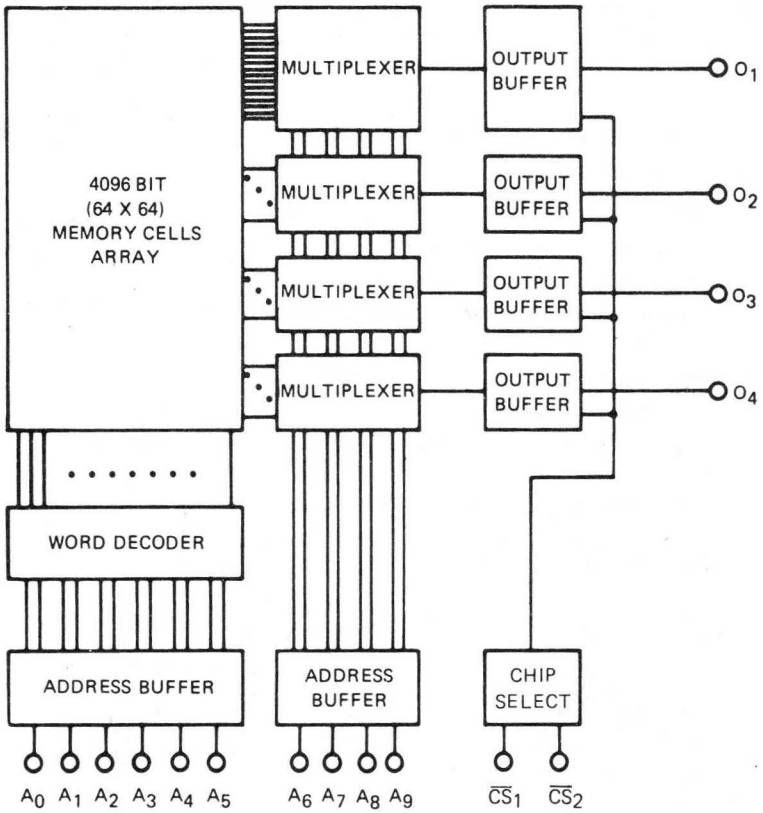
Programming

A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First, the desired word is selected by the ten address inputs in TTL levels. Either or both of the two chip select inputs must be at a logic one (high). Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

Reading

To read the memory, both of the two chip select inputs should be held at logic zero (low). The outputs then correspond to the data programmed in the selected words. When either or both of the two chip select inputs are at logic one (high), all the outputs will be high (floating).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-25°C to +75°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.5 to +5.5 Volts
All Input Voltages	-0.5 to +5.5 Volts
Supply Voltage V_{CC}	-0.5 to +7.0 Volts
Output Currents	50 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB406 and μPB426. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

A typical programming operation is performed by first sensing, then programming, then sensing again to see if the word to be programmed has reached the desired state. Either or both of the two chip enable inputs must be at a logic one (high).

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The sense measurement is to ensure that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic "1" (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. This current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process is continued until that location is altered to the "1" state. A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse pass the limit. When this condition has been met, four additional pulses are applied, then the sense current is terminated.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate (both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty Cycle	70% MIN.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate	70 MAX.	V/μs	15V point/ 150Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum Sensed Voltage for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

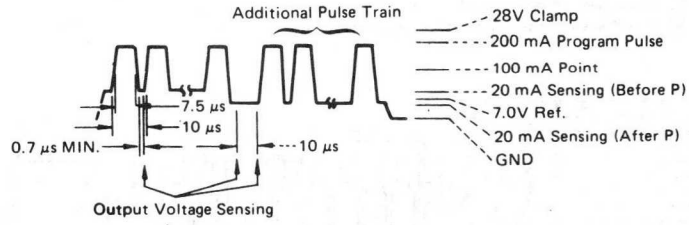


Figure 2 – Typical Output Voltage Waveform

DC CHARACTERISTICS

T_a = 0°C to +75°C, V_{CC} = 4.75V to 5.25V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IL}			40	μA	V_I = 2.7V
Input Low Current	$-I_{IL}$			0.5	mA	V_I = 0.4V
Output Low Voltage	V_{OL}			0.45	V	I_O = 16 mA
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.25V
Output Leakage Current	$-I_{OFF2}$	40			μA	V_O = 0.4V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I = −12 mA
Power Supply Current	I_{CC}		100	150	mA	All Inputs Grounded
Output High Voltage①	V_{OH}	2.4			V	I_O = −2.4 mA
Output Short Circuit Current①	$-I_{SC}$	15		60	mA	V_O = 0V

NOTE: ① Applicable to μPB426 only.

CAPACITANCE

T_a = 25°C, f = 1 MHz, V_{CC} = 5V, V_{IN} = 2.5V

CHARACTERISTICS	SYMBOL	MIN	MAX	UNIT
Input Capacitance	C_{IN}		8	pF
Output Capacitance	C_{OUT}		10	pF

AC CHARACTERISTICS

T_a = 0°C to +75°C, V_{CC} = 4.75V to 5.25V

PARAMETER	SYMBOL	μPB406/426		μPB406/426-1		μPB406/426-2		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
Address Access Time	t_{AA}		70		60		50	ns	①②③④
Chip Select Access Time	t_{ACS}		45		40		30	ns	
Chip Select Disable Time	t_{DCS}		45		40		30	ns	

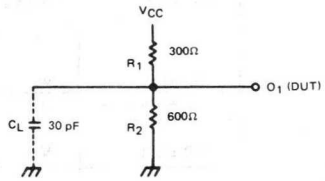


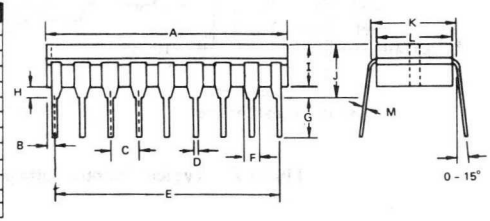
Figure 1

Notes: ① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10 ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

PACKAGE OUTLINE μPB406/426D

CERDIP

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.05
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01



NEC

μPB409
μPB429
μPB409-1
μPB429-1
μPB409-2
μPB429-2

2048 WORD BY 8 BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

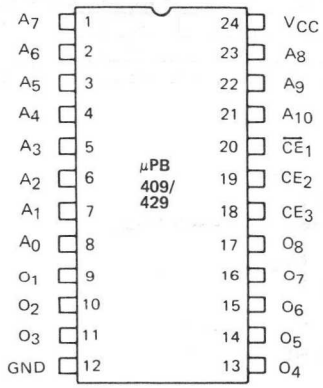
DESCRIPTION

The μPB409 and μPB429 are high-speed, electrically programmable, fully-decoded 16384 bit TTL read only memories. On-chip address decoding, three chip enable inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB409 and μPB429 are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 2048 WORDS x 8 BITS Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time :50 ns MAX
- Medium Power Consumption :500 mW TYP
- Three Chip Enable Inputs for Memory Expansion
- Open-Collector Outputs (μPB409)
- Three-State Outputs (μPB429)
- Ceramic 24-Lead Dual In-Line Package (μPB409D, μPB429D)
- Plastic 24-Lead Dual In-Line Package (μPB409C, μPB429C)
- Fast Programming Time :200 μs/bit TYP
- Replaceable with :82S190/191
  HM76160/76161, 3636
  and Equivalent Type Devices

PIN CONFIGURATION



PIN NAMES

A_0-A_{10}	Address Inputs
CE_1-CE_3	Chip Enable Inputs
O_1-O_8	Data Outputs

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . -0.5 to +7.0V
Input Voltage . . . . . -0.5 to +5.5V
Output Voltage . . . . . -0.5 to +5.5V
Output Current . . . . . 50 mA
Operating Temperature . . . . . -25°C to +75°C
Storage Temperature
Ceramic Package . . . . . -65°C to +150°C
Plastic Package . . . . . -55°C to +125°C

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 75°C, V_{CC} = 4.5 to 5.5V

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.85	V	
Input High Current	I_{IH}			40	μA	V_I=5.5V, V_{CC}=5.5V
Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4V, V_{CC}=5.5V
Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA, V_{CC}=4.5V
Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5V, V_{CC}=5.5V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4V, V_{CC}=5.5V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I=-18 mA, V_{CC}=4.5V
Power Supply Current	I_{CC}		100	160	mA	All inputs Grounded, V_{CC}=5.5V
Output High Voltage*	V_{OH}	2.4			V	I_O=-2.4 mA, V_{CC}=4.5V
Output Short Circuit Current*	$-I_{SC}$	20		70	mA	V_O=0V

*Note: Applicable to μPB429

CAPACITANCE

T_a = 25°C, f = 1 MHz, V_{CC} = 5V, V_{IN} = 2.5V

CHARACTERISTICS	SYMBOL	MIN	MAX	UNIT
Input Capacitance	C_{IN}		8	pF
Output Capacitance	C_{OUT}		10	pF

AC CHARACTERISTICS

T_a = 0°C to 75°C, V_{CC} = 4.5 to 5.5V ①②③④

CHARACTERISTIC	SYMBOL	μPB409-2, μPB429-2		μPB409-1, μPB429-1		μPB409, μPB429		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Address Access Time	t_{AA}		50		60		70	ns
Chip Enable Access Time	t_{ACE}		30		40		50	ns
Chip Enable Disable Time	t_{DCE}		30		40		50	ns

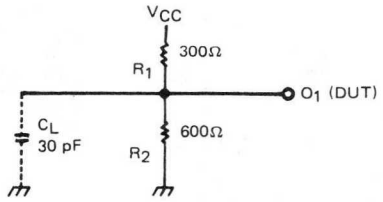


FIGURE 1

NOTES: ① Output Load: See Fig. 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Fig. 1 includes jig and probe stray capacitances.

OPERATION

You can program only when the outputs are disabled by any one of the chip enable inputs. This insures that the output will not be damaged when you apply programming voltages.

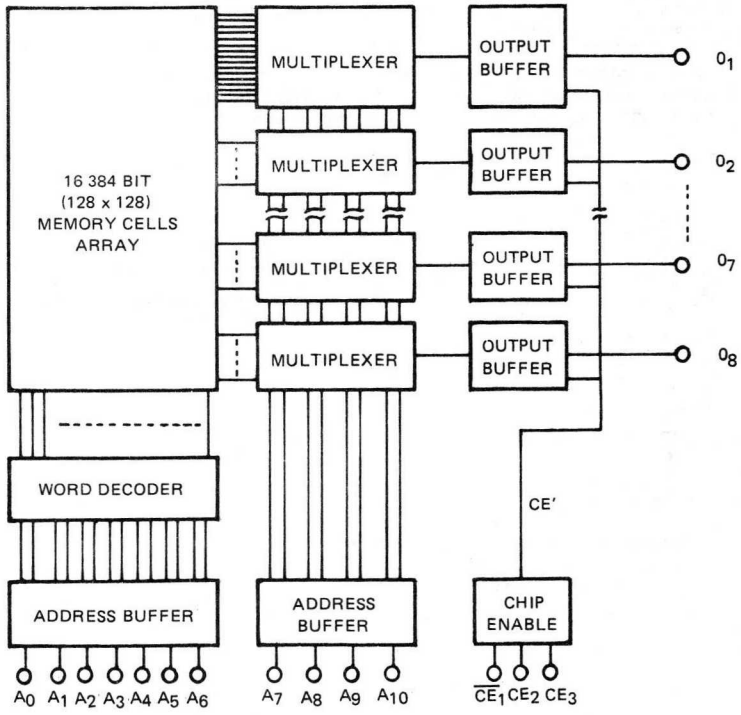
Programming

You can permanently program a logic one into a selected bit location by using special equipment (programmer). First, disable the chip as described above. Second, apply a train of high-current programming pulses to the desired output. Apply an additional pulse train after the sensed voltage indicates that the selected bit is in the logic one state. Then, stop the pulse train.

Reading

To read the memory, enable the chip (i.e., $CE_1 = 0, CE_2 = CE_3 = 1$). The outputs then correspond to the data programmed into the selected words. When the chip is disabled, all the outputs will be in a high impedance (floating) state.

LOGIC DIAGRAM



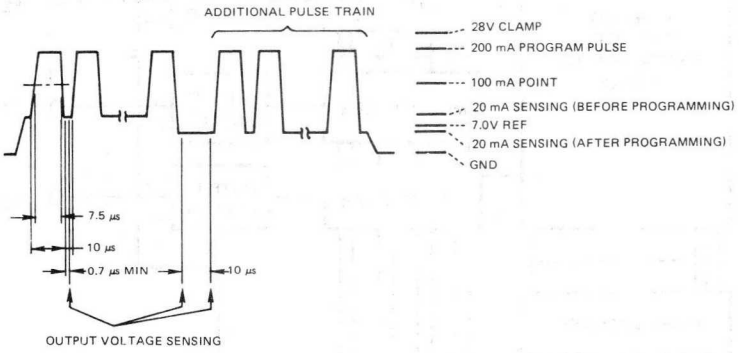
PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB409 and μPB429. NEC will not accept responsibility for any device found to be defective if it was not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% – 2%	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/150Ω load
Duty Cycle	70% MIN		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% – 2%	V	
Ramp Rate	70 MAX	V/μs	15V point/150Ω load
Sense Current Interruption before and after address change	10 MIN	μs	
Programming V_{CC}	5.0 + 5% – 0%	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN	μs	

*A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse pass the limit. When this condition has been met, four additional pulses are applied, then the sense current is terminated.

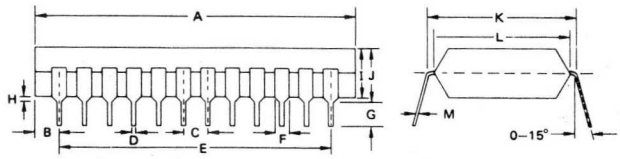
TYPICAL OUTPUT VOLTAGE WAVEFORM



COMMERCIALLY AVAILABLE PROGRAMMING EQUIPMENT:

DATA I/O: PROGRAM CARD 909/919-1555
WITH SOCKET ADAPTER 715-1033

PACKAGE OUTLINE
μPB409C/429C

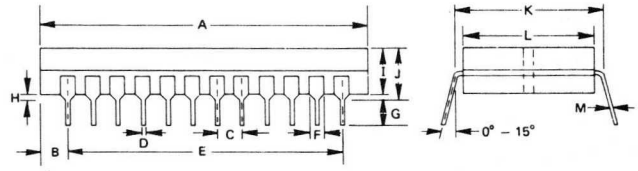


(Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

4

μPB409D/429D



(Cerdip)

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

16,384 (2K X 8) BIT UV ERASABLE PROM

DESCRIPTION

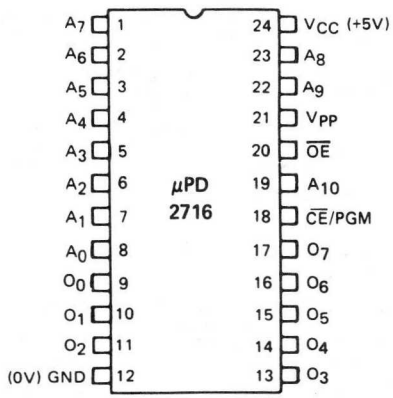
The μPD2716 is a 16,384 bit (2048 x 8 bit) Ultraviolet Erasable and Electrically Programmable Read-Only Memory (EPROM). It operates from a single +5 volt supply, making it ideal for microprocessor applications. It offers a standby mode with an attendant 75% savings in power consumption, and is compatible with the μPD2316E as a ROM. This allows for economical change-over to a masked ROM for production quantities, where desired.

The μPD2716 features fast, simple one pulse programming controlled by TTL level signals. Total programming time for all 16,384 bits is only 100 seconds.

FEATURES

- Ultraviolet Erasable and Electrically Programmable
- Access Time – 450 ns Max
- Single Location Programming
- Programmable with Single Pulse
- Low Power Dissipation Standby Mode
- Input/Output TTL Compatible for Reading and Programming
- Pin Compatible to μPD2316E (16K ROM)
- Single +5V Power Supply
- 24 Pin Ceramic DIP
- Three-State Outputs

PIN CONFIGURATION



PIN NAMES

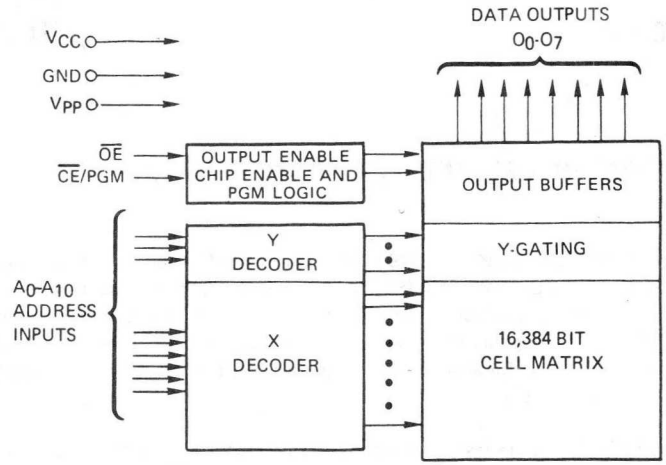
A_0-A_{10}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs
$\overline{CE}$/PGM	Chip Enable/Program

TABLE 1. MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

V_{IH} and V_{IL} are TTL high level ("1") and TTL low level ("0") respectively.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +80°C
Storage Temperature	-65°C to +125°C
Output Voltage	-0.3 to +6 Volts
Input Voltage	-0.3 to +6 Volts
Supply Voltage V_{CC}	-0.3 to +6 Volts
Supply Voltage V_{PP}	-0.3 to +26.5 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0V

DC CHARACTERISTICS

READ MODE AND STANDBY MODE

T_a = 0°C ~ 70°C; V_{CC} ① = +5V ± 5%; V_{PP} ①② = V_{CC} ± 0.6V ③

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input High Voltage	V_{IN}	2.0		V_{cc} +1	V	
Input Low Voltage	V_{IL}	-0.1		0.8	V	
Output Leakage Current	I_{LO}			10	μA	V_{OUT} = 5.25V
Input Leakage Current	I_{IL}			10	μA	V_{IN} = 5.25V
V_{PP} Current	I_{PP1}			5	mA	V_{PP} = 5.85V
V_{CC} Current ②	I_{CC1}		10	25	mA	$\overline{CE}/PGM = V_{IH}$ $\overline{OE} = V_{IL}$ Standby Mode
	I_{CC2}		57	100	mA	$\overline{CE}/PGM = V_{IL}$ $\overline{OE} = V_{IL}$ Read Mode

Notes: ① V_{CC} must be applied simultaneously or before V_{PP} and removed after V_{PP}.

② V_{PP} may be connected directly to V_{CC} (+5V) at read mode and standby mode. The supply current would then be the sum of I_{PP1} and I_{CC} (I_{CC1} or I_{CC2}).

③ The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from +25V to +5V.

DC CHARACTERISTICS (CONT.)

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C; V_{CC} ① = +5V ± 5%; V_{PP} ①④ = +25V ± 1V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.0		V_{CC}+1	V	
Input Low Voltage	V_{IL}	-0.1		0.8	V	
Input Leakage Current	I_{IL}			10	μA	V_{IN} = 5.25V/0.45V
V_{PP} Current	I_{PP1}			5	mA	$\overline{CE}/PGM = V_{IL}$ Program Verify / Program Inhibit
	I_{PP2}			30	mA	$\overline{CE}/PGM = V_{IH}$ Program Mode
V_{CC} Current'	I_{CC}			100	mA	

AC CHARACTERISTICS

READ MODE AND STANDBY MODE

T_a = 0°C to +70°C; V_{CC} ① = +5V ± 5%; V_{PP} ①② = V_{CC} ± 0.6V ③

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address to Output Delay	t_{ACC}			450	ns	$\overline{CE}/PGM = \overline{OE} = V_{IL}$
$\overline{CE}/PGM$ to Output Delay	t_{CE}			450	ns	$\overline{OE} = V_{IL}$
Output Enable to Output Delay	t_{OE}			120	ns	$\overline{CE}/PGM = V_{IL}$
Output Enable High to Output Float	t_{DF}	0		100	ns	$\overline{CE}/PGM = V_{IL}$
Address to Output Hold	t_{OH}	0			ns	$\overline{CE}/PGM = \overline{OE} = V_{IL}$

Test Conditions
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.8 to 2.2V
Timing Measurement Reference Level:
Inputs: 1.0V and 2.0V
Outputs: 0.8V and 2.0V

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C; V_{CC} ① = +5V ± 5%; V_{PP} ①④ = +25V ± 1V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
$\overline{OE}$ Hold Time	t_{OEH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Output Enable to Output Float Delay	t_{DF}	0		120	ns	$\overline{CE}/PGM = V_{IL}$
Output Enable to Output Delay	t_{OE}			120	ns	$\overline{CE}/PGM = V_{IL}$
Program Pulse Width	t_{PW}	45	50	55	ms	
Program Pulse Rise Time	t_{PRT}	5			ns	
Program Pulse Fall Time	t_{PFT}	5			ns	

Test Conditions:

Input Pulse Levels . . . . . 0.8V to 2.2V
Input Timing Reference Level. . . . . 1V and 2V
Output Timing Reference Level . . .0.8V and 2V

Notes: ① V_{CC} must be applied simultaneously or before V_{PP} and removed after V_{PP}.

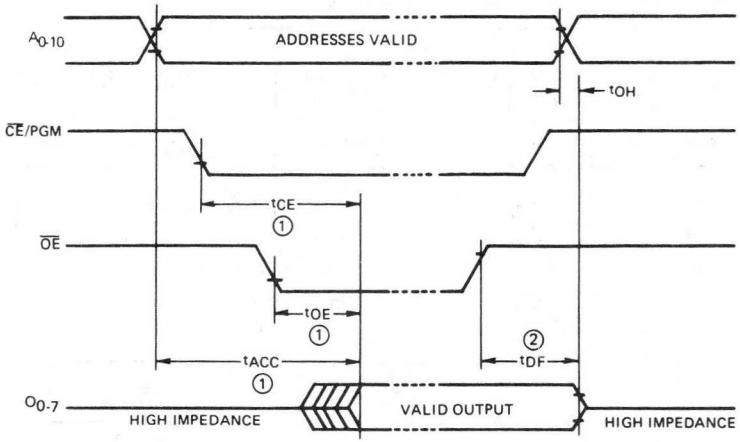
② V_{PP} may be connected directly to V_{CC} (+5V) at read mode and standby mode. The supply current would then be the sum of I_{PP1} and I_{CC} (I_{CC1} or I_{CC2}).

③ The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from +25V to +5V.

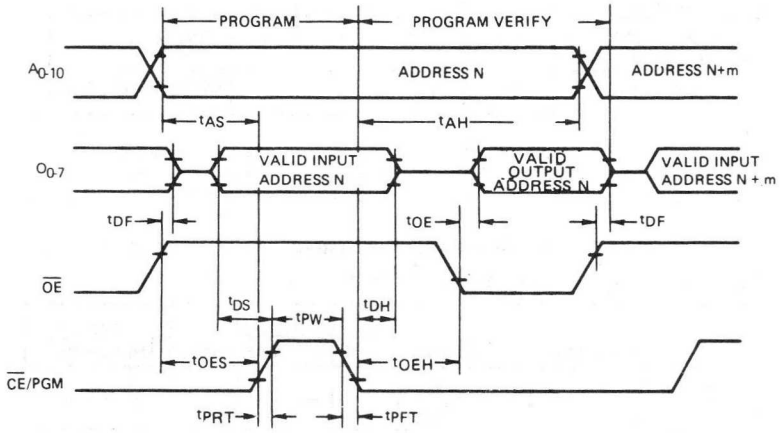
④ During programming, program inhibit, and program verify, a maximum of +26V should be applied to the V_{PP} pin. Overshoot voltages to be generated by the V_{PP} power supply should be limited to less than +26V.

TIMING WAVEFORMS

READ MODE



PROGRAM MODE



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$/PGM for read mode without impact on t_{ACC}

② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$/PGM, whichever occurs first.

FUNCTIONAL DESCRIPTION

The μPD2716 operates from a single +5V power supply and, accordingly, is ideal for use with +5V microprocessors such as μPD8085 and μPD8048/8748.

Programming of the μPD2716 is achieved with a single 50 ms TTL pulse. Total programming time for all 16,384 bits is only 100 sec. Due to the simplicity of the programming requirements, devices on boards and in systems may be programmed easily and without any special programmer.

The μPD2716 features a standby mode which reduces the power dissipation from a maximum active power dissipation of 525 mW to a maximum standby power dissipation of 132 mW. This results in a 75% savings with no increase in access time.

Erasure of the μPD2716 programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms (Å). It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD2716. Consequently, if the μPD2716 is to be exposed to these types of lighting conditions for long periods of time, the μPD2716 window should be masked to prevent unintentional erasure.

The recommended erasure procedure for the μPD2716 is exposure to ultraviolet light with wavelengths of 2,537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be not less than 15 W-sec/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000 μW/cm^2 power rating.

During erasure, the μPD2716 should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

OPERATION

The five operation modes of the μPD2716 are listed in Table 1. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply should be at +25V during programming, program verification and program inhibit, and it should be at +5V during read and standby. $\overline{CE}$/PGM, $\overline{OE}$ and V_{PP} select the operation mode as shown in Table 1.

READ MODE

When $\overline{CE}$/PGM and $\overline{OE}$ are at low (0) level with V_{PP} at +5V, the READ MODE is set and the data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

STANDBY MODE

The μPD2716 is placed in the standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$/PGM and a V_{PP} of +5V. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input. The active power dissipation is reduced by 75% from 525 mW to 132 mW.

PROGRAMMING MODE

Programming of the μPD2716 is commenced by erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD2716 is placed in the programming mode by applying a high (1) level TTL signal to the $\overline{OE}$ with V_{PP} at +25V. The data to be programmed is applied to the output pins 8 bits in parallel at TTL levels.

Any location can be programmed at any time, either individually, sequentially or at random.

When multiple μPD2716s are connected in parallel, except for $\overline{CE}$/PGM, individual μPD2716s can be programmed by applying a high (1) level TTL pulse to the $\overline{CE}$/PGM input of the desired μPD2716 to be programmed.

Programming of multiple μPD2716s in parallel with the same data is easily accomplished. All the alike inputs are tied together and are programmed by applying a high (1) level TTL pulse to the $\overline{CE}$/PGM inputs.

PROGRAMMING INHIBIT MODE

Programming of multiple μPD2716s in parallel with different data is rendered more easily by the program inhibit mode. Except for $\overline{CE}$/PGM, all alike inputs (including $\overline{OE}$) of the parallel μPD2716s may be common. Programming is accomplished by applying a TTL level program pulse to the μPD2716 $\overline{CE}$/PGM input with V_{PP} at +25V. A low level applied to the $\overline{CE}$/PGM of the other μPD2716 will inhibit it from being programmed.

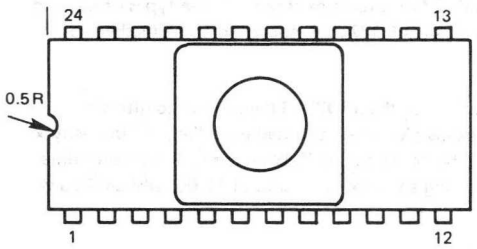
PROGRAM VERIFY MODE

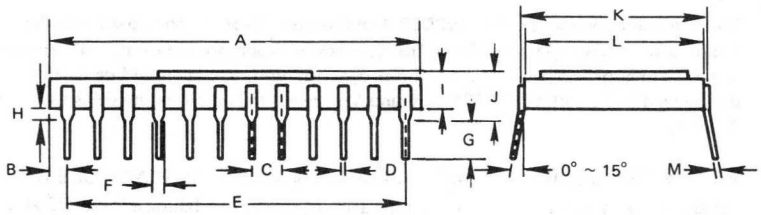
A verify should be performed on the programmed bits to determine that the data was correctly programmed on all bits of the μPD2716. The program verify can be performed with V_{PP} at +25V and $\overline{CE}$/PGM and $\overline{OE}$ at low (0) levels.

OUTPUT DESELECTION

The data outputs of two or more μPD2716s may be wire-ored together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD2716s should be deselected by raising the $\overline{OE}$ input to a TTL high.

PACKAGE OUTLINE μPD2716D





CERAMIC

ITEM	MILLIMETERS	INCH
A	33.5 MAX.	1.32 MAX.
B	2.78	1.1
C	2.54	0.1
D	0.46 ± 0.10	0.018 ± 0.004
E	27.94	1.10
F	1.3	0.05
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.020
I	5.0 MAX.	0.20
J	5.5 MAX.	0.216
K	15.24	0.60
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

2716DS-12-80-CAT

32,768 (4K X 8) BIT UV ERASABLE PROM

DESCRIPTION

The μPD2732 is a 32,768 bit (4096 x 8 bit) Ultraviolet Erasable and Electrically Programmable Read-Only Memory (EPROM). It operates from a single +5V supply, making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with an attendant 80% savings in power consumption.

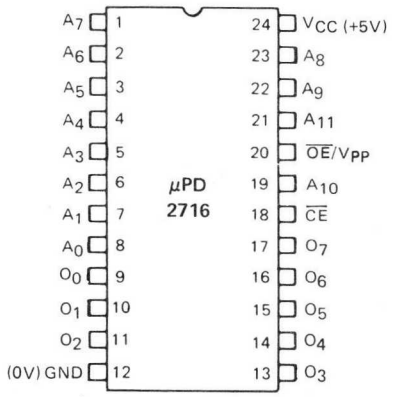
A distinctive feature of the μPD2732 is a separate output control, output enable ($\overline{OE}$) from the chip enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple-bus microprocessor systems. The μPD2732 features fast, simple one-pulse programming controlled by TTL-level signals. Total programming time for all 32,768 bits is only 210 seconds.

FEATURES

- Ultraviolet Erasable and Electrically Programmable
- Access Time – 450 ns Max
- Single Location Programming
- Programmable with Single Pulse
- Low Power Dissipation: 150 mA Max Active Current, 30 mA Max Standby Current
- Input/Output TTL Compatible for Reading and Programming
- Single +5V Power Supply
- 24 Pin Ceramic DIP
- Three-State Outputs

4

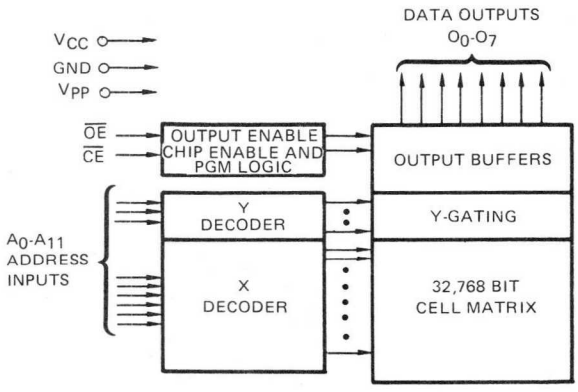
PIN CONFIGURATION



MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

BLOCK DIAGRAM



PIN NAMES

A_0-A_{11}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable

NOTES

9216 BIT FIELD PROGRAMMABLE LOGIC ARRAY

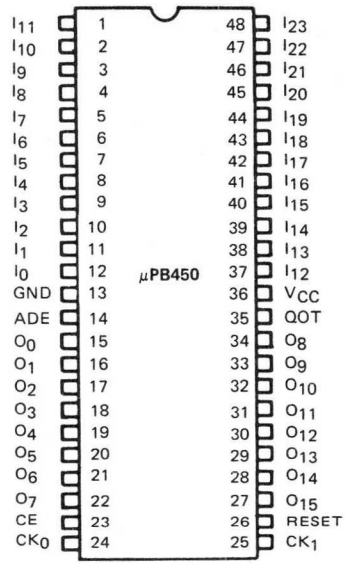
DESCRIPTION

The μPB450 is a bipolar, 9, 216-bit field programmable logic array. It includes 24 input and 16 output lines, 72 product terms, input 2-bit decoders, and 16-bit feedback registers. This provides an extremely versatile organization. Interconnection of internal AND-OR arrays is performed electrically by the proven, avalanche induced migration method which is widely used in NEC Bipolar PROM technology.

FEATURES

- 24 Input Terminals
- 16 Output Terminals with Latches
- 72 Product Terms
- 16 Feedback Loops with J-K Flip Flops
- 20 2704 Input Decoders
- 80 x 72 AND-Array Elements
- 72 x 48 OR-Array Elements
- Scan Path (Shift Register Mode) Capability of J-K Flip Flops
- TTL Compatible
- Single +5V Supply
- 48 Pin Ceramic Dual-In-Line Package

PIN CONFIGURATION



PIN NAMES

$I_0 \sim I_{23}$	Input
$O_0 \sim O_{15}$	Outputs
ADE	Mode Control
QOT	Shift Register Output (Mode 2)
CE	Output and Mode Control
CK0	Output Latch Control
CK1	Feed Back Register Clock
RESET	Feed Back Register Reset
V_{CC}	Power Supply (+5V)
GND	Ground

NOTES

MICROCOMPUTERS 5

NEC Microcomputers, Inc.

MICROCOMPUTER SELECTION GUIDE

SINGLE CHIP 4-BIT MICROCOMPUTERS

DEVICE	PRODUCT	ROM	RAM	I/O	PROCESS	OUTPUT	FEATURES	SUPPLY VOLTAGES	PINS
μPD546	μCOM-43	2000 x 8	96 x 4	35	PMOS	O.D.		−10	42
μPD553	μCOM-43H	2000 x 8	96 x 4	35	PMOS	O.D.	A	−10	42
μPD557L	μCOM-43SL	2000 x 8	96 x 4	21	PMOS	O.D.	A	−8	28
μPD650	μCOM-43C	2000 x 8	96 x 4	35	CMOS	push-pull		+5	42
μPD547	μCOM-44	1000 x 8	64 x 4	35	PMOS	O.D.		−10	42
μPD547L	μCOM-44L	1000 x 8	64 x 4	35	PMOS	O.D.		−8	42
μPD552	μCOM-44H	1000 x 8	64 x 4	35	PMOS	O.D.	A	−10	42
μPD651	μCOM-44C	1000 x 8	64 x 4	35	CMOS	push-pull		+5	42
μPD550	μCOM-45	640 x 8	32 x 4	21	PMOS	O.D.	A	−10	28
μPD550L	μCOM-45L	640 x 8	32 x 4	21	PMOS	O.D.	A	−8	28
μPD554	μCOM-45	1000 x 8	32 x 4	21	PMOS	O.D.	A	−10	28
μPD554L	μCOM-45L	1000 x 8	32 x 4	21	PMOS	O.D.	A	−8	28
μPD652	μCOM-45C	1000 x 8	32 x 4	21	CMOS	push-pull		+5	28
μPD556	μCOM-43	External	96 x 4	35	PMOS	O.D.	C	−10	64
μPD7500	μCOM-75	External	256 x 4	46	CMOS	O.D.	D	+2.7 to 5.5	64
μPD7502	μCOM-75	2000 x 8	128 x 4	23	CMOS	O.D.	E	+2.7 to 5.5	64
μPD7503	μCOM-75	4000 x 8	224 x 4	23	CMOS	O.D.	E	+2.7 to 5.5	64
μPD7507	μCOM-75	2000 x 8	128 x 4	32	CMOS	O.D.	E	+2.7 to 5.5	40
μPD7520	μCOM-75	768 x 8	48 x 4	24	PMOS	O.D.	B	−6 to −10 variable	28

Notes: A = −35V VF Drive
B = μCOM-4 Evaluation Chip
C = μCOM-75 Evaluation Chip
D = LCD Controller
E = LED Display Controller
O.D. = Open Drain

SINGLE CHIP 8-BIT MICROPROCESSORS

DEVICE	SPECIAL FEATURES	ROM	RAM	I/O	PROCESS	OUTPUT	CYCLE	SUPPLY VOLTAGES	PINS
μPD8021	Zero-Cross Detector	1024 x 8	64 x 8	21	NMOS	BD	3.6 MHz	+5V	28
μPD8022	On-Chip S/D Converter	2048 x 8	64 x 8	26	NMOS	BD	3.6 MHz	+5V	40
μPD8035L	μPD8048 w/External Memory	External	64 x 8	27	NMOS	TS, BD	6 MHz	+5V	40
μPD8039L	μPD8049 w/External Memory	External	128 x 8	27	NMOS	TS, BD	11 MHz	+5V	40
μPD8041	Peripheral Interface w/Slave Bus	1024 x 8	64 x 8	18	NMOS	TS, BD	6 MHz	+5V	40
μPD8041A	Enhanced μPD8041	1024 x 8	64 x 8	18	NMOS	TS, BD	6 MHz	+5V	40
μPD8048	Expansion Bus	1024 x 8	64 x 8	27	NMOS	TS, BD	6 MHz	+5V	40
μPD8049	High Speed μPD8048	2048 x 8	128 x 8	27	NMOS	TS, BD	11 MHz	+5V	40
μPD8741A	UV-EPROM μPD8041A	1024 x 8	64 x 8	18	NMOS	TS, BD	6 MHz	+5V	40
μPD8748	UV-EPROM μPD8048	1024 x 8	64 x 8	27	NMOS	TS, BD	6 MHz	+5V	40
μPD7800	Development Chip	External	128 x 8	48	NMOS	TS, BD	4 MHz	+5V	64
μPD7801	8080 Type Expansion Bus 64K Memory Address Space	4096 x 8	128 x 8	48	NMOS	TS, BD	4 MHz	+5V	64
μPD7802	Expanded μPD7801	6144 x 8	64 x 8	48	NMOS	TS, BD	4 MHz	+5V	64

MICROPROCESSORS

DEVICE	PRODUCT	SIZE	PROCESS	OUTPUT	CYCLE	SUPPLY VOLTAGES	PINS
μPD780	Microprocessor	8-bit	NMOS	3-State	4.0 MHz	+5	40
μPD8080AF	Microprocessor	8-bit	NMOS	3-State	2.0 MHz	+12 ± 5	40
μPD8080AF-2	Microprocessor	8-bit	NMOS	3-State	2.5 MHz	+12 ± 5	40
μPD8080AF-1	Microprocessor	8-bit	NMOS	3-State	3.0 MHz	+12 ± 5	40
μPD8085A	Microprocessor	8-bit	NMOS	3-State	3.0 MHz	+5	40
μPD8085A-2	Microprocessor	8-bit	NMOS	3-State	5.0 MHz	+5	40
μPD8086	Microprocessor	16-bit	NMOS	3-State	5.0 MHz	+5	40

NEC Microcomputers, Inc.

MICROCOMPUTER SELECTION GUIDE

SYSTEM SUPPORT

DEVICE	PRODUCT	SIZE	PROCESS	OUTPUT	CYCLE	SUPPLY VOLTAGES	PINS
μPD765	Double Sided/Double Density Floppy Disk Controller	8-bit	NMOS	3-State	8 MHz	+5	40
μPD781	Dot Matrix Printer Controller-Epson 500 Printer	8-bit	NMOS	3-State	6 MHz	+5	40
μPD782	Dot Matrix Printer Controller-Epson 200 Printer	8-bit	NMOS	3-State	6 MHz	+5	40
μPD3301	CRT Controller	8-bit	NMOS	3-State	3 MHz	+5	40
μPD7001	8-Bit A/D Converter	8-bit	CMOS	Open Collector Serial	10 kHz Conversion Time	+5	16
μPD7002	12-Bit A/D Converter	8-bit	CMOS	3-State	400 Hz Conversion Time	+5	28
μPD7201	Multi-Protocol Serial Controller	8-bit	NMOS	3-State	3 MHz	+5	40
μPD7210	IEEE Controller (Talker, Listener, Controller)	8-bit	NMOS	3-State	8 MHz	+5	40
μPD7220	Graphic Display Controller	8-bit	NMOS	3-State	6 MHz	+5	40
μPD7225	Alpha Numeric LCD Controller	8-bit	CMOS	–	–	+5	52
μPD7227	Dot Matrix LCD Controller	8-bit	CMOS	–	–	+5	64
μPD7720	Signal Processor	16-bit	NMOS	3-State	8 MHz	+5	28
μPD8155	256 x 8 RAM with I/O Ports and Timer	8-bit	NMOS	3-State	–	+5	40
μPD8155-2	256 x 8 RAM with I/O Ports and Timer	8-bit	NMOS	3-State	–	+5	40
μPD8156	256 x 8 RAM with I/O Ports and Timer	8-bit	NMOS	3-State	–	+5	40
μPD8156-2	256 x 8 RAM with I/O Ports and Timer	8-bit	NMOS	3-State	–	+5	40
μPB8212	I/O Port	8-bit	Bipolar	3-State	–	+5	24
μPB8214	Priority Interrupt Controller	3-bit	Bipolar	Open Collector	3 MHz	+5	24
μPB8216	Bus Driver Non-Inverting	4-bit	Bipolar	3-State	–	+5	16
μPB8224	Clock Generator Driver	2 phase	Bipolar	High Level Clock	3 MHz	+12 ± 5	16
μPB8226	Bus Driver Inverting	4-bit	Bipolar	3-State	–	+5	16
μPB8228	System Controller	8-bit	Bipolar	3-State	–	+5	28
μPD8243	I/O Expander	4 x 4 bits	NMOS	3-State	–	+5	24
μPD8251	Programmable Communications Interface (Async/Sync)	8-bit	NMOS	3-State	A-9.6K baud S-56K baud	+5	28
μPD8251A	Programmable Communications Interface (Async/Sync)	8-bit	NMOS	3-State	A-9.6K baud S-64K baud	+5	28
μPD8253	Programmable Timer	8-bit	NMOS	3-State	3.3 MHz	+5	24
μPD8253-5	Programmable Timer	8-bit	NMOS	3-State	3.3 MHz	+5	24
μPD8255	Peripheral Interface	8-bit	NMOS	3-State	–	+5	40
μPD8255A-5	Peripheral Interface	8-bit	NMOS	3-State	–	+5	40
μPD8257	Programmable DMA Controller	8-bit	NMOS	3-State	3 MHz	+5	40
μPD8257-5	Programmable DMA Controller	8-bit	NMOS	3-State	3 MHz	+5	40
μPD8259	Programmable Interrupt Controller	8-bit	NMOS	3-State	–	+5	28
μPD8259-5	Programmable Interrupt Controller	8-bit	NMOS	3-State	–	+5	28
μPD8279-5	Programmable Keyboard/ Display Interface	8-bit	NMOS	3-State	–	+5	40
μPB8282/ 8283	8-Bit Latches		Bipolar	3-State	5 MHz	+5	20
μPB8284	Clock Driver		Bipolar	3-State	5 MHz	+5	18
μPB8286/ 8287	8-Bit Bus Transceivers		Bipolar	3-State	5 MHz	+5	20
μPB8288	Bus Controller		Bipolar	3-State	5 MHz	+5	20
μPD8355	2048 x 8 ROM with I/O Ports	8-bit	NMOS	3-State	–	+5	40
μPD8755A	2048 x 8 EPROM with I/O Ports	8-bit	NMOS	3-State	–	+5	40

NEC Microcomputers, Inc.

MICROCOMPUTER ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
AMD	AM8080A/9080A	Microprocessor (2.0 MHz)	μPD8080AF
	AM8080A-2/9080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	AM8080A-1/9080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	AM8085A	Microprocessor (3.0 MHz)	μPD8085A
	AM8155	Programmable Peripheral Interface with 256 x 8 RAM	μPD8155
	AM8156	Programmable Peripheral Interface with 256 x 8 RAM	μPD8156
	AM8212	I/O Port (8-Bit)	μPB8212
	AM8214	Priority Interrupt Controller	μPB8214
	AM8216	Bus Driver, Inverting	μPB8216
	AM8224	Clock Generator/Driver	μPB8224
	AM8226	Bus Driver, Non-Inverting	μPB8226
	AM8228	System Controller	μPB8228
	AM8251	Programmable Communications Interface	μPD8251
	AM8255	Programmable Peripheral Interface	μPD8255
	AM8257	Programmable DMA Controller	μPD8257
	AM8355	Programmable Peripheral Interface with 2048 x 8 ROM	μPD8355
	AM8048	Single Chip Microcomputer	μPD8048
INTEL	8080A	Microprocessor (2.0 MHz)	μPD8080AF
	8080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	8080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	8021	Microcomputer with ROM	μPD8021
	8022	Microcomputer with A/D Converter	μPD8022
	8035L	Microprocessor	μPD8035L
	8039L	Microprocessor	μPD8039L
	8041A	Programmable Peripheral Controller with ROM	μPD8041A
	8048	Microcomputer with ROM	μPD8048
	8049	Microcomputer with ROM	μPD8049
	8085A	Microprocessor (3.0 MHz)	μPD8085A
	8085A-2	Microprocessor (5.0 MHz)	μPD8085A-2
	8086	Microprocessor (16-Bit)	μPD8086
	8155/8155-2	Programmable Peripheral Interface with 256 x 8 RAM	μPD8155/8155-2
	8156/8156-2	Programmable Peripheral Interface with 256 x 8 RAM	μPD8156/8156-2
	8212	I/O Port (8-Bit)	μPB8212
	8214	Priority Interrupt Controller	μPB8214
	8216	Bus Driver, Non-Inverting	μPB8216
	8224	Clock Generator/Driver	μPB8224
	8226	Bus Driver, Inverting	μPB8226
	8228	System Controller	μPB8228
	8243	I/O Expander	μPD8243
	8251	Programmable Communications Interface (Async/Sync)	μPD8251

MICROCOMPUTER ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
INTEL (CONT.)	8251A	Programmable Communications Interface (Async/Sync)	μPD8251A
	8253	Programmable Timer	μPD8253
	8253-5	Programmable Timer	μPD8253-5
	8255	Programmable Peripheral Interface	μPD8255
	8255A	Programmable Peripheral Interface	μPD8255A-5
	8255A-5	Programmable Peripheral Interface	μPD8255A-5
	8257	Programmable DMA Controller	μPD8257
	8257-5	Programmable DMA Controller	μPD8257-5
	8259	Programmable Interrupt Controller	μPD8259
	8259-5	Programmable Interrupt Controller	μPD8259-5
	8272	Double Sided/Double Density Floppy Disk Controller	μPD765
	8279-5	Programmable Keyboard/Display Interface	μPD8279-5
	8282/8283	8-Bit Latches	μPB8282/8283
	8284	Clock Driver	μPB8284
	8286/8287	8-Bit Transceivers	μPB8286/8287
	8288	Bus Controller	μPB8288
	8355	Programmable Peripheral Interface with 2048 x 8 ROM	μPD8355
	8741A	Programmable Peripheral Controller with EPROM	μPD8741A
	8748	Microcomputer with EPROM	μPD8748
	8755A	Programmable Peripheral Interface with 2K x 8 EPROM	μPD8755A
NATIONAL	INS8048	Microcomputer with ROM	μPD8048
	INS8049	Microcomputer with ROM	μPD8049
	INS8080A	Microprocessor (2.0 MHz)	μPD8080AF
	INS8080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	INS8080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	8212	I/O Port (8-Bit)	μPB8212
	8214	Priority Interrupt Controller	μPB8214
	8216	Bus Driver, Non-Inverting	μPB8216
	8224	Clock Generator/Driver	μPB8224
	8226	Bus Driver, Inverting	μPB8226
	8228	System Controller	μPB8228
	INS8251	Programmable Communications Interface	μPD8251
	INS8253	Programmable Timer	μPD8253
	INS8255	Programmable Peripheral Interface	μPD8255
	INS8257	Programmable DMA Controller	μPD8257
	INS8259	Programmable Interrupt Controller	μPD8259
T.I.	TMS8080A	Microprocessor (2.0 MHz)	μPD8080AF
	TMS8080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	TMS8080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	SN74S412	I/O Port (8-Bit)	μPB8212
	SN74LS424	Clock Generator/Driver	μPB8224
	SN74S428	System Controller	μPB8228

4-BIT SINGLE CHIP MICROCOMPUTER FAMILY

DESCRIPTION

The μCOM-4 4-bit Microcomputer Family is a broad product line of 14 individual devices designed to fulfill a wide variety of design criteria. The product line shares a compatible architecture and instruction set. The architecture includes all functional blocks necessary for a single chip controller, including an ALU, Accumulator, Byte-wide ROM, RAM, and Stack. The instruction set maximizes the efficient utilization of the fixed ROM space, and includes a variety of Single Bit Manipulation, Table Look-Up, BCD arithemetic, and Skip instructions.

The μCOM-4 Microcomputer Family includes seven different products capable of directly driving 35V Vacuum Fluorescent Displays. Four products are manufactured with a CMOS process technology. μCOM-4 Microcomputers are ideal for low-cost general purpose controller applications such as industrial controls, instruments, appliance controls, intelligent VF display drivers, and games.

The μCOM-4 Microcomputer Family can be broken down into 3 distinct groups according to their performance capabilities. These groups are distinguished by their ROM, RAM, and I/O capabilities, as follows.

μCOM-4 MICRO COMPUTER FAMILY	ROM	RAM	I/O	RELATIVE PERFORMANCE
μCOM-43	2000 x 8	96 x 4	35 ①	Highest
μCOM-44	1000 x 8	64 x 4	35	Medium
μCOM-45	1000 x 8 ②	32 x 4	21	Lowest

Notes: ① The μPD557L has 21 I/O lines.

② The μPD550 and μPD550L have 640 x 8 ROMs.

FEATURES

- Choice of ROM size: 2000 x 8, 1000 x 8, or 640 x 8
- Choice of RAM size: 96 x 4, 64 x 4, or 32 x 4
  - Six 4-Bit Working Registers Available
  - One 4-Bit Flag Register Available
- Powerful Instruction Set
  - Choice of 80 or 58 Instructions
  - Table Look-Up Capability with CZP and JPA Instructions
  - Single Bit Manipulation of RAM or I/O Ports
  - BCD Arithmetic Capability
- Choice of 3-Level, 2-Level, or 1-Level Subroutine Stack
- Extensive I/O Capability
  - Choice of 35 or 21 I/O Lines

	35 Lines	21 Lines
– 4-Bit Input Ports	2	1
– 4-Bit I/O Ports	2	2
– 4-Bit Output Ports	4	2
– 3-Bit Output Ports	1	–
– 1-Bit Output Port	–	1

- Programmable 6-Bit Timer Available
- Choice of Hardware or Testable Interrupt
- Built-In Clock Signal Generation Circuitry
- Built-In Reset Circuitry
- Single Power Supply
- Low Power Consumption
- PMOS or CMOS Technologies
- Choice of 42-pin DIP, 28-pin DIP, or 52-pin Flat Plastic Package

Internal Registers

The ALU, the Accumulator, and the Carry Flag together comprise the central portion of the μCOM-4 Microcomputer Family architecture. The ALU performs the arithmetic and logical operations and checks for various results. The Accumulator stores the results generated by the ALU and acts as the major interface point between the RAM, the I/O ports, and the Data Pointer registers. The Carry F/F can be addressed directly, and can also be set during an addition. The μCOM-43 Microcomputers also have a Carry Save F/F for storage the value of the Carry F/F.

Data Pointer Registers

The DP_H register and 4-bit DP_L register reside outside the RAM. They function as the Data Pointer, addressing the rows and columns of the RAM, respectively. They are individually accessible and the L register can be automatically incremented or decremented.

RAM

All μCOM-4 microcomputers have a static RAM organized into a multiple-row by 16-column configuration, as follows:

MICROCOMPUTER	RAM	ORGANIZATION	DP_H	DP_L
μCOM-43	96 x 4	6 rows x 16 columns	3	4
μCOM-44	64 x 4	4 rows x 16 columns	2	4
μCOM-45	32 x 4	2 rows x 16 columns	1	4

The μCOM-43 Microcomputers also have a 4-bit Flag register and six 4-bit working registers resident in the last row of the RAM. The extended μCOM-43 instruction set provides 10 additional instructions with which you can access or manipulate these seven registers.

ROM

The ROM is the mask-programmable portion of the μCOM-4 Microcomputer which stores the application program. It is organized as follows:

MICROCOMPUTER	ROM	ORGANIZATION	
		FIELDS	PAGES
μCOM-43	2000 x 8	8	8
μCOM-44	1000 x 8	8	8
μCOM-45	1000 x 8	8	8

Note that the μPD550 and μPD550L of the μCOM-45 Microcomputer Family have a 640 x 8 ROM.

FUNCTIONAL DESCRIPTION (CONT.)

Program Counter and Stack Register

The Program Counter is an 11-bit register in the μCOM-43 microcomputers, or a 10-bit register in μCOM-44 and μCOM-45 microcomputers, which contains the address of a particular instruction being executed. It is incremented during normal operation, but can be modified by various JUMP and CALL instructions. The Stack Register is a LIFO push-down stack register used to save the value of the Program Counter when a subroutine is called. It is organized as follows:

MICROCOMPUTER	STACK ORGANIZATION	ALLOWABLE SUBROUTINE CALLS
μCOM-43	3 words x 11 bits	3 Levels
μCOM-44	1 word x 10 bits	1 Level
μCOM-45	1 word x 10 bits	1 Level

Note that the CMOS μPD651 microcomputers of the μCOM-44 Microcomputer Family have a 2-level Stack Register.

Interrupts

All μCOM-4 microcomputers are equipped with a software-testable interrupt which skips an instruction if the Interrupt F/F has been set. The TIT instruction resets the Interrupt F/F.

In addition, the μCOM-43 microcomputers have a hardware interrupt, which causes an automatic stack level shift and subroutine call when an interrupt occurs.

Interval Timer

The μCOM-43 microcomputers are equipped with a programmable 6-bit interval timer which consists of a 6-bit polynomial counter and a 6-bit binary down counter. The STM instruction sets the initial value of the binary down counter and starts the timing. The polynomial counter decrements the binary down counter when 63 instruction cycles have been completed. When the binary down counter reaches zero, the timer F/F is set. The TTM instruction tests the timer F/F, and skips the next instruction if it is set.

Clock and Reset Circuitry

The Clock Circuitry for any μCOM-4 microcomputer can be implemented by connecting either an Intermediate Frequency Transformer (IFT) and a capacitor; or a Ceramic Resonator and two capacitors, to the CL_0 and CL_1 Inputs. The Power-On-Reset Circuitry for any μCOM-4 microcomputer can be implemented by connecting a Resistor, a Capacitor, and a Diode to the RESET input.

FUNCTIONAL DESCRIPTION (CONT.)

I/O Capability

The μCOM-4 microcomputer family has either 35 or 21 I/O lines, depending upon the individual part, for communication with and control of external circuitry. They are organized as follows:

Port A	PA_{0-3}	4-Bit Input
Port B	PB_{0-3}	4-Bit Input
Port C	PC_{0-3}	4-Bit Input/Output (VF Drive Possible)
Port D	PD_{0-3}	4-Bit Input/Output (VF Drive Possible)
Port E	PE_{0-3}	4-Bit Output (VF Drive Possible)
Port F	PF_{0-3}	4-Bit Output (VF Drive Possible)
Port G	PG_{0-3}	4-Bit Output (VF Drive Possible)
Port H	PH_{0-3}	4-Bit Output (VF Drive Possible)
Port I	PI_{0-2}	3-Bit Output (VF Drive Possible)

Development Tools

The NEC Microcomputers' NDS Development System is available for developing software service code, editing, and assembling source code into object code. In addition, the ASM-43 Cross Assembler is available for systems which support the ISIS-II (TM Intel Corp.) Operating System. The CASM-43 Cross Assembler is available for systems which support the CP/M (® Digital Research Corp.) Operating System.

The EVAKIT-43P Evaluation Board is available for production device emulation and prototype system debugging. The SE-43P Emulation Board is available for demonstrating the final system design. The μPD556B ROM-less Evaluation Chip is available for small pilot production.

INSTRUCTION SET SYMBOL DEFINITIONS

The following abbreviations are used in the description of the μCOM-4 instruction set:

SYMBOL	EXPLANATION AND USE
ACC	Accumulator
ACC_n	Bit "n" of Accumulator
address	Immediate address
C	Carry F/F
C'	Carry Save F/F
data	Immediate data
D_n	Bit "n" of immediate data or immediate address
DP	Data Pointer
DP_H	Upper Bits of Data Pointer
DP_L	Lower 4 Bits of Data Pointer
FLAG	FLAG Register
INTE F/F	Interrupt Enable F/F
INT F/F	Interrupt F/F
P( )	Parallel Input/Output Port addressed by the value within the brackets
P_n	Bit "n" of Program Counter
PA	Input Port A
PC	Input/Output Port C
PD	Input/Output Port D
PE	Output Port E
R	R Register
S	S Register
SKIP	Number of Bytes in next instruction when skip condition occurs
STACK	Stack Register
TC	6-Bit Binary Down Timer Counter
TIMER F/F	Timer F/F
W	W Register
X	X Register
Y	Y Register
Z	Z Register
( )	The contents of RAM addressed by the value within the brackets
[ ]	The contents of ROM addressed by the value within the brackets
←	Load, Store, or Transfer
↔	Exchange
–	Complement
∀	LOGICAL EXCLUSIVE OR

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								BYTES	CYCLES	SKIP CONDITION
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
LOAD													
LI data	$A_{CC} \leftarrow D_{3-0}$	Load A_{CC} with 4 bits of immediate data; execute succeeding LI instructions as NOP instructions	1	0	0	1	D_3	D_2	D_1	D_0	1	1	String
L	$A_{CC} \leftarrow (DP)$	Load A_{CC} with the RAM contents addressed by DP	0	0	1	1	1	0	0	0	1	1	
LM data	$A_{CC} \leftarrow (DP)$ $DP_H \leftarrow DP_H \forall D_{1-0}$	Load A_{CC} with the RAM contents addressed by DP; Perform a LOGICAL EXCLUSIVE-OR Between DP_H and 2 bits of Immediate Data; Store the result in DP_H	0	0	1	1	1	0	D_1	D_0	1	1	
LDI data	$DP \leftarrow D_{6-0}$	Load DP with 7 bits of immediate data	0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	2	2	
LDZ data	$DP_H \leftarrow 0$ $DP_L \leftarrow D_{3-0}$	Load DP_H with 0; Load DP_L with 4 bits of immediate data	1	0	0	0	D_3	D_2	D_1	D_0	1	1	
STORE													
S	$(DP) \leftarrow A_{CC}$	Store A_{CC} into the RAM location addressed by DP	0	0	0	0	0	0	1	0	1	1	
TRANSFER													
TAL	$DP_L \leftarrow A_{CC}$	Transfer A_{CC} to DP_L	0	0	0	0	0	1	1	1	1	1	
TLA	$A_{CC} \leftarrow DP_L$	Transfer DP_L to A_{CC}	0	0	0	1	0	0	1	0	1	1	
EXCHANGE													
X	$A_{CC} \leftrightarrow (DP)$	Exchange A with the RAM contents addressed by DP	0	0	1	0	1	0	0	0	1	1	
XI	$A_{CC} \leftrightarrow (DP)$ $DP_L \leftarrow DP_L + 1$ Skip if $DP_L = 0H$	Exchange A_{CC} with RAM contents addressed by DP; increment DP_L; Skip if $DP_L = 0H$	0	0	1	1	1	1	0	0	1	1 + S	$DP_L = 0H$
XD	$A_{CC} \leftrightarrow (DP)$ $DP_L \leftarrow DP_L - 1$ Skip if $DP_L = FH$	Exchange A_{CC} with the RAM contents addressed by DP; decrement DP_L; Skip if $DP_L = FH$	0	0	1	0	1	1	0	0	1	1 + S	$DP_L = FH$
XM data	$A_{CC} \leftrightarrow (DP)$ $DP_H \leftarrow DP_H \forall D_{1-0}$	Exchange A_{CC} with the RAM contents addressed by DP; Perform a LOGICAL EXCLUSIVE-OR Between DP_H and 2 bits of immediate data; store the results in DP_H	0	0	1	0	1	0	D_1	D_0	1	1	
XMI data	$A_{CC} \leftrightarrow (DP)$ $DP_H \leftarrow DP_H \forall D_{1-0}$ $DP_L \leftarrow DP_L + 1$ Skip if $DP_L = 0H$	Exchange A_{CC} with the RAM contents addressed by DP; Perform a LOGICAL EXCLUSIVE-OR Between DP_H and 2 bits of immediate data; store the results in DP_H increment DP_L; Skip if $DP_L = 0H$	0	0	1	1	1	1	D_1	D_0	1	1 + S	$DP_L = 04$
XMD data	$A_{CC} \leftrightarrow (DP)$ $DP_H \leftarrow DP_H \forall D_{1-0}$ $DP_L \leftarrow DP_L - 1$ Skip if $DP_L = FH$	Exchange A_{CC} with the RAM contents addressed by DP; Perform a LOGICAL EXCLUSIVE-OR Between DP_H and 2 bits of immediate data; store the results in DP_H decrement DP_L; Skip if $DP_L = FH$	0	0	1	0	1	1	D_1	D_0	1	1 + S	$DP_L = FH$
ARITHMETIC													
AD	$A_{CC} \leftarrow A_{CC} + (DP)$ Skip if overflow	Add the RAM contents addressed by DP to A_{CC}; skip if overflow is generated	0	0	0	0	1	0	0	0	1	1 + S	Overflow
ADC	$A_{CC} \leftarrow A_{CC} + (DP) + C$ if overflow occurs, $C \leftarrow 1$	Add the RAM contents addressed by DP, and the Carry F/F to A_{CC}; if overflow occurs, set carry F/F	0	0	0	1	1	0	0	1	1	1	
ADS	$A_{CC} \leftarrow A_{CC} + (DP) + C$ if overflow occurs, $C \leftarrow 1$ and skip	Add the RAM contents addressed by DP and the carry F/F to A_{CC}; if overflow occurs, set Carry F/F and skip	0	0	0	0	1	0	0	1	1	1 + S	Overflow
DAA	$A_{CC} \leftarrow A_{CC} + 6$	Add 6 to A_{CC} to Adjust Decimal for BCD Addition	0	0	0	0	0	1	1	0	1	1	
DAS	$A_{CC} \leftarrow A_{CC} + 10$	Add 10 to A_{CC} to Adjust Decimal for BCD Subtraction	0	0	0	0	1	0	1	0	1	1	

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
LOGICAL													
EXL	$A_{CC} \leftarrow A_{CC} \forall (DP)$	Perform a LOGICAL EXCLUSIVE-OR between the RAM contents addressed by DP and A_{CC}; store the result in A_{CC}	0	0	0	1	1	0	0	0	1	1	
ACCUMULATOR													
CLA	$A_{CC} \leftarrow 0$	Clear A_{CC} to zero	1	0	0	1	0	0	0	0	1	1	
CMA	$A_{CC} \leftarrow \overline{A_{CC}}$	Complement A_{CC}	0	0	0	1	0	0	0	0	1	1	
CIA	$A_{CC} \leftarrow \overline{A_{CC}} + 1$	Complement A; Increment A	0	0	0	1	0	0	0	1	1	1	
CARRY FLAG													
CLC	$C \leftarrow 0$	Reset Carry F/F to zero	0	0	0	0	1	0	1	1	1	1	
STC	$C \leftarrow 1$	Set Carry F/F to one	0	0	0	1	1	0	1	1	1	1	
TC	Skip if C = 1	Skip if Carry F/F is true	0	0	0	0	0	1	0	0	1	1 + S	C = 1
INCREMENT AND DECREMENT													
INC	$A_{CC} \leftarrow A_{CC} + 1$ Skip if overflow	Increment A; Skip if overflow is generated	0	0	0	0	1	1	0	1	1	1 + S	Overflow
DEC	$A_{CC} \leftarrow A_{CC} - 1$ Skip if underflow	Decrement A; Skip if underflow occurs	0	0	0	0	1	1	1	1	1	1 + S	Underflow
IND	$DP_L \leftarrow DP_L + 1$ Skip if DP_L = 0H	Increment DP_L; Skip if DP_L = 0H	0	0	1	1	0	0	1	1	1	1 + S	DP_L = 0H
DED	$DP_L \leftarrow DP_L - 1$ Skip if DP_L = FH	Decrement DP_L; Skip if DP_L = FH	0	0	0	1	0	0	1	1	1	1 + S	DP_L = FH
BIT MANIPULATION													
RMB data	$(DP)_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1-D_0) of RAM at the location addressed by DP to zero	0	1	1	0	1	0	D_1	D_0	1	1	
SMB data	$(DP)_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of RAM at the location addressed by DP to one	0	1	1	1	1	0	D_1	D_0	1	1	
REB data	$PE_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1D_0) of output Port E to zero	0	1	1	0	0	1	D_1	D_0	1	2	
SEB data	$PE_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of output Port E to one	0	1	1	1	0	1	D_1	D_0	1	2	
RPB data	$P(DP_L)_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1D_0) of the output port addressed by DP_L to zero	0	1	1	0	0	0	D_1	D_0	1	1	
SPB data	$P(DP_L)_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of the output port addressed by DP_L	0	1	1	1	0	0	D_1	D_0	1	1	
JUMP, CALL AND RETURN													
JMP address	$P_{10\text{-}0} \leftarrow D_{10\text{-}0}$	Jump to the address specified by 11 bits of immediate data	1 D_7	0 D_6	1 D_5	0 D_4	0 D_3	D_{10} D_2	D_9 D_1	D_8 D_0	2	2	
JCP address	$P_{5\text{-}0} \leftarrow D_{5\text{-}0}$	Jump to the address within the current ROM page specified by 6 bits of immediate data	1	1	D_5	D_4	D_3	D_2	D_1	D_0	1	1	
JPA	$P_{5\text{-}2} \leftarrow A_{CC}$ $P_{1\text{-}0} \leftarrow 00$	Jump to the address within the current ROM page modified by A_{CC}	0	1	0	0	0	0	0	1	1	2	
CAL address	Stack $\leftarrow$ P + 2 $P_{10\text{-}0} \leftarrow D_{10\text{-}0}$	Store a return address (P + 2) in the stack; call the subroutine program at the location specified by 11 bits of immediate data	1 D_7	0 D_6	1 D_5	0 D_4	1 D_3	D_{10} D_2	D_9 D_1	D_8 D_0	2	2	
CZP address	Stack $\leftarrow$ P + 1 $P_{10\text{-}6} \leftarrow 00000$ $P_{5\text{-}2} \leftarrow D_{3\text{-}0}$ $P_{1\text{-}0} \leftarrow 00$	Store a return address (P + 1) in the stack; call the subroutine program at one of sixteen locations in Page 0 of Field 0, specified by 4 bits of immediate data	1	0	1	1	D_3	D_2	D_1	D_0	1	1	
RT	P $\leftarrow$ Stack	Return from Subroutine	0	1	0	0	1	0	0	0	1	2	
RTS	P $\leftarrow$ Stack Skip unconditionally	Return from Subroutine; skip unconditionally	0	1	0	0	1	0	0	1	1	1 + S	Unconditional

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INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
SKIP													
CI data	Skip if $A_{CC} = D_{3-0}$	Skip if A_{CC} equals 4 bits of immediate data	0 1	0 1	0 0	1 0	0 D_3	1 D_2	1 D_1	1 D_0	2	2 + S	$A_{CC} = D_{3-0}$
CM	Skip if $A_{CC} = (DP)$	Skip if A_{CC} equals the RAM contents addressed by DP	0	0	0	0	1	1	0	0	1	1 + S	$A_{CC} = (DP)$
CMB data	Skip if $A_{CC_{bit}} = (DP)_{bit}$	Skip if the single bit (denoted by D_1D_0) of A_{CC}, is equal to the single bit (also denoted by D_1D_0) of RAM addressed by DP	0	0	1	1	0	1	D_1	D_0	1	1 + S	$A_{CC_{bit}} = (DP)_{bit}$
TAB data	Skip if $A_{CC_{bit}} = 1$	Skip if the single bit (denoted by D_1D_0) of A_{CC} is true	0	0	1	0	0	1	D_1	D_0	1	1 + S	$A_{CC_{bit}} = 1$
CLI data	Skip if $DP_L = D_{3-0}$	Skip if DP_L equals 4 bits of immediate data	0 1	0 1	0 1	1 0	0 D_3	1 D_2	1 D_1	0 D_0	2	2 + S	$DP_L = D_{3-0}$
TMB data	Skip if $(DP)_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of the RAM location addressed by DP is true	0	1	0	1	1	0	D_1	D_0	1	1 + S	$(DP)_{bit} = 1$
TPA data	Skip if $PA_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of Port A is true	0	1	0	1	0	1	D_1	D_0	1	1 + S	$PA_{bit} = 1$
TPB data	Skip if $P(DP_L)_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of the input Port addressed by DP_L is true	0	1	0	1	0	0	D_1	D_0	1	1 + S	$P(DP_L)_{bit} = 1$
INTERRUPT													
TIT	Skip if INT F/F = 1	Skip if Interrupt F/F is true; Reset Interrupt F/F	0	0	0	0	0	0	1	1	1	1 + S	INT F/F = 1
PARALLEL I/O													
IA	$A_{CC} \leftarrow PA$	Input Port A to A_{CC}	0	1	0	0	0	0	0	0	1	1	
IP	$A_{CC} \leftarrow P(DP_L)$	Input the Port addressed by DP_L to A_{CC}	0	0	1	1	0	0	1	0	1	1	
OE	$PE \leftarrow A_{CC}$	Output A_{CC} to Port E	0	1	0	0	0	1	0	0	1	1	
OP	$P(DP_L) \leftarrow A_{CC}$	Output A_{CC} to the port addressed by DP_L	0	0	0	0	1	1	1	0	1	1	
OCD	$PD_{3-0} \leftarrow D_{7-4}$ $PC_{3-0} \leftarrow D_{3-0}$	Output 8 bits of immediate data to Ports C and D	0 D_7	0 D_6	0 D_5	1 D_4	1 D_3	1 D_2	1 D_1	0 D_0	2	2	
CPU CONTROL													
NOP		Perform no operation; consume one machine cycle	0	0	0	0	0	0	0	0	1	1	

INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								BYTES	CYCLES	SKIP CONDITION
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
TRANSFER													
TAW	$W \leftarrow ACC$	Transfer ACC to W	0	1	0	0	0	0	1	1	1	2	
TAZ	$Z \leftarrow ACC$	Transfer ACC to Z	0	1	0	0	0	0	1	0	1	2	
THX	$X \leftarrow DP_H$	Transfer DP_H to X	0	1	0	0	0	1	1	1	1	2	
TLY	$Y \leftarrow DP_L$	Transfer DP_L to Y	0	1	0	0	0	1	1	0	1	2	
EXCHANGE													
XAW	$ACC \leftrightarrow W$	Exchange ACC with W	0	1	0	0	1	0	1	1	1	2	
XAZ	$ACC \leftrightarrow Z$	Exchange ACC with Z	0	1	0	0	1	0	1	0	1	2	
XHR	$DP_H \leftrightarrow R$	Exchange DP_H with R	0	1	0	0	1	1	0	1	1	2	
XHX	$DP_H \leftrightarrow X$	Exchange DP_H with X	0	1	0	0	1	1	1	1	1	2	
XLS	$DP_L \leftrightarrow$ S Register	Exchange DP_L with S Register	0	1	0	0	1	1	0	0	1	2	
XLY	$DP_L \leftrightarrow Y$	Exchange DP_L with Y	0	1	0	0	1	1	1	0	1	2	
XC	$C \leftrightarrow C'$	Exchange Carry F/F with Carry Save F/F	0	0	0	1	1	0	1	0	1	1	
FLAG													
SFB	$FLAG_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of FLAG Register to one	0	1	1	1	1	1	D_1	D_0	1	2	
RFB	$FLAG_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1D_0) of FLAG Register to zero	0	1	1	0	1	1	D_1	D_0	1	2	
FBT	Skip if $FLAG_{bit} = 1$	Skip if a single bit (denoted by D_1D_0) of the FLAG Register is true	0	1	0	1	1	1	D_1	D_0	1	2 + S	$FLAG_{bit} = 1$
FBF	Skip if $FLAG_{bit} = 0$	Skip if a single bit (denoted by D_1D_0) of the FLAG Register is false	0	0	1	0	0	0	D_1	D_0	1	2 + S	$FLAG_{bit} = 0$
ACCUMULATOR													
RAR	$ACC_{n-1} \leftarrow ACC_n$ $C \leftarrow ACC_0 (n = 1 \rightarrow 3)$ $ACC_3 \leftarrow C$	Rotate ACC right through Carry F/F	0	0	1	1	0	0	0	0	1	1	
INCREMENT AND DECREMENT													
INM	(DP) ← (DP) + 1 Skip if (DP) = 0H	Increment the RAM contents addressed by DP; Skip if the contents = 0H	0	0	0	1	1	1	0	1	1	1 + S	(DP) = 0H
DEM	(DP) ← (DP) – 1 Skip if (DP) = FH	Decrement the RAM contents addressed by DP; skip if the contents = FH	0	0	0	1	1	1	1	1	1	1 + S	(DP) = FH
TIMER													
STM	TIMER F/F ← 0 $TC \leftarrow D_{5-0}$	Reset Timer F/F to zero; Load Timer Counter with 6 bits of immediate data; Start timer	0 1	0 0	0 D_5	1 D_4	0 D_3	1 D_2	0 D_1	0 D_0	2	2	
TTM	Skip if TIMER F/F = 1	Skip if Timer F/F is true	0	0	0	0	0	1	0	1	1	1 + S	TIMER F/F = 1
INTERRUPT													
EI	INTE F/F ← 1	Set Interrupt Enable F/F to one; Enable Interrupt	0	0	1	1	0	0	0	1	1	1	
DI	INTE F/F ← 0	Reset Interrupt Enable F/F to zero; Disabie Interrupt	0	0	0	0	0	0	0	1	1	1	

NOTES

4-BIT SINGLE CHIP MICROCOMPUTERS

DESCRIPTION

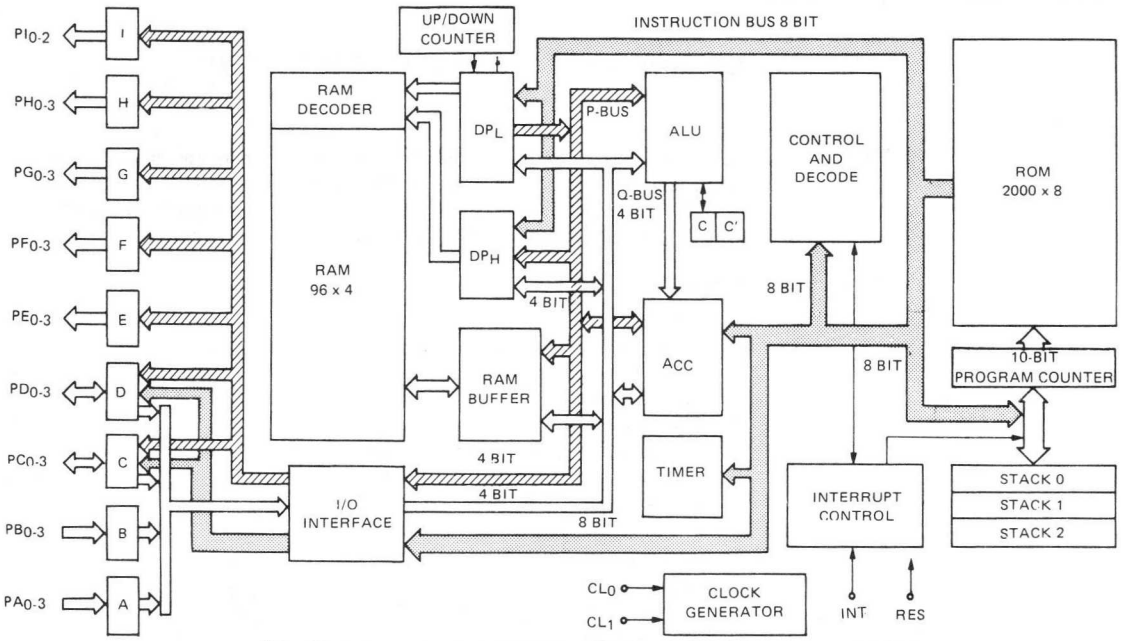
The μCOM-43 4-bit single chip microcomputers described below comprise the high-performance end of the μCOM-4 Microcomputer Family. They are distinguished from other μCOM-4 products by their larger ROM and RAM, their extensive 35 line I/O capability, and the 22 additional instructions of the Instruction Set.

FEATURES

- 2000 x 8 ROM
- 96 x 4 RAM
  - Six 4-Bit Working Registers
  - One 4-Bit Flag Register
- 10 μs Instruction Cycle Time, Typical
- 80 Powerful Instructions
  - Table Look-Up Capability with CZP and JPA Instructions
  - Single Bit Manipulation of RAM or I/O Ports
  - Ten Transfer and Exchange Instructions for Working Registers
  - Four Flag Instructions
- 3-Level Subroutine Stack
- Extensive I/O Capability
  - Two 4-Bit Input Ports (μPD557L has One)
  - Two 4-Bit I/O Ports
  - Four 4-Bit Output Ports (μPD557L has Two)
  - One 3-Bit Output Port (μPD557L has One 1-Bit Output Port Instead)
- Programmable 6-Bit Timer
- Hardware Interrupt
- Built-In Clock Signal Generation Circuitry
- Built-In RESET Circuitry
- Single Power Supply
- Low Power Consumption
- PMOS or CMOS Technologies
- 42-Pin Plastic DIP (28-Pin for μPD557L)
- Choice of 4 Different Products to Suit a Variety of Applications

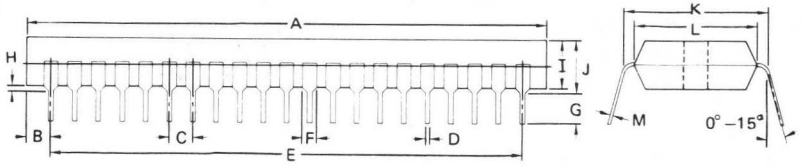
Part #	Technology	Power Supply	Package	Features
μPD546	PMOS	−10V	42-pin DIP	
μPD553	PMOS	−10V	42-pin DIP	35V Vacuum Fluorescent Display Drive
μPD557L	PMOS	−8V	28-pin DIP	
μPD650	CMOS	+5V	42-pin DIP	

μCOM-43 BLOCK DIAGRAM



Note: Block diagram above applies to μPD546, μPD553, and μPD650 4-bit microcomputers. The μPD557L block diagram is similar to the above, except that PB_{0-3}, PG_{1-3}, PH_{0-3}, and PI_{0-2} have been eliminated to accommodate the μPD557L's 28-pin package.

μCOM-43 PACKAGE OUTLINES

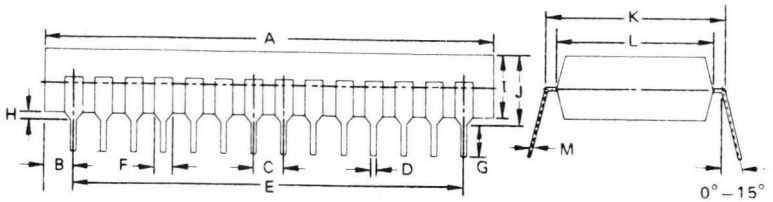


42-PIN DIP
μPD546C
μPD553C
μPD650C

Plastic

ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

28-PIN DIP
μPD557LC



Plastic

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$

6

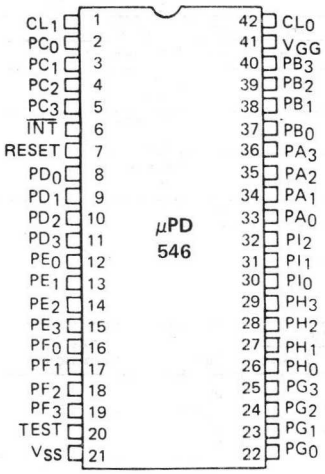
NOTES

4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD546 is the original μCOM-43 4-bit single chip microcomputer. It is manufactured with a standard PMOS process, allowing use of a single −10V power supply. The μPD546 provides all of the hardware features of the μCOM-43 family, and executes all 80 instructions of the μCOM-43 instruction set.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltages	−15 to +0.3 Volts
Output Voltages	−15 to +0.3 Volts
Output Current (Ports C through I, each bit)	−4 mA
(Total, all ports)	−25 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−2.0	V	Ports A through D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL}	−4.3		V_{GG}	V	Ports A through D, $\overline{INT}$, RESET
Clock Voltage High	$V_{\phi H}$	0		−0.8	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -1V$
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -11V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L} = -11V$
Output Voltage High	V_{OH_1}			−1.0	V	Ports C through I, $I_{OH} = -1.0$ mA
	V_{OH_2}			−2.3	V	Ports C through I, $I_{OH} = -3.3$ mA
Output Leakage Current Low	I_{LOL}			−10	μA	Ports C through I, $V_O = -11V$
Supply Current	I_{GG}		−30	−50	mA	

CAPACITANCE

$T_a = 25°C$

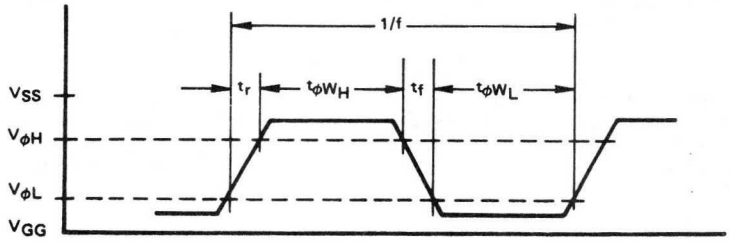
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CLOCK WAVEFORM

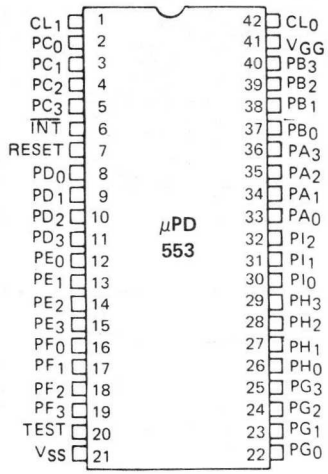


4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD553 is a μCOM-43 4-bit single chip microcomputer with high voltage outputs that can be pulled to −35V for direct interfacing to vacuum fluorescent displays. The μPD553 is manufactured with a standard PMOS process, allowing use of a single −10V power supply. The μPD553 provides all of the hardware features of the μCOM-43 family, and executes all 80 instructions of the μCOM-43 instruction set.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
CL_0-CL_1	External Clock Signals
INT	Interrupt Input
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltages (Port A, B, INT, RESET)	−15 to +0.3 Volts
(Ports C, D)	−40 to +0.3 Volts
Output Voltages	−40 to +0.3 Volts
Output Current (Ports C through I, each bit)	−12 mA
(Total, all ports)	−60 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

6

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−3.5	V	Ports A through D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−7.5		V_{GG}	V	Ports A, B, $\overline{INT}$, RESET
	V_{IL_2}	−7.5		−35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0.8	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -1V$
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -11V$
	I_{LIL_2}			−30	μA	Ports C, D, $V_I = -35V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L} = -11V$
Output Voltage High	V_{OH}			-2.0	V	Ports C through I, $I_{OH} = -8$ mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through I, $V_O = -11V$
	I_{LOL_2}			−30	μA	Ports C through I, $V_O = -35V$
Supply Current	I_{GG}		−30	−50	mA	

CAPACITANCE

$T_a = 25°C$

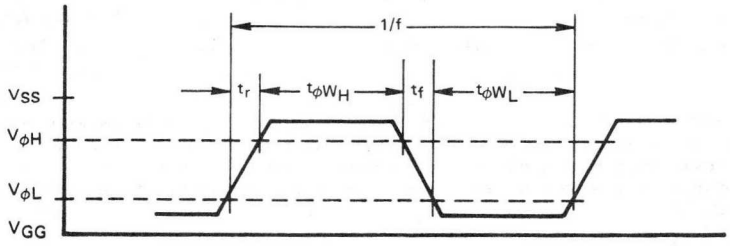
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CLOCK WAVEFORM

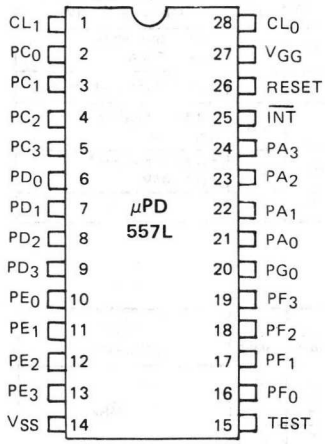


4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD557L is a μCOM-43 4-bit single chip microcomputer with high voltage outputs,and low power consumption. The outputs can be pulled to-35V for direct interfacing to vacuum fluorescent displays. The μPD557L is manufactured with a low-power-consumption PMOS process, allowing use of a -8V, low current power supply. The μPD557L provides all of the hardware features of the μCOM-43 family, except that it has 21 I/O lines in a 28-pin dual-in-line package to reduce device cost. The μPD557L executes all 80 instructions of the μCOM-43 instruction set.

PIN CONFIGURATION



PIN NAMES

PA_0–PA_3	Input Port A
PC_0–PC_3	Input/Output Port C
PD_0–PD_3	Input/Output Port D
PE_0–PE_3	Output Port E
PF_0–PF_3	Output Port F
PG_0	Output Port G
$\overline{INT}$	Interrupt Input
CL_0–CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +70°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-15 to +0.3 Volts
Input Voltages (Port A, $\overline{INT}$, RESET)	-15 to +0.3 Volts
(Ports C, D)	-40 to +0.3 Volts
Output Voltages	-40 to +0.3 Volts
Output Current (Ports C, D, each bit)	-4 mA
(Ports E, F, G, each bit)	-25 mA
(Total, all ports)	-100 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

6

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -8.0V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−2.5	V	Ports A, C, D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−6.5		V_{GG}	V	Ports A, $\overline{INT}$, RESET
	V_{IL_2}	−6.5		−35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0.6	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−5.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RESET $V_I = -1V$
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A, C, D, $\overline{INT}$, RESET $V_I = -9V$
	I_{LIL_2}			−30	μA	Ports C, D, $V_I = -35V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L} = -9V$
Output Voltage High	V_{OH_1}			−1.0	V	Ports C through G, $I_{OH} = -2$ mA
	V_{OH_2}			−4.0	V	Ports E, F, G, $I_{OH} = -20$ mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through G, $V_O = -9V$
	I_{LOL_2}			−30	μA	Ports C through G, $V_O = -35V$
Supply Current	I_{GG}		−20	−36	mA	

CAPACITANCE

$T_a = 25°C$

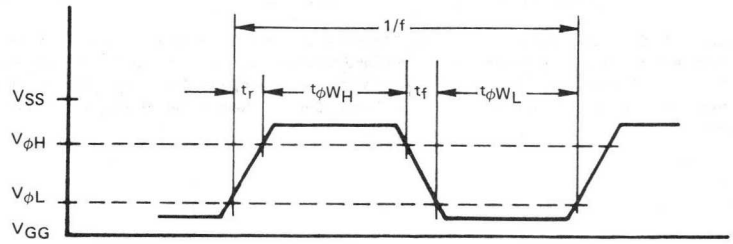
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -8.0V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	100		180	kHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	External Clock
Clock Pulse Width High	$t_{\phi W_H}$	2.0		8.0	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	2.0		8.0	μs	

CLOCK WAVEFORM

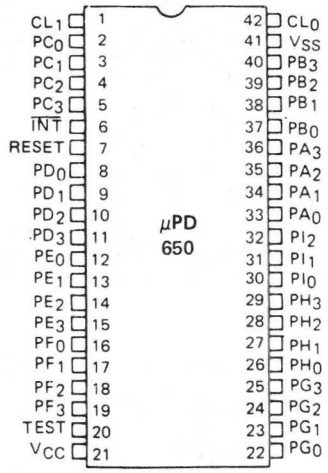


4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD650 is a μCOM-43 4-bit single chip microcomputer manufactured with a low-power-consumption CMOS process, allowing use of a single +5V power supply. The μPD650 provides all of the hardware features of the μCOM-43 family, and executes all 80 instructions of the μCOM-43 instruction set.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{CC}	Power Supply Positive
V_{SS}	Ground
TEST	Factory Test Pin (Connect to V_{CC})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-30°C to +85°C
Storage Temperature	-55°C to +125°C
Supply Voltage	-0.3 to +7.0 Volts
Input Voltages (Port A through D, $\overline{INT}$, RESET)	-0.3 to +7.3 Volts
Output Voltages	-0.3 to +7.3 Volts
Output Current (Ports C through I, each bit)	2.5 mA
(Total, all ports)	28mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = -30°C$ to $+85°C$; $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0.7 V_{CC}		V_{CC}	V	Ports A through D, $\overline{INT}$ RESET
Input Voltage Low	V_{IL}	0		0.3 V_{CC}	V	Ports A through D, $\overline{INT}$ RESET
Clock Voltage High	$V_{\phi H}$	0.7 V_{CC}		V_{CC}	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	0		0.3 V_{CC}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$ RESET, $V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = 0V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = V_{CC}$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L} = 0V$
Output Voltage High	V_{OH_1}	V_{CC} −0.5			V	Ports C through I, $I_{OH} = -1.0$ mA
	V_{OH_2}	V_{CC} −2.5			V	Ports C through I, $I_{OH} = -2.0$ mA
Output Voltage Low	V_{OL_1}			+0.6	V	Ports E through I, $I_{OL} = +2.0$ mA
	V_{OL_2}			+0.4	V	Ports E through I, $I_{OL} = +1.2$ mA
Output Leakage Current Low	I_{LOL}			−10	μA	Ports C, D, $V_O = 0V$
Supply Current	I_{CC}		+0.8	+2.0	mA	

CAPACITANCE

$T_a = 25°C$

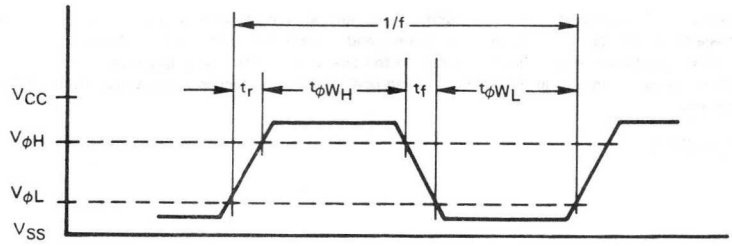
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -30°C$ to $+85°C$; $V_{CC} = +5 \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μS	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μS	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μS	

CLOCK WAVEFORM



4-BIT SINGLE CHIP MICROCOMPUTERS

DESCRIPTION

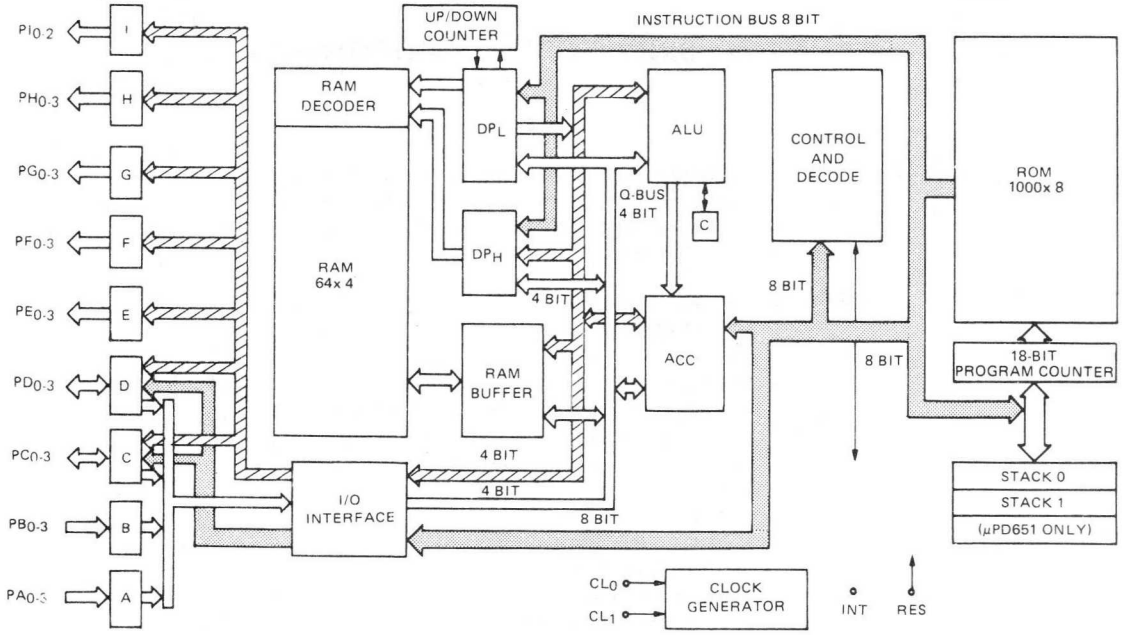
The μCOM-44 4-bit single chip microcomputers described below comprise the medium-performance portion of the μCOM-4 Microcomputer Family. They are distinguished from other μCOM-4 products by their ROM and RAM, and their extensive 35 line I/O capability.

FEATURES

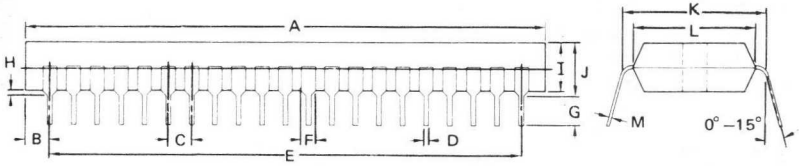
- 1000 x 8 ROM
- 64 x 4 RAM
- 10 μs Instruction Cycle Time, Typical
- 58 Powerful Instructions
  - Table Look-Up Capability with CZP and JPA Instructions
  - Single Bit Manipulation of RAM or I/O Ports
- 1-Level Subroutine Stack (μPD651 has a 2-Level Stack)
- Extensive I/O Capability
  - Two 4-Bit Input Ports
  - Two 4-Bit I/O Ports
  - Four 4-Bit Output Ports
  - One 3-Bit Output Port
- Software Testable Interrupt
- Built-In Clock Signal Generation Circuitry
- Built-In RESET Circuitry
- Single Power Supply
- Low Power Consumption
- PMOS or CMOS Technologies
- 42-Pin Plastic DIP
- Choice of 5 Different Products to Suit a Variety of Applications

Part #	Technology	Power Supply	Package	Features
μPD547	PMOS	−10V	42-pin DIP	
μPD547L	PMOS	−8V	42-pin DIP	
μPD552	PMOS	−10V	42-pin DIP	35V Vacuum Fluorescent Display Drive
μPD651C	CMOS	+5V	42-pin DIP	
μPD651G	CMOS	+5V	52-pin Flat Plastic	

μCOM-44
BLOCK DIAGRAM



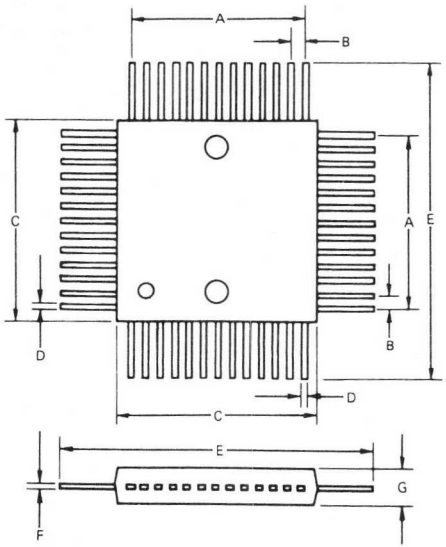
μCOM-44 PACKAGE
OUTLINES



42-PIN DIP
μPD547
μPD547L
μPD552
μPD651C

ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

52-PIN FLAT PLASTIC
PACKAGE
μPD651G



ITEM	MILLIMETERS	INCHES
A	12.0 MAX.	0.47 MAX.
B	1.0 · 0.1	0.04 · 0.004
C	14.0	0.55
D	0.4	0.016
E	21.8 · 0.4	0.86 · 0.016
F	0.15	0.006
G	2.6	0.1

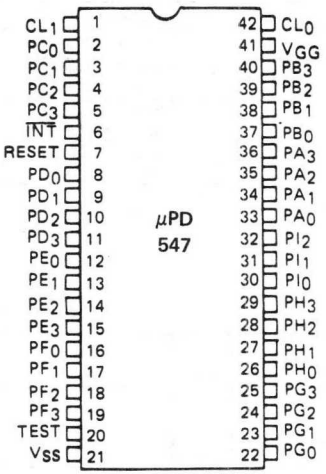
6

4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD547 is the original μCOM-44 4-bit single chip microcomputer. It is manufactured with a standard PMOS process, allowing use of a single – 10V power supply. The μPD547 provides all of the hardware features of the μCOM-44 family, and executes all 58 instructions of the μCOM-44 instruction set.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

6

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	–10°C to +70°C
Storage Temperature	–40°C to +125°C
Supply Voltage	–15 to +0.3 Volts
Input Voltages	–15 to +0.3 Volts
Output Voltages	–15 to +0.3 Volts
Output Current (Ports C through I, each bit)	–4 mA
(Total, all ports)	–25 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		-2.0	V	Ports A through D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL}	-4.3		V_{GG}	V	Ports A through D, $\overline{INT}$, RESET
Clock Voltage High	$V_{\phi H}$	0		-0.8	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	-6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -1V$
Input Leakage Current Low	I_{LIL}			-10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -11V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			-200	μA	CL_0 Input, $V_{\phi L} = -11V$
Output Voltage High	V_{OH_1}			-1.0	V	Ports C through I, $I_{OH} = -1.0$ mA
	V_{OH_2}			-2.3	V	Ports C through I, $I_{OH} = -3.3$ mA
Output Leakage Current Low	I_{LOL}			-10	μA	Ports C through I, $V_O = -11V$
Supply Current	I_{GG}		-30	-50	mA	

CAPACITANCE

$T_a = 25°C$

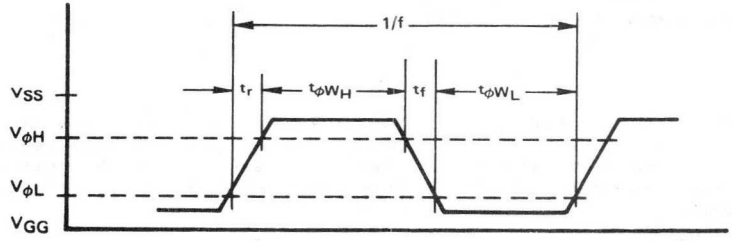
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CLOCK WAVEFORM

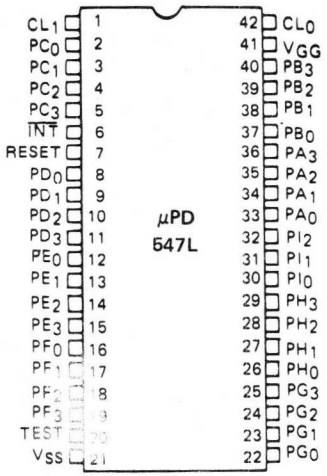


4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD547L is a μCOM-44 4-bit single chip microcomputer, manufactured with the low power consumption PMOS process, allowing use of a single −8V power supply. The μPD547L provides all of the hardware features of the μCOM-44 family, and executes all 58 instructions of the μCOM-44 instruction set.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

6

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltages	−15 to +0.3 Volts
Output Voltages	−15 to +0.3 Volts
Output Current (Ports C through I, each bit)	−4 mA
(Total, all ports)	−25 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -8V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−1.6	V	Ports A through D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL}	−3.8		V_{GG}	V	Ports A through D, $\overline{INT}$, RESET
Clock Voltage High	$V_{\phi H}$	0		−0.6	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−5.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -1V$
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -9V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L} = -9V$
Output Voltage High	V_{OH_1}			−1.0	V	Ports C through I, $I_{OH} = -1.0$ mA
	V_{OH_2}			−2.3	V	Ports C through I, $I_{OH} = -3.3$ mA
Output Leakage Current Low	I_{LOL}			−10	μA	Ports C through I, $V_O = -9V$
Supply Current	I_{GG}		−15	−25	mA	

CAPACITANCE

$T_a = 25°C$

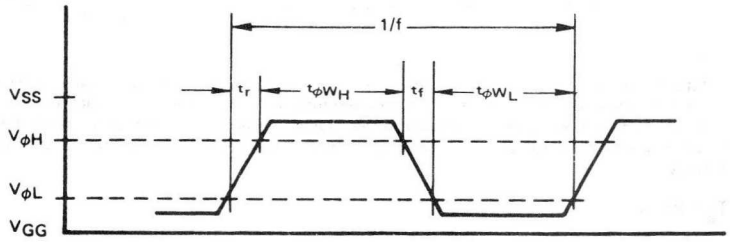
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -8V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	100		180	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	2.0		8.0	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	2.0		8.0	μs	

CLOCK WAVEFORM



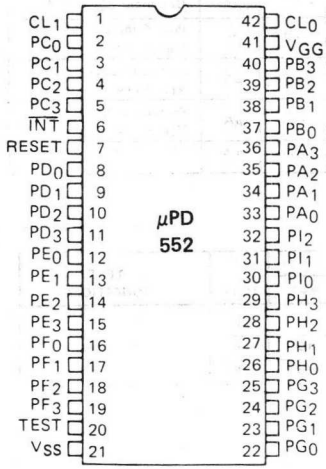
547LS-10-80-CAT

4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD552 is a μCOM-44 4-bit single chip microcomputer with high voltage outputs that can be pulled to −35V for direct interfacing to vacuum fluorescent displays. The μPD552 is manufactured with a standard PMOS process, allowing use of a single −10V power supply. The μPD552 provides all of the hardware features of the μCOM-44 family, and executes all 58 instructions of the μCOM-44 instruction set.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltages (Port A, B, $\overline{INT}$, RESET)	−15 to +0.3 Volts
(Ports C, D)	−40 to +0.3 Volts
Output Voltages	−40 to +0.3 Volts
Output Current (Ports C through I, each bit)	−12 mA
(Total, all ports)	−60 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

μPD552

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		-3.5	V	Ports A through D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	-7.5		V_{GG}	V	Ports A, B, $\overline{INT}$, RESET
	V_{IL_2}	-7.5		-35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		-0.8	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	-6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -1V$
Input Leakage Current Low	I_{LIL_1}			-10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -11V$
	I_{LIL_2}			-30	μA	Ports C, D, $V_I = -35V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			-200	μA	CL_0 Input, $V_{\phi L} = -11V$
Output Voltage High	V_{OH}			-2.0	V	Ports C through I, $I_{OH} = -8$ mA
Output Leakage Current Low	I_{LOL_1}			-10	μA	Ports C through I, $V_O = -11V$
	I_{LOL_2}			-30	μA	Ports C through I, $V_O = -35V$
Supply Current	I_{GG}		-30	-50	mA	

CAPACITANCE

$T_a = 25°C$

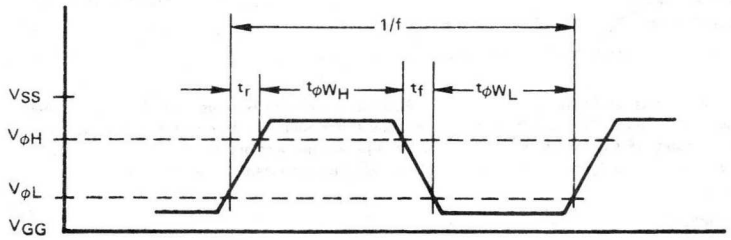
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	External Clock
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CLOCK WAVEFORM

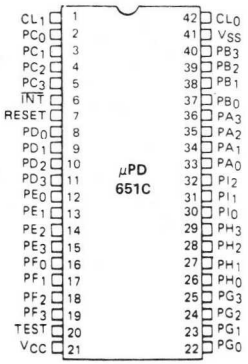


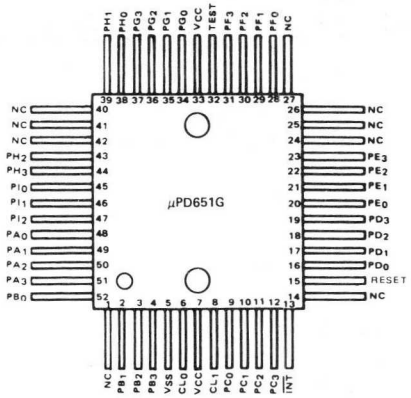
4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD651 is a μCOM-44 4-bit single chip microcomputer manufactured with a low-power-consumption CMOS process, allowing use of a single +5V power supply. The μPD651 provides all of the hardware features of the μCOM-44 family, except that it has two subroutine stack levels to enhance software development. The μPD651 executes all 58 instructions of the μCOM-44 instruction set, and it is available either in a 42-pin Dual-in-line package (μPD651C), or in a space-saving 52-pin Flat-package (μPD651G).

PIN CONFIGURATION





PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{CC}	Power Supply Positive
V_{SS}	Ground
TEST	Factory Test Pin (Connect to V_{CC})
NC	No Connection

6

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-30°C to +85°C
Storage Temperature	-55°C to +125°C
Supply Voltage	-0.3 to +7.0 Volts
Input Voltages (Port A through D, $\overline{INT}$, RESET)	-0.3 to +7.3 Volts
Output Voltages	-0.3 to +7.3 Volts
Output Current (Ports C through I, each bit)	2.5 mA
(Total, all ports)	28 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −30°C to +85°C; V_{CC} = +5V ±10%

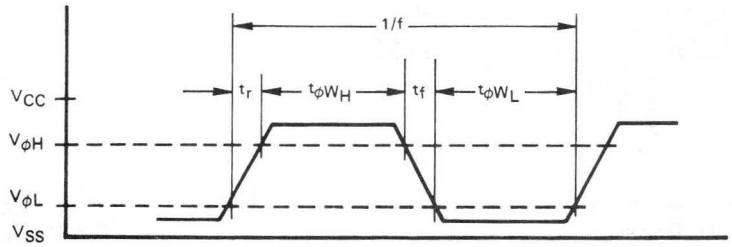
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0.7 V_{CC}		V_{CC}	V	Ports A through D, $\overline{INT}$ RESET
Input Voltage Low	V_{IL}	0		0.3 V_{CC}	V	Ports A through D, $\overline{INT}$ RESET
Clock Voltage High	$V_{\phi H}$	0.7 V_{CC}		V_{CC}	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	0		0.3 V_{CC}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$ RESET, $V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A through D, $\overline{INT}$, RESET, V_I = 0V
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = V_{CC}$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L}$ = 0V
Output Voltage High	V_{OH_1}	V_{CC} −0.5			V	Ports C through I, I_{OH} = −1.0 mA
	V_{OH_2}	V_{CC} −2.5			V	Ports C through I, I_{OH} = −2.0 mA
Output Voltage Low	V_{OL_1}			+0.6	V	Ports E through I, I_{OL} = +2.0 mA
	V_{OL_2}			+0.4	V	Ports E through I, I_{OL} = +1.2 mA
Output Leakage Current Low	I_{LOL}			−10	μA	Ports C, D, V_O = 0V
Supply Current	I_{CC}		+0.8	+2.0	mA	

AC CHARACTERISTICS

T_a = −30°C to +85°C; V_{CC} = +5 ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μS	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μS	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μS	

CLOCK WAVEFORM



CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

4-BIT SINGLE CHIP MICROCOMPUTERS

DESCRIPTION

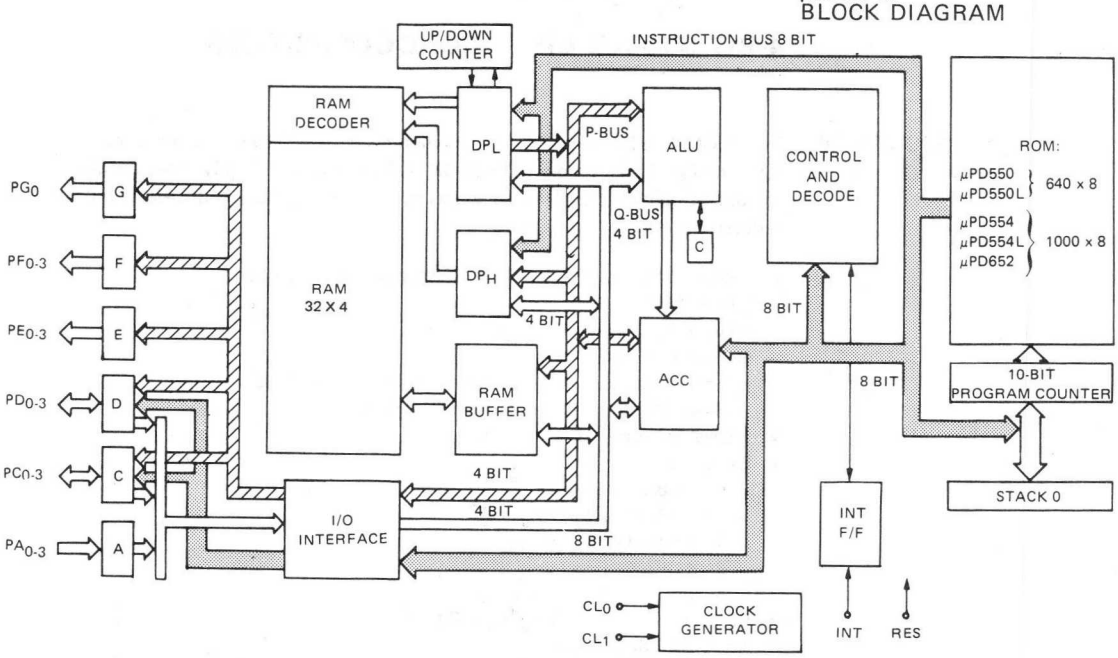
The μCOM-45 4-bit single chip microcomputers described below comprise the lower-performance portion of the μCOM-4 Microcomputer Family. They are distinguished from other μCOM-4 products by their smaller ROM and RAM, and their reduced 21 line I/O capability.

FEATURES

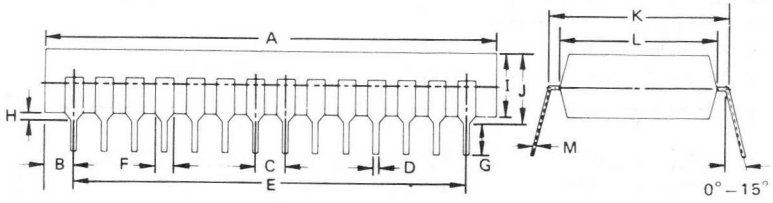
- 1000 x 8 ROM (μPD550 and μPD550L have 640 x 8 ROM)
- 32 x 4 RAM
- 10 μs Instruction Cycle Time, Typical
- 58 Powerful Instructions
  - Table Look-Up Capability with CZP and JPA Instructions
  - Single Bit Manipulation of RAM or I/O Ports
- 1-Level Subroutine Stack
- Extensive I/O Capability
  - One 4-Bit Input Ports
  - Two 4-Bit I/O Ports
  - Two 4-Bit Output Ports
  - One 1-Bit Output Port
- Software Testable Interrupt
- Built-In Clock Signal Generation Circuitry
- Built-In RESET Circuitry
- Single Power Supply
- Low Power Consumption
- PMOS or CMOS Technologies
- 28-Pin Plastic DIP
- Choice of 5 Different Products to Suit a Variety of Applications

Part #	Technology	Power Supply	Package	Features
μPD550	PMOS	−10V	28-pin DIP	
μPD550L	PMOS	−8V	28-pin DIP	
μPD554	PMOS	−10V	28-pin DIP	35V Vacuum Fluorescent Display Drive
μPD554L	PMOS	−8V	28-pin	
μPD652	CMOS	−15V	28-pin	

μCOM-45 BLOCK DIAGRAM



μCOM-45 PACKAGE OUTLINE



28-PIN DIP
μPD550C
μPD550LC
μPD554C
μPD554LC
μPD652C

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

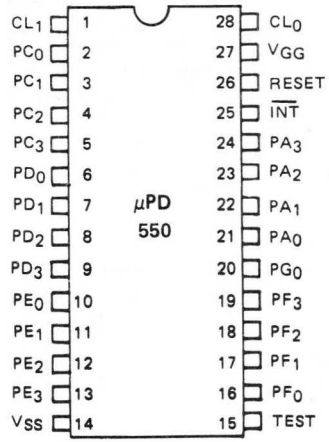
μCOM-45DS-12-80-CAT

4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD550 is a μCOM-45 4-bit single chip microcomputer with high voltage outputs that can be pulled to −35V for direct interfacing to vacuum fluorescent displays. The μPD550 is manufactured with a standard PMOS process, allowing use of a single −10V power supply. The μPD550 provides all of the hardware features of the μCOM-45 family, except that it has a 640 x 8 bit ROM to reduce device cost. The μPD550 executes all 58 instructions of the μCOM-45 instruction set.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0	Output Port G
CL_0-CL_1	External Clock Signals
$\overline{INT}$	Interrupt Input
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

6

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −40°C to +125°C
Supply Voltage . . . . . −15 to +0.3 Volts
Input Voltages (Port A, $\overline{INT}$, RESET) . . . . . −15 to +0.3 Volts
(Ports C, D) . . . . . −40 to +0.3 Volts
Output Voltages . . . . . −40 to +0.3 Volts
Output Current (Ports C, D, each bit) . . . . . −4 mA
(Ports E, F, G, each bit) . . . . . −15 mA
(Total, all ports) . . . . . −60 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−2.0	V	Ports A, C, D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−4.3		V_{GG}	V	Ports A, $\overline{INT}$, RESET
	V_{IL_2}	−4.3		−35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0.6	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RESET $V_I = -1V$
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A, C, D, $\overline{INT}$, RESET $V_I = -11V$
	I_{LIL_2}			−30	μA	Ports C, D, $V_I = -35V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L} = -11V$
Output Voltage High	V_{OH_1}			−1.0	V	Ports C, D, $I_{OH} = -2$ mA
	V_{OH_2}			−2.5	V	Ports E, F, G, $I_{OH} = -10$ mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through G, $V_O = -11V$
	I_{LOL_2}			−30	μA	Ports C through G, $V_O = -35V$
Supply Current	I_{GG}		−20	−40	mA	

CAPACITANCE

$T_a = 25°C$

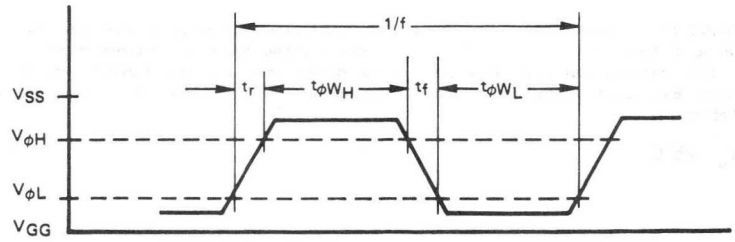
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	External Clock
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CLOCK WAVEFORM

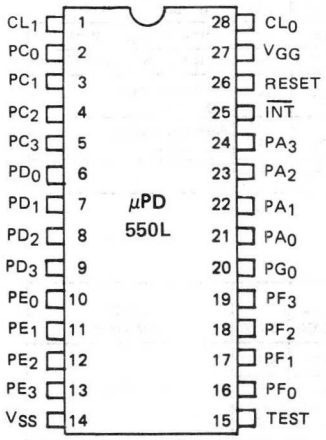


4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD550L is a μCOM-45 4-bit single chip microcomputer with high voltage outputs, and low power consumption. The outputs can be pulled to −35V for direct interfacing to vacuum fluorescent displays. The μPD550L is manufactured with a low-power-consumption PMOS process, allowing use of a −8V, low current power supply. The μPD550L provides all of the hardware features of the μCOM-45 family, except that it has a 640 x 8 bit ROM to reduce device cost. The μPD550L executes all 58 instructions of the μCOM-45 instruction set.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0	Output Port G
CL_0-CL_1	External Clock Signals
$\overline{INT}$	Interrupt Input
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

6

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltages (Port A, $\overline{INT}$, RESET)	−15 to +0.3 Volts
(Ports C, D)	−40 to +0.3 Volts
Output Voltages	−40 to +0.3 Volts
Output Current (Ports C, D, each bit)	−4 mA
(Ports E, F, G, each bit)	−15 mA
(Total, all ports)	−60 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −8.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−1.6	V	Ports A, C, D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−4.5		V_{GG}	V	Ports A, $\overline{INT}$, RESET
	V_{IL_2}	−4.5		−35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0.6	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−5.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RESET V_I = −1V
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A, C, D, $\overline{INT}$, RESET V_I = −9V
	I_{LIL_2}			−30	μA	Ports C, D, V_I = −35V
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H}$ = 0V
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L}$ = −9V
Output Voltage High	V_{OH_1}			−1.0	V	Ports C, D, I_{OH} = −2 mA
	V_{OH_2}			−2.5	V	Ports E, F, G, I_{OH} = −10 mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through G, V_O = −9V
	I_{LOL_2}			−30	μA	Ports C through G, V_O = −35V
Supply Current	I_{GG}		−12	−24	mA	

CAPACITANCE

T_a = 25°C

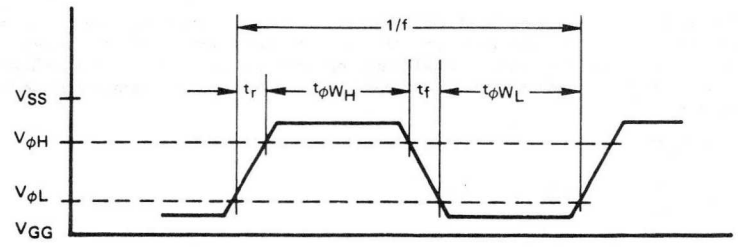
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −8.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	100		180	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	External Clock
Clock Pulse Width High	$t_{\phi W_H}$	2.0		8.0	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	2.0		8.0	μs	

CLOCK WAVEFORM

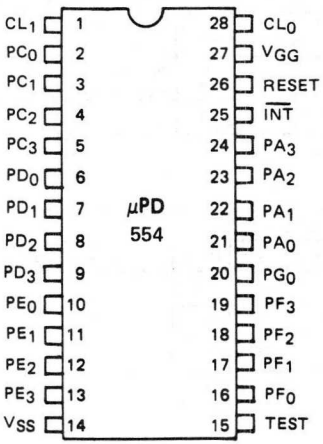


4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD554 is the standard μCOM-45 4-bit single chip microcomputer, with high voltage outputs that can be pulled to −35V for direct interfacing to vacuum fluorescent displays. The μPD554 is manufactured with a standard PMOS process, allowing use of a single −10V power supply. The μPD554 provides all of the hardware features of the μCOM-45 family, and executes all 58 instructions of the μCOM-45 instruction set.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0	Output Port G
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
$\overline{TEST}$	Factory Test Pin (Connect to V_{SS})

6

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltages (Port A, $\overline{INT}$, RESET)	−15 to +0.3 Volts
(Ports C, D)	−40 to +0.3 Volts
Output Voltages	−40 to +0.3 Volts
Output Current (Ports C, D, each bit)	−4 mA
(Ports E, F, G, each bit)	−15 mA
(Total, all ports)	−60 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −10V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−2.0	V	Ports A, C, D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−4.3		V_{GG}	V	Ports A, $\overline{INT}$, RESET
	V_{IL_2}	−4.3		−35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0.6	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RESET V_I = −1V
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A, C, D, $\overline{INT}$, RESET V_I = −11V
	I_{LIL_2}			−30	μA	Ports C, D, V_I = −35V
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H}$ = 0V
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L}$ = −11V
Output Voltage High	V_{OH_1}			−1.0	V	Ports C, D, I_{OH} = −2 mA
	V_{OH_2}			−2.5	V	Ports E, F, G, I_{OH} = −10 mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through G, V_O = −11V
	I_{LOL_2}			−30	μA	Ports C through G, V_O = −35V
Supply Current	I_{GG}		−20	−40	mA	

CAPACITANCE

T_a = 25°C

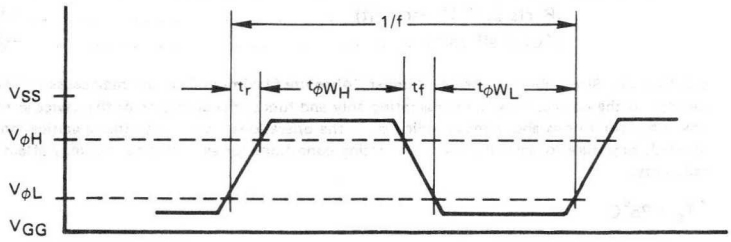
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_I			15	pF	

AC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −10V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	External Clock
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CLOCK WAVEFORM

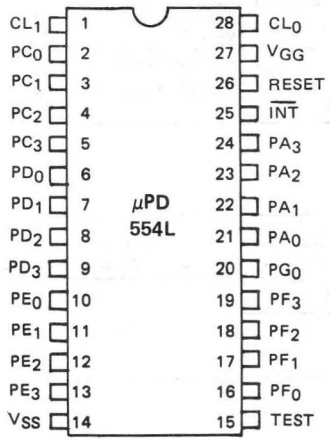


4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD554L is a μCOM-45 4-bit single chip microcomputer with high voltage outputs and low power consumption. The outputs can be pulled to −35V for direct interfacing to vacuum fluorescent displays. The μPD554L is manufactured with a low-power-consumption PMOS process, allowing use of a −8V, low current power supply. The μPD554L provides all of the hardware features of the μCOM-45 family, and executes all 58 instructions of the μCOM-45 instruction set.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0	Output Port G
CL_0-CL_1	External Clock Signals
$\overline{INT}$	Interrupt Input
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltages (Port A, $\overline{INT}$, RESET)	−15 to +0.3 Volts
(Ports C, D)	−40 to +0.3 Volts
Output Voltages	−40 to +0.3 Volts
Output Current (Ports C, D, each bit)	−4 mA
(Ports E, F, G, each bit)	−15 mA
(Total, all ports)	−60 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

μPD554L

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -8.0V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−1.6	V	Ports A, C, D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−4.5		V_{GG}	V	Ports A, $\overline{INT}$, RESET
	V_{IL_2}	−4.5		−35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0.6	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−5.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RESET $V_I = -1V$
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A, C, D, $\overline{INT}$, RESET $V_I = -9V$
	I_{LIL_2}			−30	μA	Ports C, D, $V_I = -35V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L} = -9V$
Output Voltage High	V_{OH_1}			−1.0	V	Ports C, D, $I_{OH} = -2$ mA
	V_{OH_2}			−2.5	V	Ports E, F, G, $I_{OH} = -10$ mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through G, $V_O = -9V$
	I_{LOL_2}			−30	μA	Ports C through G, $V_O = -35V$
Supply Current	I_{GG}		−12	−24	mA	

CAPACITANCE

$T_a = 25°C$

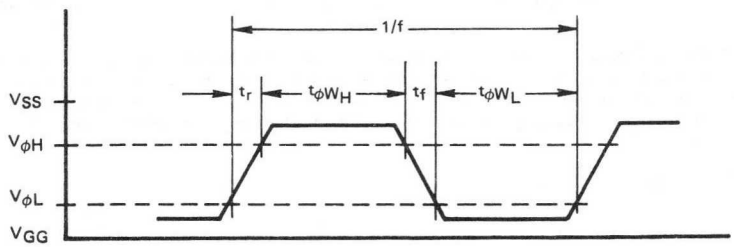
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -8.0V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	100		180	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	External Clock
Clock Pulse Width High	$t_{\phi W_H}$	2.0		8.0	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	2.0		8.0	μs	

CLOCK WAVEFORM



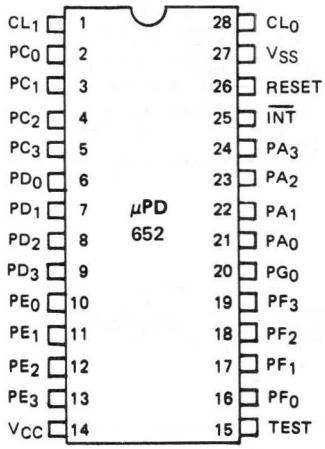
554LDS-9-80-CAT

4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD652 is a μCOM-45 4-bit single chip microcomputer manufactured with a low-power-consumption CMOS process, allowing use of a single +5V power supply. The μPD652 provides all of the hardware features of the μCOM-45 family, and executes all 58 instructions of the μCOM-45 instruction set.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0	Output Port G
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{CC}	Power Supply Positive
V_{SS}	Power Supply Negative
TEST	Factory Test Pin (Connect to V_{CC})

6

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−30°C to +85°C
Storage Temperature	−55°C to +125°C
Supply Voltage	−0.3 to 7.0V
Input Voltages (Ports A, C, D, $\overline{INT}$, RESET)	−0.3 to 7.3V
Output Voltages	−0.3 to 7.3V
Output Current (Ports C through G, each bit)	−2.5 mA
(Total, all ports)	−28.0 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTS

T_a = −30°C to +85°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0.7 V_{CC}		V_{CC}	V	Ports A, C, D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL}	0		0.3 V_{CC}	V	Ports A, C, D, $\overline{INT}$, RESET
Clock Voltage High	$V_{\phi H}$	0.7 V_{CC}		V_{CC}	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	0		0.3 V_{CC}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RESET, $V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A, C, D, $\overline{INT}$, RESET, V_I = 0V
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = V_{CC}$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L}$ = 0V
Output Voltage High	V_{OH_1}	V_{CC}−0.5			V	Ports C through G, I_{OH} = −1.0 mA
	V_{OH_2}	V_{CC}−2.5			V	Ports C through G, I_{OH} = −2.0 mA
Output Voltage Low	V_{OL_1}			+0.6	V	Ports E, F, G, I_{OL} = +2.0 mA
	V_{OL_2}			+0.4	V	Ports E, F, G, I_{OL} = +1.2 mA
Output Leakage Current Low	I_{LOL}			−10	μA	Ports C, $\overline{D}$, V_O = 0V
Supply Current	I_{CC}		+0.8	+2.0	mA	

CAPACITANCE

T_a = 25°C

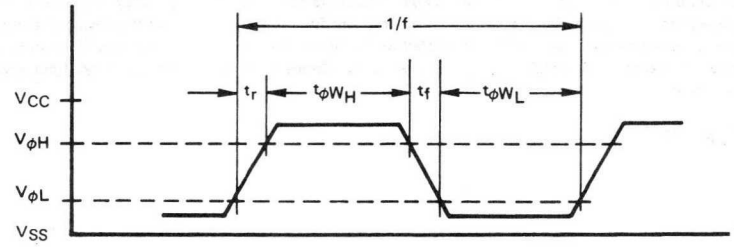
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

T_a = −30°C to +85°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	kHz	External Clock
Rise and Fall Times	t_r, t_f	0		0.3	μs	
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CLOCK WAVEFORM



EVACHIP-43

DESCRIPTION

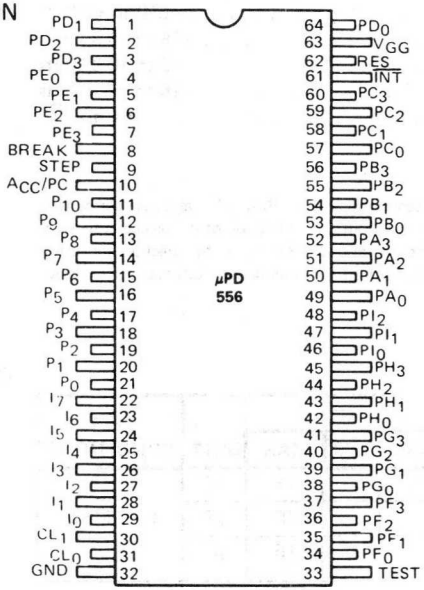
The μPD556 is an evaluation chip for the μCOM-43/44/45 single chip microcomputers. Designed to be used for both hardware and software debugging, the EVACHIP-43 is functionally equivalent to the μCOM-43, except that it does not contain on-chip ROM. Instead, it is able to address external memory. In addition, in order to facilitate debugging, the μPD556 is capable of displaying the contents of the internal accumulator and data pointer and of being single stepped.

When the μPD556 is being used to evaluate μCOM-44/45 designs, the external memory capacity should be restricted to that of the respective on-chip ROM and the instructions should be restricted to the 58 comprising the μCOM-44/45 instruction set.

FEATURES

- 4-bit Parallel Processor
- Full 80 Instruction Set of μCOM-43
- 10 μs Instruction Cycle
- Capable of addressing 2K x 8-bits of external program memory
- Single step capability
- Full Functionality of μCOM-43
- Single supply: -10V PMOS Technology
- Available in a 64-pin Ceramic Quad-in-Line Package

PIN CONFIGURATION

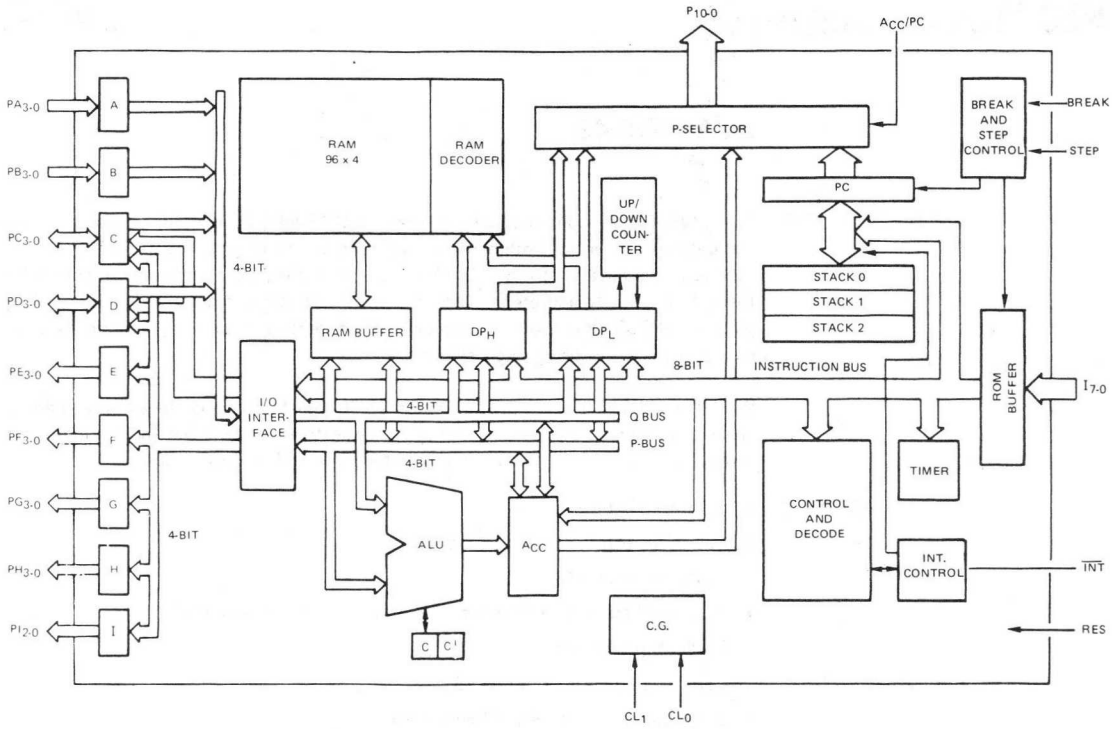


PIN NAMES

PF_0 – PF_3	Output Port F
PG_0 – PG_3	Output Port G
PH_0 – PH_3	Output Port H
PI_0 – PI_2	Output Port I
PA_0 – PA_3	Input Port A
PB_0 – PB_3	Input Port B
PC_0 – PC_3	Input/Output Port C
$\overline{INT}$	Interrupt Input
RES	Reset
PD_0 – PD_3	Input/Output Port D
PE_0 – PE_3	Output Port E
BREAK	Hold Input
STEP	Single Step Input
A_{CC}/PC	Display A_{CC}/PC Input
P_0 – P_{10}	PC Output
I_0 – I_7	Instruction Input
CL_0 – CL_1	External Clock Source
TEST	Tied to V_{SS} (GND)

6

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage V_{GG}	−15 to +0.3 Volts
All Input Voltages	−15 to +0.3 Volts
All Output Voltages	−15 to +0.3 Volts
Output Current	−4 mA ①

Note: ① All output pins.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

DC CHARACTERISTICS ①

$T_a = -10$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	0		−2.0	V	Port A to D, I_7 to I_0, BREAK, STEP, $\overline{INT}$, RES, and A_{CC}/PC
Input Low Voltage	V_{IL}	−4.3		V_{GG}	V	Port A to D, I_7 to I_0, BREAK, STEP, $\overline{INT}$, RES, and A_{CC}/PC
Clock High Voltage	V_{OH}	0		−0.8	V	CL_0 Input
Clock Low Voltage	V_{OL}	−6.0		V_{GG}	V	CL_0 Input
Input Leakage Current High	I_{LIH}			+10	μA	Port A and B, I_7 to I_0 $\overline{INT}$, RES, BREAK, STEP
				+30	μA	A_{CC}/PC, $V_I = -1V$ Port C and D, $V_I = -1V$
Input Leakage Current Low	I_{LIL}			−10	μA	Port A and B, I_7 to I_0 $\overline{INT}$, RES, BREAK, STEP
				−30	μA	A_{CC}/PC, $V_I = -11V$ Port C and D, $V_I = -11V$
Clock Input Leakage High	I_{LOH}			+200	μA	CL_0 Input, $V_{OH} = 0V$
Clock Input Leakage Low	I_{LOL}			−200	μA	CL_0 Input, $V_{OL} = -11V$
Output High Voltage	V_{OH1}			−1.0	V	Port C to I, P_{10} to P_0 $I_{OH} = -1.0$ mA
	V_{OH2}			−2.3	V	Port C to I, P_{10} to P_0 $I_{OH} = -3.3$ mA
Output Leakage Current Low	I_{LOL}			−30	μA	Port C to I, P_{10} to P_0 $V_O = -11V$
Supply Current	I_{GG}		−30	−50	mA	

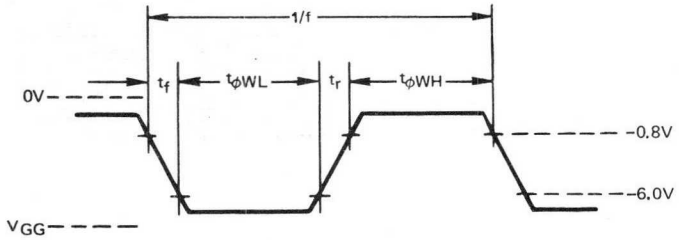
Note: ① Relative to $V_{SS} = 0V$

AC CHARACTERISTICS

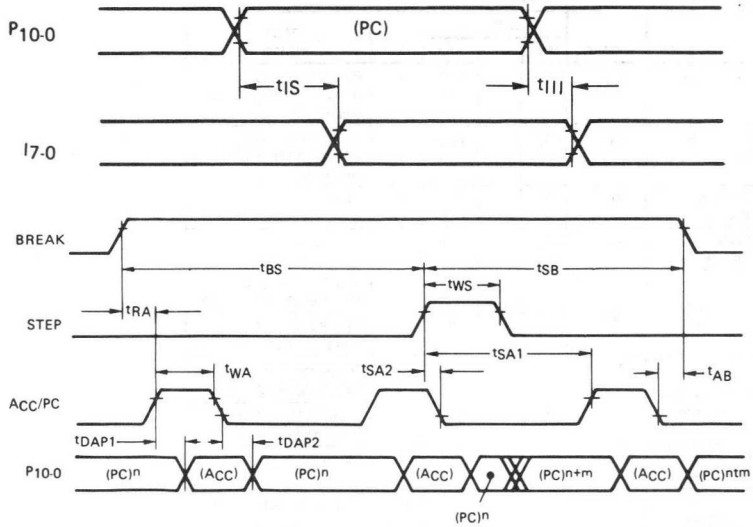
$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Frequency	f	150		440	KHz	
Clock Rise and Fall Times	t_r, t_f	0		0.3	μs	
Clock Pulse Width High	$t_{\phi WH}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi WL}$	0.5		5.6	μs	
Input Setup Time	t_{IS}			5	μs	
Input Hold Time	t_{IH}	0			μs	
BREAK to STEP Interval	t_{BS}	80			tcy	
STEP to RUN Interval	t_{SB}	80			tcy	
STEP Pulse Width	t_{WS}	12			tcy	
BREAK to A_{CC} Interval	t_{BA}	80			tcy	
A_{CC}/PC Pulse Width	t_{WA}	12			tcy	
STEP to A_{CC} Interval	t_{SA1}	80			tcy	
PC to STEP Overlap	t_{SA2}			2	tcy	
PC to RUN Interval	t_{AB}	0			μs	
A_{CC}/PC → P_{10}-P_0 Delay	t_{DAP1}			6	tcy	
	t_{DAP2}			6	tcy	

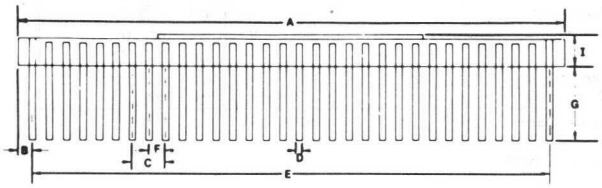
CLOCK WAVEFORM

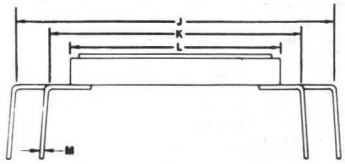


TIMING WAVEFORM



PACKAGE OUTLINE μPD556B





(CERAMIC)

ITEM	MILLIMETERS	INCHES
A	41.5	1.634 MAX
B	1.05	0.042
C	2.54	0.1
D	0.5 ± 0.1	0.2 ± 0.004
E	39.4	1.55
F	1.27	0.05
G	5.4 MIN	0.21 MIN
I	2.35 MAX	0.13 MAX
J	24.13	0.95
K	19.05	0.75
L	15.9	0.626
M	0.25 ± 0.05	0.01 ± 0.002

556DS-12-80-CAT

4-BIT SINGLE CHIP MICROCOMPUTER

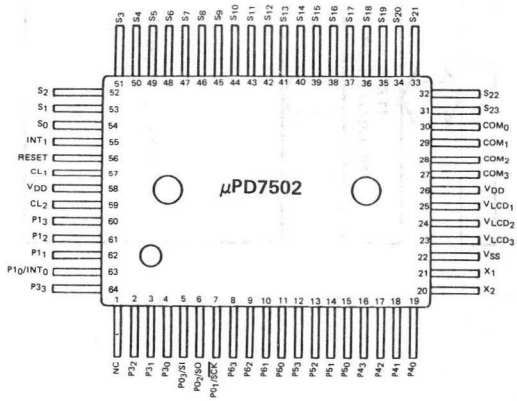
DESCRIPTION

The μPD7502 is a μCOM-75 4-bit single chip microcomputer with a 2048 x 8 ROM, a 128 x 4 RAM, a programmable 8-bit timer/event counter, and 4 vectored, prioritized interrupts. It is also capable of directly driving a 24-segment, 3 or 4-backplane multiplexed Liquid Crystal Display (LCD). The μPD7502 is manufactured with a low-power-consumption CMOS process, allowing use of a single power supply between 2.7 and 5.5V, and providing programmable power-down capability. It has 23 I/O lines, organized into one 3-bit parallel port, five 4-bit parallel ports, and one 8-bit serial port. The μPD7502 executes 92 instructions of the μCOM-75 instruction set, and it is available in a 64-pin plastic flat package.

FEATURES

- 2048 x 8 Bit ROM
- 128 x 4 Bit RAM
- 15 μs Instruction Cycle Time
- 92 Powerful Instructions
  - ROM Data Table Look-up Capability with LHLT and LAMT Instructions
  - Subroutine Address Table Look-up Capability with CALT Instruction
- RAM Stack
- 4 General Purpose 4-Bit Registers (D, E, H and L)
- Extensive I/O Capability
  - One 3-Bit Input Port
  - One 4-Bit Input Port
  - One 4-Bit Output Port
  - Three 4-Bit I/O Ports, of which two are 8-Bit Byte Accessible
  - One 8-Bit Serial I/O Port
- Programmable LCD Controller
  - 24 Segment Outputs and 4-Backplane Outputs
  - Can Directly Drive 3- or 4-Backplane Multiplexed LCDs
  - Automatic Synchronization of Segment and Backplane Signals, Transparent to Program Execution
- Programmable 8-Bit Timer/Event Counter with Crystal Clock Generator
- Vectored, Prioritized Interrupts
  - 2 External
  - 2 Internal (Timer and Serial I/O)
- Programmable Power-Down Operation with HALT and STOP Instructions
- Built-In System Clock Generator
- Built-In Reset Circuitry
- Single Power Supply, Variable from 2.7V to 5.5V
- CMOS Technology
- 64-Pin Plastic Flat Package

PIN CONFIGURATION

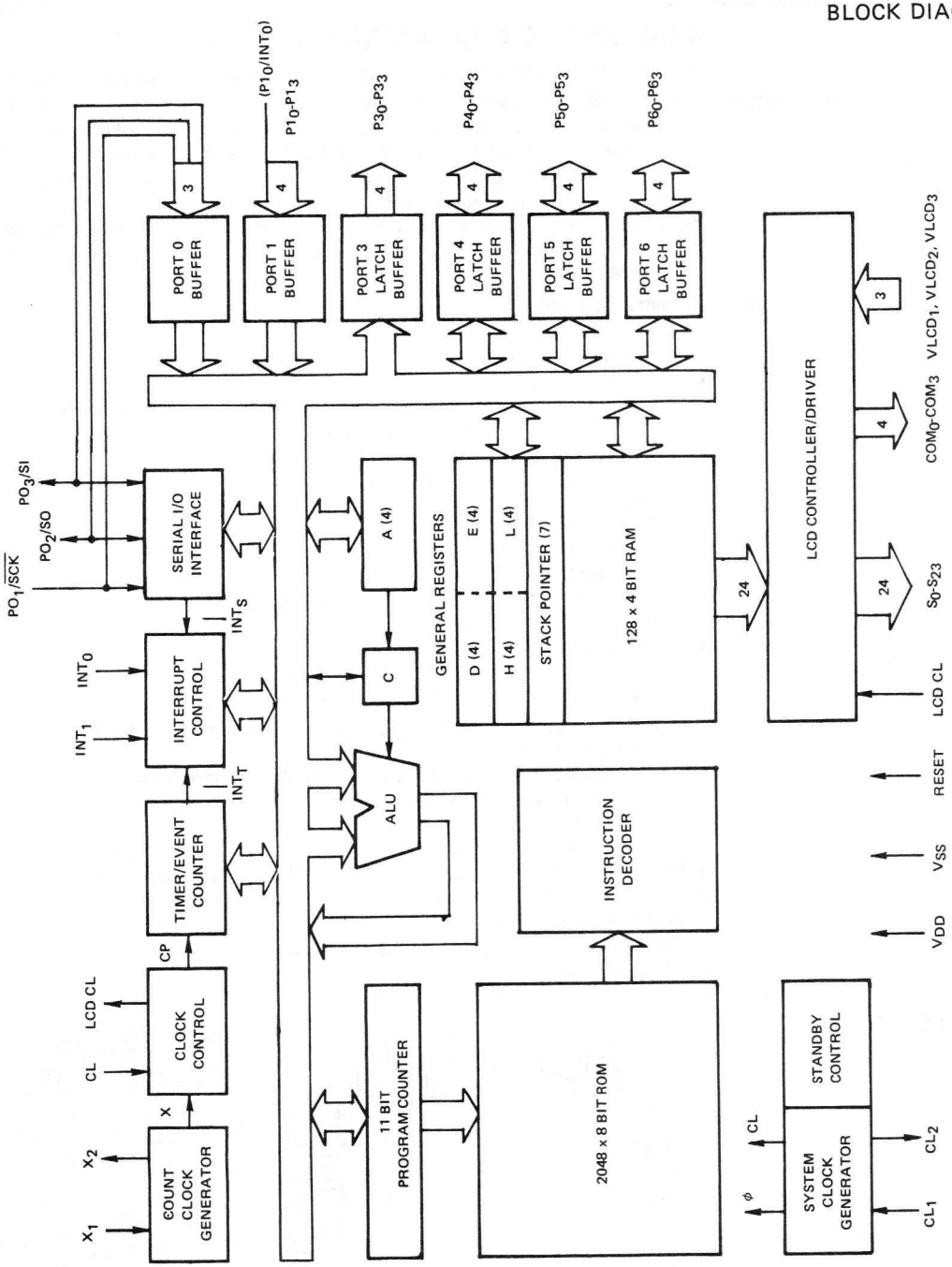


PIN NAMES

S_0-S_{23}	LCD Segment Outputs
COM_0-COM_3	LCD Backplane Outputs
$P0_3$/SI	Input Port 0_3/Serial Input
$P0_2$/SO	Input Port 0_2/Serial Output
$P0_1$/$\overline{SCK}$	Input Port 0_1/Serial Clock
$P1_0$/INT_0	Input Port 1_0/Interrupt 0
INT_1	Interrupt 1
$P1_0$-$P1_3$	Input Port 1
$P3_0$-$P3_3$	Output Port 3
$P4_0$-$P4_3$	Input/Output Port 4
$P5_0$-$P5_3$	Input/Output Port 5
$P6_0$-$P6_3$	Input/Output Port 6
X_1, X_2	Crystal Clock Input, Output
C_1, C_2	System Clock Input, Output
RESET	Reset
V_{LCD_1}-V_{LCD_3}	LCD Power Supply
V_{DD}	Power Supply Positive
V_{SS}	Ground

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BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

ROM

The μPD7502 is equipped with a 2048 x 8 bit general purpose ROM, organized as one large, single field. It is accessible anywhere between addresses 000H and 7FFH by the Program Counter. Several portions of the ROM are reserved for special operations, as follows:

Address	Function
000H	Program start address after RESET Input
010H	Timer/Counter Interrupt (INT_T) Start Address
020H	Serial Interface or External Interrupt ($INT_{0/S}$) Start Address
030H	External Interrupt (INT_1) Start Address
0C0H – 0CFH	LHLT Instruction Reference Table
0D0H – 0FFH	CALT Instruction Reference Table

These ROM addresses can be used for other purposes if these features are not used.

RAM

The μPD7502 is equipped with a 128 x 4 bit general purpose RAM. It is accessible between addressed 00H and 7FH by Direct Addressing with immediate data, by Register Pair Indirect Addressing, or by Stack Pointer Addressing. Two portions of the RAM are reserved for special operations, as follows:

Address	Function
00H – 17H	LCD Segment Data
(Definable by Stack Pointer)	LIFO Stack Address Storage

In addition, there are four general purpose 4-bit registers, D, E, H, and L, which may be used individually, or as register pairs DE, DL, or HL, during program execution.

Clocks

The μPD7502 can accept two different clock signals. Pins CL_1 and CL_2 can accept a simple RC input for the system clock. Pins X_1 and X_2 can accept a more accurate crystal, such as 32.768 kHz, for timer/event counter functions where clock accuracy is important to the application.

Timer/Event Counter

The timer of the μPD7502 is an 8-bit Binary-Up counter. It is reset during execution of RESET, or the "Timer" instruction. During operation, the count register of the timer is incremented until it coincides with the value of the modulus register. At this point, the timer interrupt INT_T becomes active, the count register is reset, and counting begins again. The count register can also be read at any time by executing the "TCNTAM" instruction.

The Event Counter of the μPD7502 takes advantage of the Timer capabilities to measure external pulses occurring on pin X_1.

Interrupts

There are four interrupts available on the μPD7502. Two of them are generated externally (INT_1 and INT_0), and two of them are generated internally (Timer interrupt INT_T, and SIO interrupt INT_S).

Under software control, the four interrupts can be prioritized in any order. They can be controlled individually, or under a master control.

Stack Pointer

The Stack Pointer is a 7-bit register containing the leading address information of the LIFO stack, located in RAM. The Stack Pointer is decremented when CALL, CALT, PSHDE, or PSHHL instructions are executed, and incremented when RT, RTS, TRPSW, POPDE, or POPHL instructions are executed.

The Stack Pointer can be accessed by executing the TAMSP or TSPAM instructions.

Serial I/O

The Serial I/O port of the μPD7502 consists of an 8-bit shift register, a 4-bit shift mode register, and a 3-bit counter. Data is output at the fall of the serial clock, with the MSB transferring first. Serial data input at the rise of the serial clock, with the MSB transferring first. The serial clock $\overline{SCK}$ can be selected under software control from the internal system clock, an external clock signal, or the Timer-Out F/F.

The TSIOAM and TAMSIO instructions facilitate the I/O operations of the μPD7502 SIO port. These instructions make it easy for the μPD7502 to handle odd-sized data containing parity, start or stop bits.

LCD Controller

When direct LCD drive is required for an application, a portion of the RAM must be reserved for LCD segment data storage. This segment data is decoded by ROM table look-up instructions during program execution.

It must then be stored in the RAM, for direct access by the LCD Controller Hardware according to the following pattern:

	SEGMENT																						
BIT	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}	S_{17}	S_{18}	S_{19}	S_{20}	S_{21}	S_{22}	S_{23}	BACKPLANE
0																									COM_0
1																									COM_1
2																									COM_2
3																									COM_3
RAM ADDRESS	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	

For applications using 3-backplane multiplexed LCDs, the third bit of each RAM location is not used, and it may be used for other general purpose storage.

Actual determination of functioning of the LCD Controller occurs when the Display Mode Register is set.

INSTRUCTION SET SYMBOL DEFINITIONS

The following abbreviations are used in the description of the μPD7502

SYMBOL	EXPLANATION AND USE
A	Accumulator
address	Immediate address
A_n	Bit "n" of Accumulator
C	Carry Flag
data	Immediate data
D	Register D
DE	Register Pair DE
DL	Register Pair DL
D_n	Bit "n" of immediate data or immediate address
E	Register E
H	Register H
HL	Register pair HL
IER	Interrupt Enable Register
IME	Interrupt Master Enable F/F
INT_n	Interrupt "n"
L	Register L
P( )	Parallel Input/Output Port addressed by the value within the brackets
PC_n	Bit "n" of Program Counter
PSW	Program Status Word
rp	Register Pair, selected by 3 bits of immediate data, $D_{2\text{-}0}$, as follows:
RQF	Request Flag
S	Number of bytes in next instruction when skip condition occurs
SIO	Serial I/O Shift Register
SIOCR	Serial I/O Count Register
SP	Stack Pointer
TCR	Time Count Register
TMR	Timer Modulo Register
( )	The contents of RAM addressed by the value within the brackets
[ ]	The contents of ROM addressed by the value within the brackets
←	Load, Store, or Transfer
↔	Exchange
−	Complement
∧	LOGICAL AND
∨	LOGICAL OR
∀	LOGICAL Exclusive OR

D_2	D_1	D_0	rp	Additional Action
0	0	0	DL	none
0	0	1	DE	none
1	0	0	HL−	decrement L; skip if L = FH
1	0	1	HL+	increment L; skip if L = 0H
1	1	0	HL	none

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
LOAD													
LAI data	$A \leftarrow D_{3\text{-}0}$	Load A with 4 bits of immediate data [1]	0	0	0	1	D_3	D_2	D_1	D_0	1	1	String
LDI data	$D \leftarrow D_{3\text{-}0}$	Load D with 4 bits of immediate data	0 0	0 0	1 1	1 0	1 D_3	1 D_2	1 D_1	0 D_0	2	2	
LEI data	$E \leftarrow D_{3\text{-}0}$	Load E with 4 bits of immediate data	0 0	0 0	1 0	1 0	1 D_3	1 D_2	1 D_1	0 D_0	2	2	
LHI data	$H \leftarrow D_{3\text{-}0}$	Load H with 4 bits of immediate data	0 0	0 0	1 1	1 1	1 D_3	1 D_2	1 D_1	0 D_0	2	2	
LLI data	$L \leftarrow D_{3\text{-}0}$	Load L with 4 bits of immediate data	0 0	0 0	1 0	1 1	1 D_3	1 D_2	1 D_1	0 D_0	2	2	
LAM rp	$A \leftarrow (rp)$	Load A with the RAM contents addressed by the register pair selected by 3 bits of immediate data	0	1	0	D_2	0	0	D_1	D_0	1	1 + S	See explanation of "rp" in symbol definitions
LADR address	$A \leftarrow (D_{6\text{-}0})$	Load A with the RAM contents addressed by 7 bits of immediate data	0 0	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	0 D_0	2	2	
LDEI data	$DE \leftarrow D_{7\text{-}0}$	Load DE with 8 bits of immediate data	0 D_7	1 D_6	0 D_5	0 D_4	1 D_3	1 D_2	1 D_1	1 D_0	2	2	
LHLI data	$HL \leftarrow D_{7\text{-}0}$	Load HL with 8 bits of immediate data [2]	0 D_7	1 D_6	0 D_5	0 D_4	1 D_3	1 D_2	1 D_1	0 D_0	2	2	String
LHLT address	$H \leftarrow [\uparrow 0001100 D_{3\text{-}0} \uparrow] H$ $L \leftarrow [\uparrow 0001100 D_{3\text{-}0} \uparrow] L$	Load the upper 4 bits of ROM Table Data at address $0001100 D_{3\text{-}0}$ to H; Load the lower 4 bits of ROM Table Data at address $0001100 D_{3\text{-}0}$ to L [3]	1	1	0	0	D_3	D_2	D_1	D_0	1	2	
LAMT	$A \leftarrow [\uparrow PC_{10\text{-}6}, 0, C, A \uparrow] H$ $(HL) \leftarrow [\uparrow PC_{10\text{-}6}, 0, C, A \uparrow] L$	Load the upper 4 bits of ROM Table Data at address $PC_{10\text{-}6}, 0, C, A$ to A; Load the lower 4 bits of ROM Table Data at address $PC_{10\text{-}6}, 0, C, A$ to the RAM location addressed by HL	0	1	0	1	1	1	1	0	1	2	String
STORE													
ST	$(HL) \leftarrow A$	Store A into the RAM location addressed by HL	0	1	0	1	0	1	1	1	1	1	
TRANSFER													
TAD	$D \leftarrow A$	Transfer A to D	0 1	0 0	1 1	1 0	1 1	1 0	1 1	0 0	2	2	
TAE	$E \leftarrow A$	Transfer A to E	0 1	0 0	1 0	1 0	1 1	1 0	1 1	0 0	2	2	
TAH	$H \leftarrow A$	Transfer A to H	0 1	0 0	1 1	1 1	1 1	1 0	1 1	0 0	2	2	
TAL	$L \leftarrow A$	Transfer A to L	0 1	0 0	1 0	1 1	1 1	1 0	1 1	0 0	2	2	
TDA	$A \leftarrow D$	Transfer D to A	0 1	0 0	1 1	1 0	1 1	1 0	1 1	0 1	2	2	
TEA	$A \leftarrow E$	Transfer E to A	0 1	0 0	1 0	1 0	1 1	1 0	1 1	0 1	2	2	
THA	$A \leftarrow H$	Transfer H to A	0 1	0 0	1 1	1 1	1 1	1 0	1 1	0 1	2	2	
TLA	$A \leftarrow L$	Transfer L to A	0 1	0 0	1 0	1 1	1 1	1 0	1 1	0 1	2	2	
EXCHANGE													
XAD	$A \leftrightarrow D$	Exchange A with D	0	1	0	0	1	0	1	0	1	1	
XAE	$A \leftrightarrow E$	Exchange A with E	0	1	0	0	1	0	1	1	1	1	
XAH	$A \leftrightarrow H$	Exchange A with H	0	1	1	1	1	0	1	0	1	1	
XAL	$A \leftrightarrow L$	Exchange A with L	0	1	1	1	1	0	1	1	1	1	
XAM rp	$A \leftrightarrow (rp)$	Exchange A with the RAM contents addressed by the register pair selected by 3 bits of immediate data	0	1	0	D_2	0	1	D_1	D_0	1	1 + S	See explanation of "rp" in symbol definitions

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
XADR address	$A \leftrightarrow (D_{6\text{-}0})$	Exchange A with the RAM contents addressed by 7 bits of immediate data	0 0	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	1 D_0	2	2	
XHDR address	$H \leftrightarrow (D_{6\text{-}0})$	Exchange H with the RAM contents addressed by 7 bits of immediate data	0 0	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	1 D_1	0 D_0	2	2	
XLDR address	$L \leftrightarrow (D_{6\text{-}0})$	Exchange L with the RAM contents addressed by 7 bits of immediate data	0 0	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	1 D_1	1 D_0	2	2	
ARITHMETIC													
AISC data	$A \leftarrow A + D_{3\text{-}0}$ Skip if overflow	Add 4 bits of immediate data to A; Skip if overflow occurs	0	0	0	0	D_3	D_2	D_1	D_0	1	1 + S	Overflow = 1
ASC	$A \leftarrow A + (HL)$ Skip if overflow	Add the RAM contents addressed by HL to A; skip if overflow occurs	0	1	1	1	1	1	0	1	1	1 + S	Overflow = 1
ACSC	$A, C \leftarrow A + (HL) + C$ Skip if carry	Add the RAM contents addressed by HL and the carry flag to A; skip if carry is generated	0	1	1	1	1	1	0	0	1	1 + S	Carry Flag = 1
LOGICAL													
EXL	$A \leftarrow A \veebar (HL)$	Perform a Logical EXCLUSIVE-OR between the RAM contents addressed by HL and A; store the result in A	0	1	1	1	1	1	1	0	1	1	
ANL	$A \leftarrow A \wedge (HL)$	Perform a LOGICAL AND between A and the RAM contents addressed by HL; store the result in A	0 1	0 0	1 1	1 1	1 0	1 0	1 1	1 0	2	2	
ORL	$A \leftarrow A \vee (HL)$	Perform a LOGICAL OR between A and the RAM contents addressed by HL; store the result in A	0 1	0 0	1 1	1 1	1 0	1 1	1 1	1 0	2	2	
ACCUMULATOR													
CMA	$A \leftarrow \overline{A}$	Complement A	0	1	1	1	1	1	1	1	1	1	
RAR	$A_{n-1} \leftarrow A_n$ $(n = 1 \rightarrow 3)$ $C \leftarrow A_0$ $A_3 \leftarrow C$	Rotate A right through Carry Flag	0 1	0 0	1 1	1 1	1 0	1 0	1 1	1 1	2	2	
CARRY FLAG													
RC	$C \leftarrow 0$	Reset Carry Flag	0	1	1	1	1	0	0	0	1	1	
SC	$C \leftarrow 1$	Set Carry Flag	0	1	1	1	1	0	0	1	1	1	
INCREMENT AND DECREMENT													
IES	$E \leftarrow E + 1$ Skip if E = 0H	Increment E; Skip if E = 0H	0	1	0	0	1	0	0	1	1	1 + S	E = 0H
ILS	$L \leftarrow L + 1$ Skip if L = 0H	Increment L; Skip if L = 0H	0	1	0	1	1	0	0	1	1	1 + S	L = 0H
IDRS address	$(D_{6\text{-}0}) \leftarrow (D_{6\text{-}0}) + 1$ Skip if $(D_{6\text{-}0}) = 0H$	Increment the RAM contents addressed by 7 bits of immediate data; Skip if the contents = 0H	0 0	0 D_6	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	1 D_0	2	2 + S	$(D_{6\text{-}0}) = 0H$
DES	$E \leftarrow E - 1$ Skip if E = FH	Decrement E; Skip if E = FH	0	1	0	0	1	0	0	0	1	1 + S	E = FH
DLS	$L \leftarrow L - 1$ Skip if L = FH	Decrement L; Skip if L = FH	0	1	0	1	1	0	0	0	1	1 + S	L = FH
DDRS address	$(D_{6\text{-}0}) \leftarrow (D_{6\text{-}0}) - 1$ Skip if $(D_{6\text{-}0}) = FH$	Decrement the RAM contents addressed by 7 bits of immediate data; skip if the contents = FH	0 0	0 D_6	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	0 D_0	2	2 + S	$(D_{6\text{-}0}) = FH$
BIT MANIPULATION													
RMB	$(HL)_{bit} \leftarrow 0$	Reset a single bit of RAM at the location addressed by HL, denoted by D_1D_0, to zero	0	1	1	0	1	0	D_1	D_0	1	1	
SMB	$(HL)_{bit} \leftarrow 1$	Set a single bit of RAM at the location addressed by HL, denoted by D_1D_0, to one	0	1	1	0	1	1	D_1	D_0	1	1	

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
JUMP, CALL AND RETURN													
JMP address	$PC_{10-0} \leftarrow D_{10-0}$	Jump to the address specified by 11 bits of immediate data	0	0	1	0	0	D_{10}	D_9	D_8	2	2	
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
JCP address	$PC_{5-0} \leftarrow D_{5-0}$	Jump to the address specified by the higher-order bits PC_{10-6} of the PC, and 6 bits of immediate data	1	0	D_5	D_4	D_3	D_2	D_1	D_0	1	1	
JAM address	$PC_{10-8} \leftarrow D_{2-0}$ $PC_{7-4} \leftarrow A$ $PC_{3-0} \leftarrow (HL)$	Jump to the address specified by 3 bits of immediate data, A, and the RAM contents addressed by HL	0	0	1	1	1	1	1	1	2	2	
			0	0	0	1	0	D_2	D_1	D_0			
CALL address	$(SP-1) \leftarrow PC_{7-4}$ $(SP-2) \leftarrow PC_{3-0}$ $(SP-3) \leftarrow PSW$ $(SP-4) \leftarrow PC_{10-8}$ $PC_{10-0} \leftarrow D_{10-0}$ $SP \leftarrow SP-4$	Store a return address in the stack; call the subroutine program at the location specified by 11 bits of immediate data	0	0	1	1	0	D_{10}	D_9	D_8	2	2	
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
CALT address	$(SP-1) \leftarrow PC_{7-4}$ $(SP-2) \leftarrow PC_{3-0}$ $(SP-3) \leftarrow PSW$ $(SP-4) \leftarrow PC_{10-8}$ $PC_{10} \leftarrow 0$ $PC_{9-7} \leftarrow [00011D_{5-0}]_{7-5}$ $PC_{6-5} \leftarrow 00$ $PC_{4-0} \leftarrow [00011D_{5-0}]_{4-0}$ $SP \leftarrow SP-4$	Store a return address in the stack; LOAD ROM Subroutine Address Table data at address $00011D_{5-0}$ to PC; call the subroutine program at the location specified by the PC	1	1	D_5	D_4	D_3	D_2	D_1	D_0	1	2	
RT	$PC_{10-8} \leftarrow (SP)$ $PC_{7-4} \leftarrow (SP+3)$ $PC_{3-0} \leftarrow (SP+2)$ $SP \leftarrow SP+4$	Return from Subroutine	0	1	0	1	0	0	1	1	1	1	
RTS	$PC_{10-8} \leftarrow (SP)$ $PC_{7-4} \leftarrow (SP+3)$ $PC_{3-0} \leftarrow (SP+2)$ $SP \leftarrow SP+4$ Skip unconditionally	Return from Subroutine; skip unconditionally	0	1	0	1	1	0	1	1	1	1 + S	Unconditional
RTPSW	$PC_{10-8} \leftarrow (SP)$ $PC_{7-4} \leftarrow (SP+3)$ $PC_{3-0} \leftarrow (SP+2)$ $PSW \leftarrow (SP+1)$ $SP \leftarrow SP+4$	Return from Subroutine and restore PSW	0	1	0	0	0	0	1	1	1	2	
STACK													
PSHDE	$(SP-1) \leftarrow D$ $(SP-2) \leftarrow E$ $SP \leftarrow SP-2$	Push DE on to stack	0	0	1	1	1	1	1	0	2	2	
			1	0	0	0	1	1	1	0			
PSHHL	$(SP-1) \leftarrow H$ $(SP-2) \leftarrow L$ $SP \leftarrow SP-2$	Push HL on to stack	0	0	1	1	1	1	1	0	2	2	
			1	0	0	1	1	1	1	0			
POPDE	$E \leftarrow (SP)$ $D \leftarrow (SP+1)$ $SP \leftarrow SP+2$	Pop DE off the stack	0	0	1	1	1	1	1	0	2	2	
			1	0	0	0	1	1	1	1			
POPHL	$L \leftarrow (SP)$ $H \leftarrow (SP+1)$ $SP \leftarrow SP+2$	Pop HL off the stack	0	0	1	1	1	1	1	0	2	2	
			1	0	0	1	1	1	1	1			
TAMSP	$SP_{7-4} \leftarrow A$ $SP_{3-1} \leftarrow (HL)_{3-1}$	Transfer A and RAM contents addressed by HL to stack	0	0	1	1	1	1	1	1	2	2	
			0	0	1	1	0	0	0	1			
TSPAM	$A \leftarrow SP_{7-4}$ $(HL)_{3-1} \leftarrow SP_{3-1}$ $(HL)_0 \leftarrow 0$	Transfer stack to A and RAM contents addressed by HL	0	0	1	1	1	1	1	1	2	2	
			0	0	1	1	0	1	0	1			
SKIP													
SKC	Skip if C = 1	Skip if Carry Flag is true	0	1	0	1	1	0	1	0	1	1 + S	C = 1
SKMBT data	Skip if $(HL)_{bit} = 1$	Skip if the single bit of the RAM location addressed by HL, denoted by D_1D_0, is true	0	1	1	0	0	1	D_1	D_0	1	1 + S	$(HL)_{bit} = 1$
SKABT data	Skip if $A_{bit} = 1$	Skip if the single bit of A, denoted by D_1D_0, is true	0	1	1	1	0	1	D_1	D_0	1	1 + S	$A_{bit} = 1$
SKMBF data	Skip if $(HL)_{bit} = 0$	Skip if the single bit of the RAM location addressed by HL, denoted by D_1D_0, is false	0	1	1	0	0	0	D_1	D_0	1	1 + S	$(HL)_{bit} = 0$
SKAEM	Skip if A = (HL)	Skip if A equals the RAM contents addressed by HL	0	1	0	1	1	1	1	1	1	1 + S	A = (HL)

INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
SKAEI data	Skip if A = data	Skip if A equals 4 bits of immediate data	0 0	0 1	1 1	1 0	1 D_3	1 D_2	1 D_1	1 D_0	2	2 + S	A = data
SKDEI data	Skip if D = data	Skip if D equals 4 bits of immediate data	0 0	0 1	1 1	1 0	1 D_3	1 D_2	1 D_1	0 D_0	2	2 + S	D = data
SKEEI data	Skip if E = data	Skip if E equals 4 bits of immediate data	0 0	0 1	1 0	1 0	1 D_3	1 D_2	1 D_1	0 D_0	2	2 + S	E = data
SKHEI data	Skip if H = data	Skip if H equals 4 bits of immediate data	0 0	0 1	1 1	1 1	1 D_3	1 D_2	1 D_1	0 D_0	2	2 + S	H = data
SKLEI data	Skip if L = data	Skip if L equals 4 bits of immediate data	0 0	0 1	1 0	1 1	1 D_3	1 D_2	1 D_1	0 D_0	2	2 + S	L = data
		TIMER											
TAMMOD	$TMR_{7-4} \leftarrow A$ $TMR_{3-0} \leftarrow (HL)$	Transfer A and the RAM contents addressed by HL to Timer Modulo Register	0 0	0 0	1 1	1 1	1 1	1 1	1 1	1 1	2	2	
TIMER	$TCR_{7-0} \leftarrow 0$ $INT_T RQF \leftarrow 0$	Start Timer Operation	0 0	0 0	1 1	1 1	1 0	1 0	1 1	1 0	2	2	
TCNTAM	$A \leftarrow TCR_{7-4}$ $(HL) \leftarrow TCR_{3-0}$	Transfer Timer Count Register to A and the RAM contents addressed by HL	0 0	0 0	1 1	1 1	1 1	1 0	1 1	1 1	2	2	
		INTERRUPT											
EI data	$IER \leftarrow IER \vee D_{2-0}$ if $D_{2-0} = 0$, $IME \leftarrow 1$	Enable Interrupt specified by 3 bits of immediate data. If the immediate data D_{2-0} is 0, set the Interrupt Master Enable F/F.	0 1	0 0	1 0	1 1	1 0	1 D_2	1 D_1	1 D_0	2	2	
DI data	$IER \leftarrow IER \wedge \overline{D_{2-0}}$ if $D_{2-0} = 0$, $IME \leftarrow 0$	Disable Interrupt specified by 3 bits of immediate data. If the immediate data D_{2-0} is 0, reset the Interrupt Master Enable F/F.	0 1	0 0	1 0	1 0	1 0	1 D_2	1 D_1	1 D_0	2	2	
SKI data	Skip if $INT_n RQF \wedge D_{2-0} \neq 0$ $INT_n \leftarrow RFQ \wedge \overline{D_{2-0}}$	Test Interrupt Request Flag specified by 3 bits of immediate data; skip if Interrupt Request Flag is true; Reset the Interrupt Request Flag.	0 0	0 1	1 0	1 0	1 0	1 D_2	1 D_1	1 D_0	2	2 + S	INT_n RFQ = 1
		SERIAL I/O											
TAMSIO	$SIO_{7-4} \leftarrow A$ $SIO_{3-0} \leftarrow (HL)$	Transfer A and the RAM contents addressed by HL to SIO Shift Register	0 0	0 0	1 1	1 1	1 1	1 1	1 1	1 0	2	2	
TSIOAM	$A \leftarrow SIO_{7-4}$ $(HL) \leftarrow SIO_{3-0}$	Transfer SIO Shift Register data to A and the RAM contents addressed by HL	0 0	0 0	1 1	1 1	1 1	1 0	1 1	1 0	2	2	
SIO	$SIOCR_{2-0} \leftarrow 0$ $INT_{0/S} RQF \leftarrow 0$	Start Serial I/O Operation	0 0	0 0	1 1	1 1	1 0	1 0	1 1	1 1	2	2	
		PARALLEL I/O											
IPL	$A \leftarrow P(L)$	Input the Port addressed by L to A	0	1	1	1	0	0	0	0	1	1	
IP address	$A \leftarrow P(D_{3-0})$	Input the Port addressed by 4 bits of immediate data to A	0 1	0 1	1 0	1 0	1 D_3	1 D_2	1 D_1	1 D_0	2	2	
IP1	$A \leftarrow P1$	Input Port 1 to A	0	1	1	1	0	0	0	1	1	1	
IP54	$A \leftarrow P5_{3-0}$ $(HL) \leftarrow P4_{3-0}$	Input Port 5 to A; Input Port 4 to the RAM location addressed by HL	0 0	0 0	1 1	1 1	1 1	1 0	1 0	1 0	2	2	
OPL	$P(L) \leftarrow A$	Output A to the port addressed by L	0	1	1	1	0	0	1	0	1	1	
OP address	$P(D_{3-0}) \leftarrow A$	Output A to the port addressed by 4 bits of immediate data	0 1	0 1	1 1	1 0	1 D_3	1 D_2	1 D_1	1 D_0	2	2	
OP3	$P3 \leftarrow A$	Output A to Port 3	0	1	1	1	0	0	1	1	1	1	
OP54	$P5_{3-0} \leftarrow A$ $P4_{3-0} \leftarrow (HL)$	Output A to Port 5; Output the RAM contents addressed by HL to Port 4	0 0	0 0	1 1	1 1	1 1	1 1	1 0	1 0	2	2	
ANP data	$P(D_{7-4}) \leftarrow P(D_{7-4}) \wedge D_{3-0}$	Perform a LOGICAL AND between the port addressed by 4 bits of immediate data and an additional 4 bits of immediate data; output the result to the same port	0 D_7	1 D_6	0 D_5	0 D_4	1 D_3	1 D_2	0 D_1	0 D_0	2	2	
ORP	$P(D_{7-4}) \leftarrow P(D_{7-4}) \vee D_{3-0}$	Perform a LOGICAL OR between the port addressed by 4 bits of immediate data and an additional 4 bits of immediate data; output the result to the same port	0 D_7	1 D_6	0 D_5	0 D_4	1 D_3	1 D_2	0 D_1	1 D_0	2	2	
		CPU CONTROL											
NOP		Perform no operation; consume one machine cycle	0	0	0	0	0	0	0	0	1	1	
HALT		Enter HALT Mode	0 0	0 0	1 1	1 1	1 0	1 1	1 1	1 0	2	2	
STOP		Enter STOP Mode	0 0	0 0	1 1	1 1	1 0	1 1	1 1	1 1	2	2	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Power Supply Voltage	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to +7.3V
Output Current (Device Total)	I_{OH} = mA
	I_{OL} = mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS	
Input Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	PORT, RESET, SI, $\overline{SCK}$, INT_0, INT_1	
	V_{IL}	0		0.3 V_{DD}			
	V_{X_H}	V_{DD} −0.5		V_{DD}	V	X_1, External Pulse Input	
	V_{X_L}	0		0.5			
Clock Voltage	$V_{\phi H}$	V_{DD} −0.5		V_{DD}	V	CL_1, External Clock	
	$V_{\phi L}$	0		0.5			
Input Leakage Current	I_{LI_H}			1	μA	PORT, RESET, SI,	Vin = V_{DD}
	I_{LI_L}			−1		$\overline{SCK}$, INT_0, INT_1	Vin = 0V
	I_{LX_H}			10	μA	X_1	Vin = V_{DD}
	I_{LX_L}			−10			Vin = 0V
Clock Leakage Current	$I_{L\phi_H}$			10	μA	CL_1	Vin = V_{DD}
	$I_{L\phi_L}$			−10			Vin = 0V
Output Voltage					V	PORT, SO, $\overline{SCK}$	
	V_{O_H}	V_{DD} −1.0				V_{DD} = 5V ± 10% , I_{OH} = −1.0 mA	
		V_{DD} −0.5				V_{DD} = 2.7 to 5.5V , I_{OH} = −100 μA	
	V_{O_L}			0.4	V	V_{DD} = 5V ± 10% , I_{OL} = 1.6 mA	
				0.5		V_{DD} = 2.7 to 5.5V , I_{OL} = 400 μA	
Output Leakage Current	I_{LO_H}			1	μA	PORT, SO, $\overline{SCK}$	V_O = V_{DD}
	I_{LO_L}			−1		Output Into High Impedance	V_O = 0V
Output Impedance	R_{COM}			5	kΩ	COM_0 to COM_3 ①	V_{DD} = 5V ± 10%
			5	50			V_{DD} = 3V ± 10%
	R_{SEG}			20	kΩ	S_0 to S_{23} ①	V_{DD} = 5V ± 10%
			20				V_{DD} = 3V ± 10%
Supply Current (All Outputs Open)	I_{DD_O}		400	900		Operating Mode	V_{DD} = 5V ± 10%
			200	400			V_{DD} = 3V ± 10%
	I_{DD_H}		100	250	μA	HALT Mode	V_{DD} = 5V ± 10%
			40	100			V_{DD} = 3V ± 10%
	I_{DD_S}		20	40		STOP Mode	V_{DD} = 5V ± 10%
			5	10			V_{DD} = 3V ± 10%

Note: ① 2.7V ≤ V_{LCD} ≤ V_{DD}

AC CHARACTERISTICS

T_a = −10°C to +70°C; V_{DD} = 2.7V to 5.5V

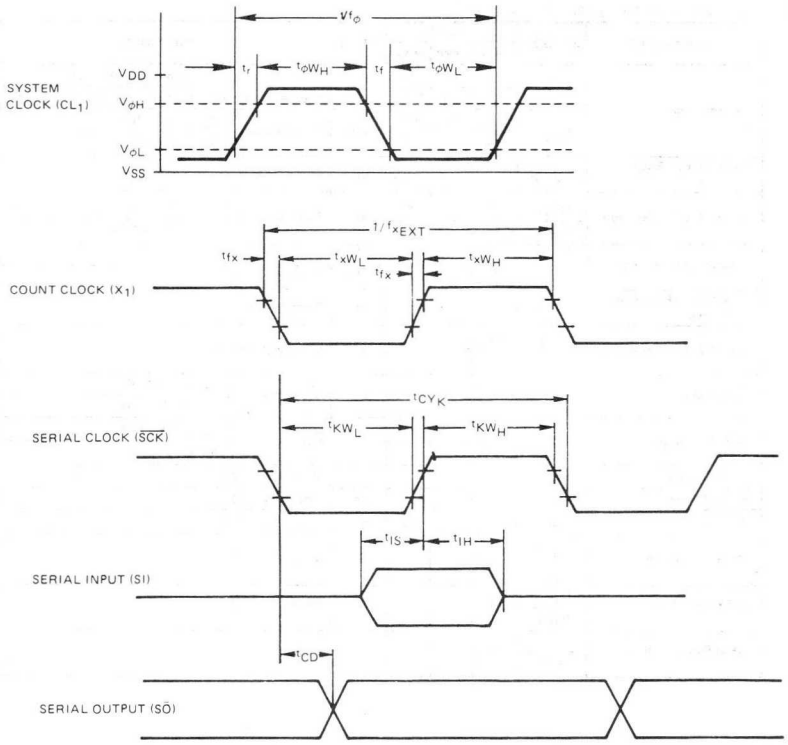
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS	
System Clock Frequency	f_ϕ	90	130	170	kHz	V_{DD} = 5V ± 10%, C = 33 pF ± 5%, R = 160 kΩ ± 2%	
		90	80	105		V_{DD} = 2.7 to 5.5V, C = 33 pF ± 5%, R = 240 kΩ ± 2%	
	$f_{\phi Ext}$	10	130	200	kHz	External Clock	V_{DD} = 5V ± 10%
		10	80	120			V_{DD} = 3V ± 10%
System Clock Rise and Fall Times	$t_{r\phi}$, $t_{f\phi}$			0.2	μs	External Clock	
System Clock Pulse Width	$t_{\phi W_H}$	23		50	μs	External Clock	V_{DD} = 5V ± 10%
	$t_{\phi W_L}$	40		50			V_{DD} = 2.7 to 5.5V
Count Clock Frequency	f_x	25	32	50	kHz	Crystal Oscillator	
	f_{xExt}	DC	32	200	kHz	External Pulse Input	
Count Clock Pulse Rise and Fall Times	t_{rx}, t_{fx}			0.2	μs	External Clock	
Count Clock Pulse Width	t_{xW_H}	23			μs	External Pulse Input	
	t_{xW_L}	23					
$\overline{SCK}$ Cycle	t_{CY_K}	4.0			μs	$\overline{SCK}$ Input	V_{DD} = 5V ± 10%
		6.0					V_{DD} = 3V ± 10%
$\overline{SCK}$ Pulse Width	t_{KW_H}	1.8			μs	$\overline{SCK}$ Input	V_{DD} = 5V ± 10%
	t_{KW_L}	3.0					V_{DD} = 3V ± 10%
SI Setup Time	t_{IS}	300			ns	V_{DD} = 5V ± 10%	
SI Hold Time	t_{IH}	450			ns	V_{DD} = 5V ± 10%	
SO Delay Time	t_{OD}			850	ns	V_{DD} = 5V ± 10%	
INT_0 Pulse Width	$t_{I_0W_H}$	10			μs	V_{DD} = 5V ± 10%	
	$t_{I_0W_L}$						
INT_1 Pulse Width	$t_{I_1W_H}$	10			μs	V_{DD} = 5V ± 10%	
	$t_{I_1W_L}$						
Reset Pulse Width	t_{RW_H}	10			μs	V_{DD} = 5V ± 10%	
	t_{RW_L}						

CAPACITANCE

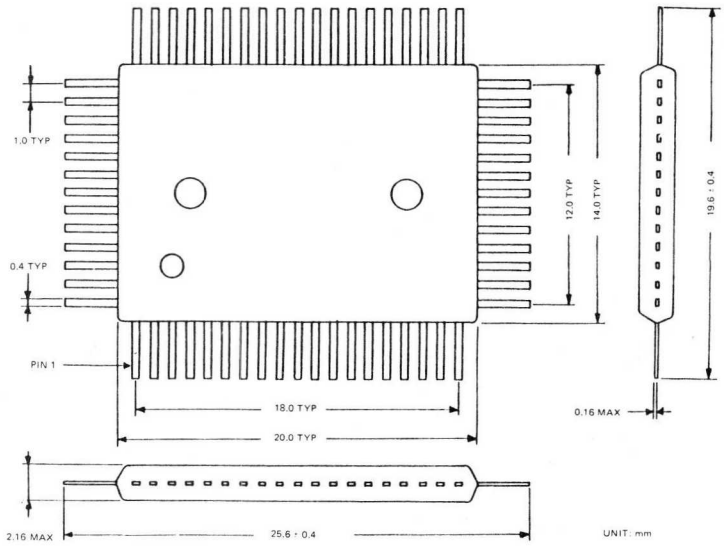
T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
Input Capacitance	C_I			20	pF	
Output Capacitance	C_O			20	pF	
System Clock Capacitance	C_ϕ			20	pF	

TIMING WAVEFORMS



PACKAGE
DIMENSIONS
μPD7502G



6

NOTES

4-BIT SINGLE CHIP MICROCOMPUTER

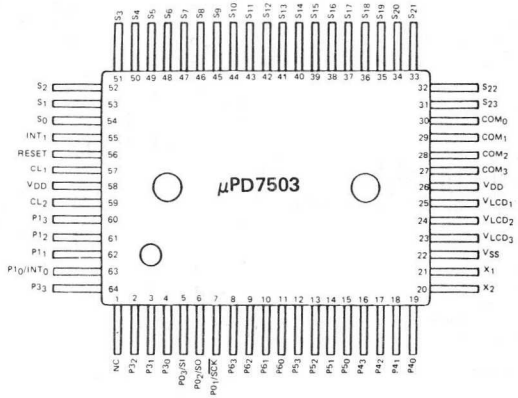
DESCRIPTION

The μPD7503 is a μCOM-75 4-bit single chip microcomputer with a 4096 x 8 ROM, a 224 x 4 RAM, a programmable 8-bit timer/event counter, and 4 vectored, prioritized interrupts. It is also capable of directly driving a 24-segment, 3 or 4-backplane multiplexed Liquid Crystal Display (LCD). The μPD7503 is manufactured with a low-power-consumption CMOS process, allowing use of a single power supply between 2.7V and 5.5V, and providing programmable power-down capability. It has 23 I/O lines, organized into one 3-bit parallel port, five 4-bit parallel ports, and one 8-bit serial port. The μPD7503 executes 92 instructions of the μCOM-75 instruction set, and it is available in a 64-pin plastic flat package.

FEATURES

- 4096 x 8 Bit ROM
- 224 x 4 Bit RAM
- 15 μs Instruction Cycle Time
- 92 Powerful Instructions
  - Table Look-up Capability with LHLT and LAMTL instructions
  - Indirect indexed addressing with CALT instruction
- RAM Stack
- Extensive I/O Capability
  - One 3-Bit Input Port
  - One 4-Bit Input Port
  - One 4-Bit Output Port
  - Three 4-Bit I/O Ports, of which two are 8-Bit Byte Accessible
  - One 8-Bit Serial I/O Port
- Programmable LCD Controller
  - 24 Segment Outputs and 4-Backplane Outputs
  - Can Directly Drive 3- or 4-Backplane Multiplexed LCDs
  - Automatic Synchronization of Segment and Backplane Signals, Transparent to Program Execution
- Programmable 8-Bit Timer/Event Counter with Crystal Clock Generator
- Vectored, Prioritized Interrupts
  - 2 External
  - 2 Internal (Timer and Serial I/O)
- Programmable Power-Down Operation with HALT and STOP Instructions
- Built-In System Clock Generator
- Built-In Reset Circuitry
- Single Power Supply, Variable from 2.7V to 5.5V
- CMOS Technology
- 64-Pin Plastic Flat Package

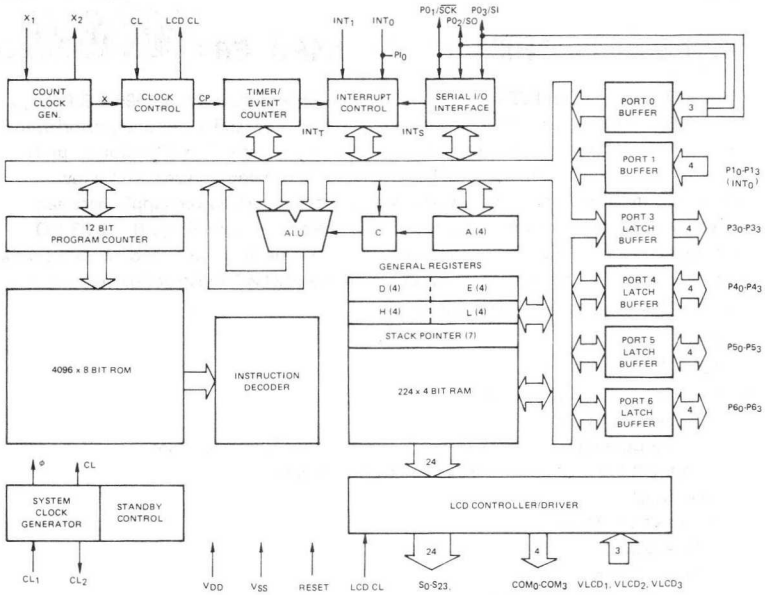
PIN CONFIGURATION



PIN NAMES

S_0-S_{23}	LCD Segment Outputs
COM_0-COM_3	LCD Backplane Outputs
$P0_1$/SCK	Input Port 0_1/Serial Clock
$P0_2$/SO	Input Port 0_2/Serial Output
$P0_3$/SI	Input Port 0_3/Serial Input
$P1_0$/INT_0	Input Port 1_0/Interrupt 0
$P1_0$-$P1_3$	Input Port 1
$P3_0$-$P3_3$	Output Port 3
$P4_0$-$P4_3$	Input/Output Port 4
$P5_0$-$P5_3$	Input/Output Port 5
$P6_0$-$P6_3$	Input/Output Port 6
INT_1	Interrupt 1
X_1, X_2	Crystal Clock Input, Output
C_1, C_2	System Clock Input, Output
RESET	Reset
V_{LCD_1}-V_{LCD_3}	LCD Power Supply
V_{DD}	Power Supply Positive
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM

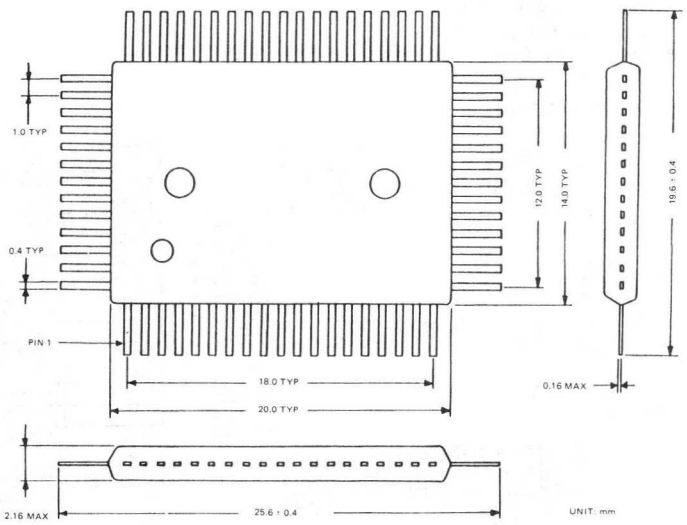


INSTRUCTION SET

The μPD7503 executes the identical instruction set of the μPD7502, with only two exceptions. First, all instructions referencing the 11-bit Program Counter PC_{10-0} of the μPD7502 will now refer to the 12-bit Program Counter PC_{11-0} of the μPD7503. Second, the LAMTL instruction below replaces the μPD7502 LAMT instruction.

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	BYTES	CYLCES	SKIP CONDITION
LOAD													
LAMTL	$A \leftarrow (PC_{10-8}, A, (HL))_H$	Load the upper 4 bits of ROM Table Data at address PC_{10-8},A,(HL) to A;	0	0	1	1	1	1	1	1	2	3	
	$(HL) \leftarrow (PC_{10-8}, A, (HL))_L$	Load the lower 4 bits of ROM Table Data at address PC_{10-8},A,(HL) to the RAM location addressed by HL	0	0	1	1	0	1	0	0			

PACKAGE OUTLINE μPD7503G



4-BIT SINGLE CHIP MICROCOMPUTER

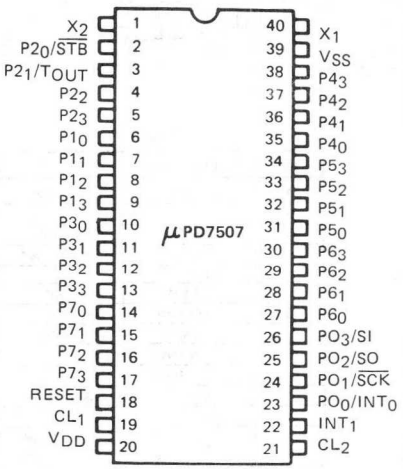
DESCRIPTION

The μPD7507 is a μCOM-75 4-bit single chip microcomputer with a 2048 x 8 ROM, a 128 x 4 RAM, a programmable 8-bit timer/event counter, and 4 vectored, prioritized interrupts. The μPD7507 is manufactured with a low power consumption CMOS process, allowing use of a single power supply between 2.7V and 5.5V, and providing programmable power-down capability. It has 32 I/O lines, organized into eight 4-bit parallel ports and one 8-bit serial port. The μPD7507 executes 92 instructions of the μCOM-75 instruction set, and it is available in a 40 pin dual-in-line package.

FEATURES

- 2048 x 8 Bit ROM
- 128 x 4 Bit RAM
- 10 μs Instruction Cycle Time
- 92 Powerful Instructions
  - Table Look-Up Capability with LHLT and LAMTL Instructions
  - Indirect Indexed Addressing with CALT Instruction
- RAM Stack
- Extensive I/O Capability
  - One 4-Bit Input Port
  - Two 4-Bit Output Ports
  - Four 4-Bit I/O Ports, of which two are 8-Bit Byte Accessible
  - One 4-Bit I/O Port with Output Strobe
  - One 8-Bit Serial I/O Port
- Programmable 8-Bit Timer/Event Counter with Crystal Clock Generator
- Vectored, Prioritized Interrupts
  - 2 External
  - 2 Internal (Timer and Serial I/O)
- Programmable Power-Down Operation with HALT and STOP Instructions
- Built-In System Clock Generator
- Built-In Reset Circuitry
- Single Power Supply, Variable from 2.7V to 5.5V
- CMOS Technology
- 40-Pin Dual-In-Line Package

PIN CONFIGURATION

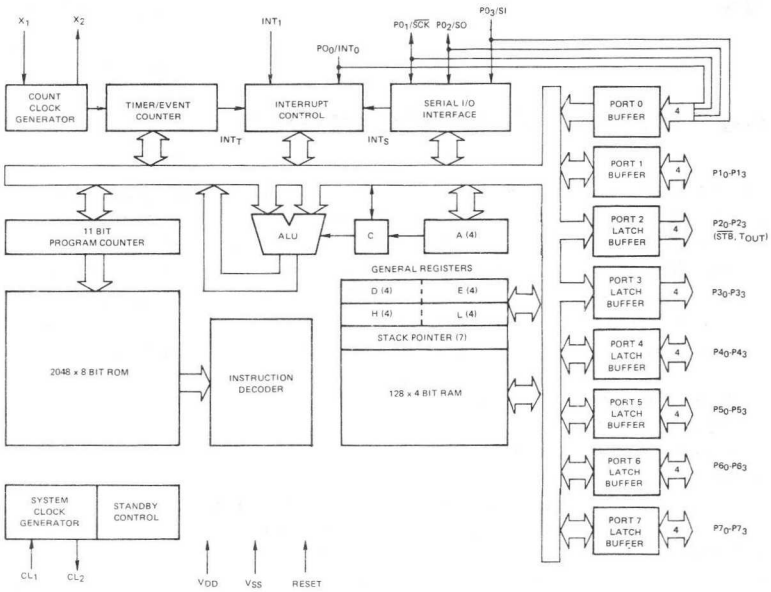


PIN NAMES

$P0_0/INT_0$	Input Port 0_0/Interrupt 0
$P0_1/\overline{SCK}$	Input Port 0_1/Serial Clock
$P0_2/SO$	Input Port 0_2/Serial Output
$P0_3/SI$	Input Port 0_3/Serial Input
$P1_0$-$P1_3$	Input/Output Port 1
$P2_0/\overline{STB}$	Output Port 2_0/Port 1 Strobe Output
$P2_1/T_{OUT}$	Output Port 2_1/Timer Output
$P2_0$-$P2_3$	Output Port 2
$P3_0$-$P3_3$	Output Port 3
$P4_0$-$P4_3$	Input/Output Port 4
$P5_0$-$P5_3$	Input/Output Port 5
$P6_0$-$P6_3$	Input/Output Port 6
$P7_0$-$P7_3$	Input/Output Port 7
INT_1	Interrupt 1
C_1, C_2	System Clock Input, Output
X_1, X_2	Crystal Clock Input, Output
RESET	Reset
V_{DD}	Power Supply Positive
V_{SS}	Ground

6

BLOCK DIAGRAM

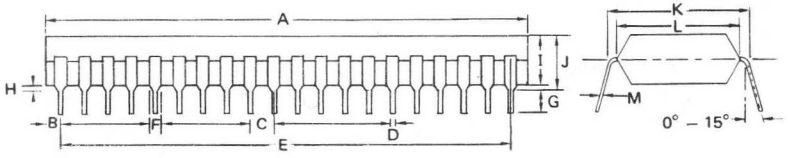


INSTRUCTION SET

The μPD7507 executes the identical instruction set of the μPD7502, with the sole exception being that the LAMTL instruction below replaces the μPD7502 LAMT instruction.

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
LOAD													
LAMTL	$A \leftarrow [PC_{10\text{-}8}.A.(HL)]_H$	Load the upper 4 bits of ROM Table Data at address $PC_{10\text{-}8}.A.(HL)$ to A;	0	0	1	1	1	1	1	1	2	3	
	$(HL) \leftarrow [PC_{10\text{-}8}.A.(HL)]_L$	Load the lower 4 bits of ROM Table Data at address $PC_{10\text{-}8}.A.(HL)$ to the RAM location addressed by HL	0	0	1	1	0	1	0	0			

PACKAGE OUTLINE μPD7507C



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

4-BIT SINGLE CHIP MICROCOMPUTER

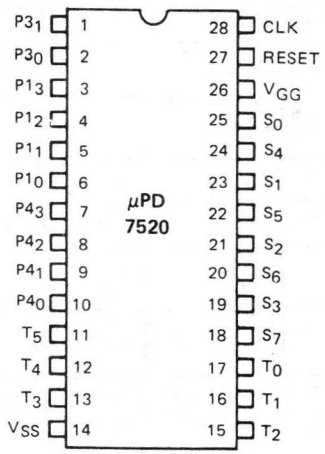
DESCRIPTION

The μPD7520 is a μCOM-75 4-bit single chip microcomputer with a Programmable Display Controller capable of directly driving a multiplexed 8-segment, 8-digit LED Display. It has a 768 x 8 ROM, a 48 x 4 RAM, and 24 I/O lines for communication with and control of external circuitry. The μPD7520 is manufactured with a low-power consumption PMOS process, allowing use of a single power supply between −6V and −10V. The μPD7520 executes 47 instructions of the μCOM-75 instruction set, and is available in a low-cost 28-pin plastic dual-in-line package.

FEATURES

- 768 x 8 Bit ROM
- 48 x 4 Bit RAM
- 20 μs Instruction Cycle Time, Typical
- 47 Powerful Instructions
  - Table Look-Up Capability with LAMT Instruction
- 2-Level Subroutine Stack
- One 4-Bit Input Port
- One 4-Bit I/O Port
- One 2-Bit Output Port (Capable of Driving Piezo Element)
- Programmable Display Controller
  - 6 LED Direct Digit Drive Outputs (8 Possible Using $P4_{0-1}$)
  - 8 LED Direct Segment Drive Outputs
  - Selection of a 4, 5, 6, or 8-Digit Display Strobe Cycle
  - Can Directly Drive 8-Segment, Multiplexed Displays, or up to an 8 x 8 Dot Matrix
  - Automatic Synchronization of Segment and Digit Signals, Transparent to Program Execution
  - Segment Outputs also Function as Latched, 8-Bit Parallel Output Port
- Built-In Clock Signal Generation Circuitry
- Built-In Reset Circuitry
- Single Power Supply, Variable from −6V to −10V
- Low Power Consumption: 45 mW, Typical
- P-Channel MOS Technology
- 28-Pin Plastic Dip

PIN CONFIGURATION



PIN NAMES

$S_0 - S_7$	Segment Drive Output Port S
$T_0 - T_5$	Digit Drive Output Port T
$P1_0 - P1_3$	Input Port 1
$P3_0 - P3_1$	Output Port 3
$P4_0 - P4_3$	Input/Output Port 4
CLK	Clock Input
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Ground

6

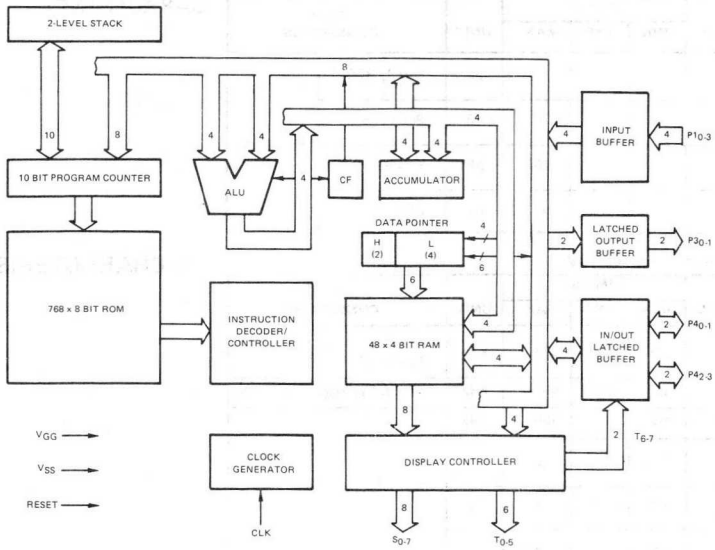
DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{GG} = −6V to −10V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS	
Input Voltage High	V_{IH}			−2	V	Ports 1, 4, RESET	V_{GG} = −9V ± 1V
				−1.8			V_{GG} = −6V to −10V
Input Voltage Low	V_{IL}	V_{GG}+1.5			V	Ports 1, 4, RESET	V_{GG} = −9V ± 1V
		V_{GG}+0.8					V_{GG} = −6V to −10V
Clock Voltage High	$V_{\phi H}$			−0.8	V	CLK, External Clock	
Clock Voltage Low	$V_{\phi L}$	−5.0			V	CLK, External Clock	
Input Current High	I_{IH}	45		200	μA	Port 1, RESET	V_I = 0V, V_{GG} = −9V ± 1V
		40		200			V_I = 0V, V_{GG} = −6V to −10V
Input Leakage Current High	I_{LIH}			+5	μA	Port 4, V_I = 0V	
Input Leakage Current Low	I_{LIL_1}			−5	μA	Port 1, RESET, V_I = −10V, V_{GG} = −10V	
	I_{LIL_2}			−5	μA	Port 4, V_I = −10V	
Clock Current High	$I_{\phi H}$			0.5	mA	CLK, External Clock, $V_{\phi H}$ = 0V, V_{GG} = −9V ± 1V	
Clock Current Low	$I_{\phi L}$			−2.1	mA	CLK, External Clock, $V_{\phi L}$ = −5V, V_{GG} = −9V ± 1V	
Output Voltage Low	V_{OL}	V_{GG}+0.5			V	Port 3, No Load	
Output Current High	I_{OH_1}	−1.0			mA	Port 3,	V_O = −1.0V, V_{GG} = −9V ± 1V
		−0.6					V_O = −1.0V, V_{GG} = −6V
	I_{OH_2}	−2.0			mA	Port 4,	V_O = −1.0V, V_{GG} = −9V ± 1V
		−1.2					V_O = −1.0V, V_{GG} = −6V
	I_{OH_3}	−5	−10		mA	Port S,	V_O = −2.0V, V_{GG} = −9V ± 1V
		−3	−6				V_O = −2.0V, V_{GG} = −6V
		−1	−3				V_O = −1.0V, V_{GG} = −6V to −10V
	I_{OH_4}	−24	−48		mA	Port T,	V_O = −2.0V, V_{GG} = −9V ± 1V
		−13	−27				V_O = −1.0V, V_{GG} = −9V ± 1V ①
		−9	−18				V_O = −1.0V, V_{GG} = −6V
Output Current Low	I_{OL_1}	1	2		mA	Port 3,	V_O = V_{GG} + 1.5V, V_{GG} = −9V ± 1V ①
		0.1	0.2				V_O = V_{GG} + 3.5V, V_{GG} = −9V ± 1V
		0.3	0.6				V_O = −4.5V, V_{GG} = −6V ①
		0.1	0.2				V_O = −2.5V, V_{GG} = −6V
	I_{OL_2}	4.5	9		mA	Port S,	V_O = V_{GG} + 5.0V, V_{GG} = −9V ± 1V
		1	2				V_O = V_{GG} + 3.5V, V_{GG} = −6V to −10V
Output Leakage Current High	I_{LOH}			+5	μA	Ports 4, T, V_O = 0V	
Output Leakage Current Low	I_{LOL}			−5	μA	Ports 4, T, V_O = −10V	
Supply Current	I_{GG}		−5	−9.8	mA	T_a = 25°C, V_{GG} = −9V, No Load	

Note: ① Current within 2.5 ms after turning to the low level (T_a = 25°C).

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Internal Registers

The ALU, the Accumulator, and the Carry Flag together comprise the central portion of the μPD7520 architecture. The ALU performs the arithmetic and logical operations, and checks for various results. The Accumulator stores the results generated by the ALU, and acts as the major interface point between the RAM, the I/O ports, and the H and L registers. The Carry Flag can be addressed directly, and can be set during an addition.

Data Pointer Registers

The 2-bit H register and 4-bit L register are two registers which reside externally to the 48 x 4 bit RAM. They function as the Data Pointer, addressing the rows and columns of the RAM, respectively. They are individually accessible, and the L register can be automatically incremented or decremented.

RAM

The μPD7520 has a static 48 x 4 bit RAM organized into 3 rows by 16 columns. The RAM is used for general purpose data storage or data transfers, and is also used to store Display Data for access by the segment latch of the Display Controller.

ROM

The ROM is the mask-programmable portion of the μPD7520 which stores the application program. It is organized into a single 768 x 8 bit field. Execution of the program resident in the ROM is independent of field or page boundary limitations.

Program Counter and Stack Register

The Program Counter is a 10-bit register which contains the address of a particular instruction being executed. It is incremented during normal operation, but can be modified by various JUMP and CALL instructions. The Stack Register is a LIFO push-down stack register used to save the value of the Program Counter when a subroutine is called. It is organized as 2 words x 10 bits to accommodate 2 levels of subroutine calls.

CAPACITANCE

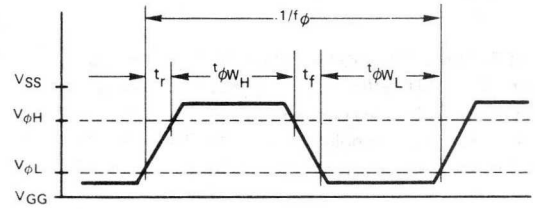
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS	
Input Capacitance	C_I			15	pF	Port 1, RESET	f = 1 MHz
Output Capacitance	C_O			20	pF	Ports 3, S, T,	
Input/Output Capacitance	C_{IO}			20	pF	Port 4	
Clock Capacitance	C_ϕ			30	pF	CLK	

AC CHARACTERISTICS

T_a = -10°C to +70°C, V_{GG} = -6V to -10V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Frequency	f_{osc}	225	300	375	kHz	R_f = 1MΩ, V_{GG} = -9V ± 1V, T_a = 25°C
		180	300	450	kHz	R_f = 1MΩ, V_{GG} = -9V ± 1V
	f_ϕ	100		330	kHz	CLK, External Clock
Clock Rise and Fall Times	t_r, t_f			2	μs	
Clock Pulse Width High	$t_{\phi W_H}$	1.5		3	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	1.5		3	μs	

CLOCK WAVEFORM



DEVELOPMENT TOOLS

The NEC Microcomputers' NDS Development System is available for the development of software source code, editing, and assembly into object code. In addition, the ASM-75 Cross Assembler is available for systems supporting the ISIS-II (TM Intel Corp.) Operating System, and the CASM-75 Cross Assembler is available for systems supporting the CP/M (® Digital Research Corp.) Operating System.

The EVAKIT-7520 Evaluation Board is available for production device evaluation and prototype system debugging.

Clock and Reset Circuitry

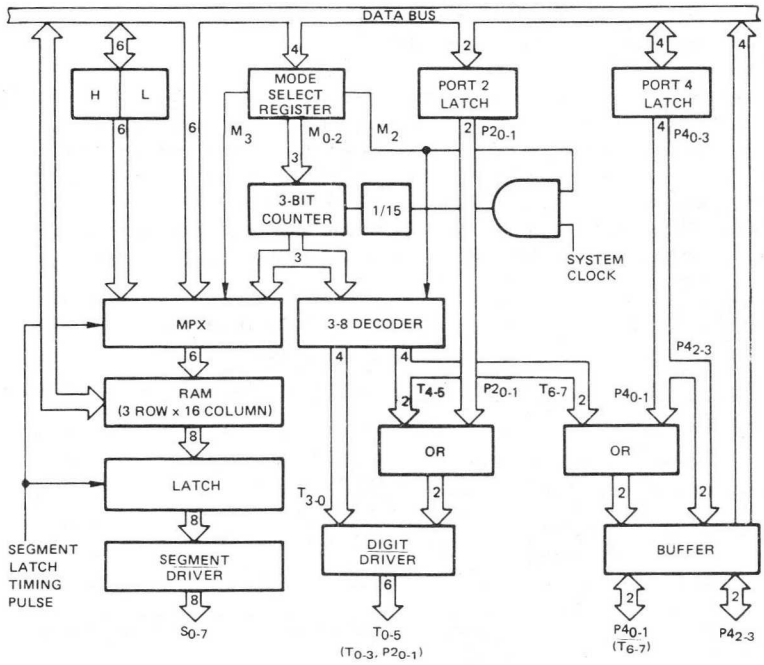
The Clock Circuitry for the μPD7520 can be implemented by connecting a resistor from the CLK input to V_{GG}. The Power-On-Reset Circuitry for the μPD7520 can be implemented by connecting a capacitor from the RESET input to V_{SS}.

I/O Capability

The μPD7520 has 24 I/O lines for communication with and control of external circuitry. The Port configuration is selectable under software control via the Mode Select Register as follows:

Port 1	$P1_{0-3}$	4-Bit Schmidt Input
Port 2	$P2_{0-1}$	2-Bit Latched Output Option, Accessible through Port T (T_{4-5})
Port 3	$P3_{0-1}$	2-Bit Latched Output
Port 4	$P4_{0-3}$	4-Bit Input/Latched Output
Port S	S_{0-7}	Latched 8-Bit Parallel/Segment Drive Output
Port T	T_{0-5}	6-Bit High-Current/Digit Drive Output
	T_{6-7}	Additional 2-Bit Digit Drive Output Option, Accessible through Port 4 ($P4_{0-1}$)

DISPLAY CONTROLLER BLOCK DIAGRAM



μPD7520

DISPLAY CONTROLLER

The Display Controller is the major feature of the μPD7520. It automatically performs scan or display strobe operations which would otherwise require considerable software.

The Display Controller interfaces to a common-anode LED display without external components. Connections from the Display Controller to the display are made from Port S to the cathodes (segments), and from Port T to the anodes (digit enables). Up to 6 digits can be driven directly by the μPD7520 in this manner. A total of 8 digit drives are available by using the two digit drives accessible through Port 4_{0-1}, and adding only two small driver transistors and four resistors externally. When Port T_{4-5} is not used to drive a display, it may be used as a high current driver, accessible through Port 2_{0-1}.

During operation, a 3-to-8 decoder selects which digit of a Display Buffer in the RAM will be multiplexed onto the display. The contents of the pair of RAM locations, corresponding to the digit chosen from the Display Buffer, are transferred to the 8 latched outputs of Port S, and the corresponding Port T digit drive is enabled. After 13 machine cycles have been completed, the digit drive is disabled, the decoder is updated to select the next digit of the Display Buffer to be multiplexed onto the display, and this cycle is repeated. Thus, the μPD7520 program needs only to load the properly decoded display data into the Display Buffer and it immediately appears on the display. Operation in this manner is completely transparent to the μPD7520, and requires no intervention once the proper display mode has been selected.

The use of a Mode Select Register enhances the utility of the Display Controller by allowing a choice of a 4, 5, 6, or 8 digit display strobe cycle output, or a direct latched output. A choice can also be made between one of the two possible Display Buffers, resident in either Row 0 or Row 2 of the RAM.

MODE SELECT REGISTER

The Mode Select Register (MSR) is a separate 4-bit register of the Display Controller which determines the function that the Display Controller will perform. The value of the MSR can range from 0_{16} to F_{16}, and it can be modified by data in the Accumulator. This is accomplished by execution of the OPL (output-to-port) instruction, where L (the lower 4-bits of the data pointer) is set to the value B_{16} in order to address the MSR. Execution of this instruction transfers the contents of the Accumulator into the MSR, and the Display Controller begins operating according to the following table:

M_3	M_2	M_1	M_0	DISPLAY CONTROLLER OPERATION
0	0	0	0	Reset (S_{0-7}: High level); (T_{0-5}: OFF)
0	0	0	1	8-bit parallel output: $S_{0-3} \leftarrow$ (0EH); $S_{4-7} \leftarrow$ (0FH); (T_{0-3}: OFF)
0	0	1	0	Not used
0	0	1	1	Not used
0	1	0	0	4-digit display (T_{0-3}); Segment data: 00H-07H
0	1	0	1	5-digit display (T_{0-4}); Segment data: 00H-09H
0	1	1	0	6-digit display (T_{0-5}); Segment data: 00H-0BH
0	1	1	1	8-digit display (T_{0-7}); Segment data: 00H-0FH
1	0	0	0	Not used
1	0	0	1	8-bit parallel output: $S_{0-3} \leftarrow$ (2EH); $S_{4-7} \leftarrow$ (2FH); (T_{0-3}: OFF)
1	0	1	0	Not used
1	0	1	1	Not used
1	1	0	0	4-digit display (T_{0-3}); Segment data: 20H-27H
1	1	0	1	5-digit display (T_{0-4}); Segment data: 20H-29H
1	1	1	0	6-digit display (T_{0-5}); Segment data: 20H-2BH
1	1	1	1	8-digit display (T_{0-7}); Segment data: 20H-2FH

The MSB, M_3, of the Mode Select Register defines the Row of RAM (0 or 2) to be used for the Display Buffer and M_2 distinguishes between a digit strobe cycle output, or a direct latched output.

INSTRUCTION SET SYMBOL DEFINITIONS

The following abbreviations are used in the description of the μPD7520 instruction set:

SYMBOL	EXPLANATION AND USE
A	Accumulator
address	Immediate address
C	Carry Flag
data	Immediate data
D_n	Bit "n" of immediate data or immediate address
H	Register H
HL	Register pair HL
L	Register L
P( )	Parallel Input/Output Port addressed by the value within the brackets
PC_n	Bit "n" of Program Counter
S	Number of bytes in next instruction when Skip Condition occurs
STACK	Stack Register
( )	The contents of RAM addressed by the value within the brackets
[ ]	The contents of ROM addressed by the value within the brackets
←	Load, Store, or Transfer
↔	Exchange
–	Complement
∀	LOGICAL Exclusive-OR

INSTRUCTION SET

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
LOAD													
LAI data	$A \leftarrow D_{3-0}$	Load A with 4 bits of immediate data; execute succeeding LAI instructions as NOP instructions	0	0	0	1	D_3	D_2	D_1	D_0	1	1	String
LHI data	$H \leftarrow D_{1-0}$	Load H with 2 bits of immediate data	0	0	1	0	1	0	D_1	D_0	1	1	
LHLI data	$HL \leftarrow D_{4-0}$	Load HL with 5 bits of immediate data; execute succeeding LHLI instructions as NOP instructions	1	1	0	D_4	D_3	D_2	D_1	D_0	1	1	String
LAMT	$A \leftarrow [PC_{9-6}, 0, C, A]_H$	Load the upper 4 bits of ROM Table Data at address PC_{9-6}, 0, C, A to A	0	1	0	1	1	1	1	0	1	2	
	$(HL) \leftarrow [PC_{9-6}, 0, C, A]_L$	Load the lower 4 bits of ROM Table Data at address PC_{9-6}, 0, C, A to the RAM location addressed by HL											
L	$A \leftarrow (HL)$	Load A with the contents of RAM addressed by HL	0	1	0	1	0	0	1	0	1	1	
LIS	$A \leftarrow (HL)$ $L = L + 1$ Skip if L = 0H	Load A with the contents of RAM addressed by HL; increment L; skip if L = 0H	0	1	0	1	0	0	0	1	1	1 + S	L = 0H
LDS	$A \leftarrow (HL)$ $L = L - 1$ Skip if L = FH	Load A with the contents of RAM addressed by HL; decrement L; skip if L = FH	0	1	0	1	0	0	0	0	1	1 + S	L = FH
LADR address	$A \leftarrow (D_{5-0})$	Load A with the contents of RAM addressed by 6 bits of immediate data	0 0	0 0	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	0 D_0	2	2	
STORE													
ST	$(HL) \leftarrow A$	Store A into the RAM location addressed by HL	0	1	0	1	0	1	1	1	1	1	
STII data	$(HL) \leftarrow D_{3-0}$ $L \leftarrow L + 1$	Store 4 bits of immediate data into the RAM location addressed by HL; increment L	0	1	0	0	D_3	D_2	D_1	D_0	1	1	

INSTRUCTION SET
(CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								BYTES	CYCLES	SKIP CONDITION
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
EXCHANGE													
XAH	$A_{1-0} \leftrightarrow H_{1-0}$ $A_{3-2} \leftarrow 00H$	Exchange A with H	0	1	1	1	1	0	1	0	1	1	
XAL	$A \leftrightarrow L$	Exchange A with L	0	1	1	1	1	0	1	1	1	1	
X	$A \leftrightarrow (HL)$	Exchange A with the contents of RAM addressed by HL	0	1	0	1	0	1	1	0	1	1	
XIS	$A \leftrightarrow (HL)$ $L \leftarrow L + 1$ Skip if L = 0H	Exchange A with the contents of RAM addressed by HL; increment L; skip if L = 0H	0	1	0	1	0	1	0	1	1	1 + S	L = 0H
XDS	$A \leftrightarrow (HL)$ $L \leftarrow L - 1$ Skip if L = FH	Exchange A with the contents of RAM addressed by HL; decrement L; skip if L = FH	0	1	0	1	0	1	0	0	1	1 + S	L = FH
XADR address	$A \leftrightarrow (D_{5-0})$	Exchange A with the contents of RAM addressed by 6 bits of immediate data	0 0	0 0	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	1 D_0	2	2	
ARITHMETIC AND LOGICAL													
AISC data	$A \leftarrow A + D_{3-0}$ Skip if overflow	Add 4 bits of immediate data to A; Skip if overflow is generated	0	0	0	0	D_3	D_2	D_1	D_0	1	1 + S	Overflow
ASC	$A \leftarrow A + (HL)$ Skip if overflow	Add the contents of RAM addressed by HL to A; skip if overflow is generated	0	1	1	1	1	1	0	1	1	1 + S	Overflow
ACSC	$A, C \leftarrow A + (HL) + C$ Skip if C = 1	Add the contents of RAM addressed by HL and the carry flag to A; skip if carry is generated	0	1	1	1	1	1	0	0	1	1 + S	C = 1
EXL	$A \leftarrow A \veebar (HL)$	Perform a LOGICAL Exclusive–OR operation between the contents of RAM addressed by HL and A; store the result in A	0	1	1	1	1	1	1	0	1	1	
ACCUMULATOR AND CARRY FLAG													
CMA	$A \leftarrow \overline{A}$	Complement A	0	1	1	1	1	1	1	1	1	1	
RC	$C \leftarrow 0$	Reset Carry Flag	0	1	1	1	1	0	0	0	1	1	
SC	$C \leftarrow 1$	Set Carry Flag	0	1	1	1	1	0	0	1	1	1	
INCREMENT AND DECREMENT													
ILS	$L \leftarrow L + 1$ Skip if L = 0H	Increment L; Skip if L = 0H	0	1	0	1	1	0	0	1	1	1 + S	L = 0H
IDRS address	$(D_{5-0}) \leftarrow (D_{5-0}) + 1$ Skip if (D_{5-0}) = 0H	Increment the contents of RAM addressed by 6 bits of immediate data; Skip if the contents = 0H	0 0	0 0	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	1 D_0	2	2 + S	(D_{5-0}) = 0H
DLS	$L \leftarrow L - 1$ Skip if L = FH	Decrement L; Skip if L = FH	0	1	0	1	1	0	0	0	1	1 + S	L = FH
DDRS address	$(D_{5-0}) \leftarrow (D_{5-0}) - 1$ Skip if (D_{5-0}) = FH	Decrement the contents of RAM addressed by 6 bits of immediate data, skip if the contents = FH	0 0	0 0	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	0 D_0	2	2 + S	(D_{5-0}) = FH
BIT MANIPULATION													
RMB data	$(HL)_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1D_0) of the RAM location addressed by HL to zero	0	1	1	0	1	0	D_1	D_0	1	1	
SMB data	$(HL)_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of the RAM location addressed by HL to one	0	1	1	0	1	1	D_1	D_0	1	1	
JUMP, CALL, AND RETURN													
JMP address	$PC_{9-0} \leftarrow D_{9-0}$	Jump to the address specified by 10 bits of immediate data	0 D_7	0 D_6	1 D_5	0 D_4	0 D_3	0 D_2	D_9 D_1	D_8 D_0	2	2	
JAM data	$PC_{9-8} \leftarrow D_{1-0}$ $PC_{7-4} \leftarrow A$ $PC_{3-0} \leftarrow (HL)$	Jump to the address specified by 2 bits of immediate data, A, and the RAM contents addressed by HL	0 0	0 0	1 0	1 1	1 0	1 0	1 D_1	1 D_0	2	2	
JCP address	$PC_{5-0} \leftarrow D_{5-0}$	Jump to the address specified by the higher-order bits PC_{9-6} of the PC, and 6 bits of immediate data	1	0	D_5	D_4	D_3	D_2	D_1	D_0	1	1	

INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								BYTES	CYCLES	SKIP CONDITION
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
CALL address	STACK ← PC + 2 PC_{9-0} ← D_{9-0}	Store a return address (PC + 2) in the stack; call the subroutine program at the location specified by 10 bits of immediate data	0 D_7	0 D_6	1 D_5	1 D_4	0 D_3	0 D_2	D_9 D_1	D_8 D_0	2	2	
CAL address	STACK ← PC + 1 PC_{9-0} ← $01D_4D_3$ $000D_2D_1D_0$	Store a return address (PC + 1) in the stack; call the subroutine program at one of the 32 special locations specified by 5 bits of immediate data	1	1	1	D_4	D_3	D_2	D_1	D_0	1	1	
RT	PC ← STACK	Return from Subroutine	0	1	0	1	0	0	1	1	1	1	
RTS	PC ← STACK Skip unconditionally	Return from Subroutine; skip unconditionally	0	1	0	1	1	0	1	1	1	1 + S	Unconditional
SKIP													
SKC	Skip if C = 1	Skip if carry flag is true	0	1	0	1	1	0	1	0	1	1 + S	C = 1
SKMBT data	Skip if $(HL)_{bit}$ = 1	Skip if the single bit (denoted by D_1D_0) of the RAM location addressed by HL is true	0	1	1	0	0	1	D_1	D_0	1	1 + S	$(HL)_{bit}$ = 1
SKMBF data	Skip if $(HL)_{bit}$ = 0	Skip if the single bit (denoted by D_1D_0) of the RAM location addressed by HL is false	0	1	1	0	0	0	D_1	D_0	1	1 + S	$(HL)_{bit}$ = 0
SKABT data	Skip if A_{bit} = 1	Skip if the single bit (denoted by D_1D_0) of A is true	0	1	1	1	0	1	D_1	D_0	1	1 + S	A_{bit} = 1
SKAEI data	Skip if A = data	Skip if A equals 4 bits of immediata data	0 0	0 1	1 1	1 0	1 D_3	1 D_2	1 D_1	1 D_0	2	2 + S	A = data
SKAEM	Skip if A = (HL)	Skip if A equals the RAM contents addressed by HL	0	1	0	1	1	1	1	1	1	1 + S	A = (HL)
PARALLEL I/O													
IPL	A ← P(L)	Input the Port addressed by L to A	0	1	1	1	0	0	0	0	1	1	
IP1	A ← P1	Input Port 1 to A	0	1	1	1	0	0	0	1	1	1	
OPL	P(L) ← A	Output A to the port addressed by L	0	1	1	1	0	0	1	0	1	1	
OP3	P3 ← A_{1-0}	Output the lower 2 bits of A to Port 3	0	1	1	1	0	0	1	1	1	1	
CPU CONTROL													
NOP		Perform no operation; consume one machine cycle	0	0	0	0	0	0	0	0	1	1	

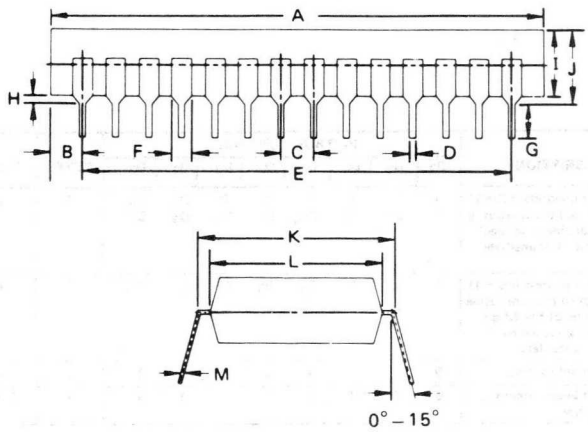
ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10° to +70°C
Storage Temperature	−40° to +125°C
Supply Voltage	−15 to +0.3 Volts
Input Voltage	−15 to +0.3 Volts
Output Voltage	−15 to +0.3 Volts
Output Current (I_{OH} Total)	−100 mA
(I_{OL} Total)	90 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

PACKAGE OUTLINE
μPD7520C



PLASTIC

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$

4-BIT MICROPROCESSOR
μPD750X EVALUATION CHIP

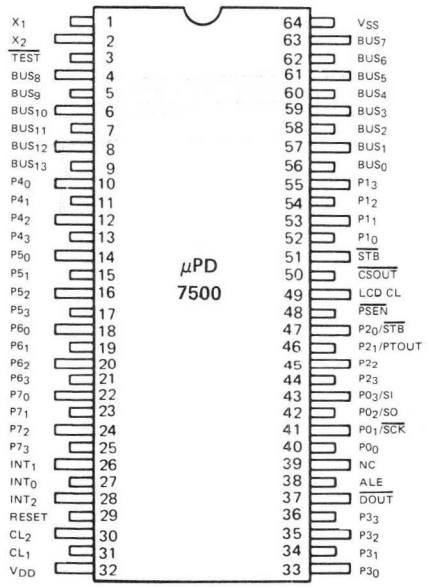
DESCRIPTION

The μPD7500 is a μCOM-75 4-bit microprocessor with a 256 x 4 RAM, a programmable 8-bit timer/event counter, and 5 vectored, prioritized interrupts. It is capable of addressing 8,192 bytes of external memory, and also functions as the prototype Evaluation Chip for the μPD750X family of 4-bit single chip microcomputers. The μPD7500 is manufactured with a low-power-consumption CMOS process, allowing use of a single power supply between 2.7 and 5.5V, and providing programmable power-down capability. It has 46 I/O lines, organized into eight 4-bit parallel ports, one 14-bit parallel address/instruction port, and one 8-bit serial port. The μPD7500 executes 102 instructions of the μCOM-75 instruction set, and it is available in a 64 pin quad-in-line package.

FEATURES

- 4-Bit Microprocessor
- Evaluation Chip for μPD750X Family of 4-Bit Single Chip Microcomputers
- Addresses up to 8,192 Bytes of External Memory
- 256 x 4 Bit RAM
- 10 μs Instruction Cycle Time
- 102 Powerful Instructions
  - Table Look-up Capability with LHLT and LAMTL instructions
  - Indirect indexed addressing with CALT instruction
- RAM Stack
- Extensive I/O Capability
  - One 4-Bit Input Port
  - Two 4-Bit Output Ports
  - Four 4-Bit I/O Ports, of which two are 8-Bit Byte Accessible
  - One 4-Bit I/O Port with Output Strobe
  - One 14-Bit Address/Instruction Port
  - One 8-Bit Serial I/O Port
- Programmable 8-Bit Timer/Event Counter with Crystal Clock Generator
- Vectored, Prioritized Interrupts
  - 3 External
  - 2 Internal (Timer and Serial I/O)
- Programmable Power-Down Operation with HALT and STOP Instructions
- Built-In System Clock Generator
- Built-In Reset Circuitry
- Single Power Supply, Variable from 2.7V to 5.5V
- CMOS LSI
- 64-Pin Quad-In-Line Package

PIN CONFIGURATION

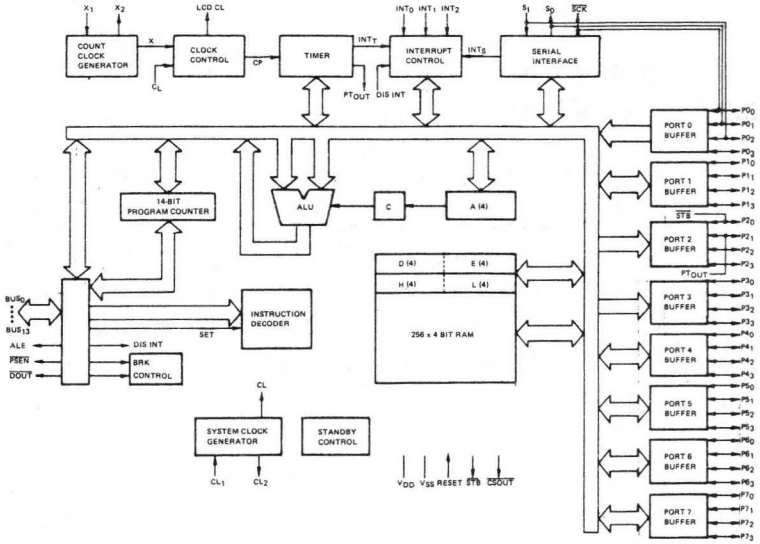


PIN NAMES

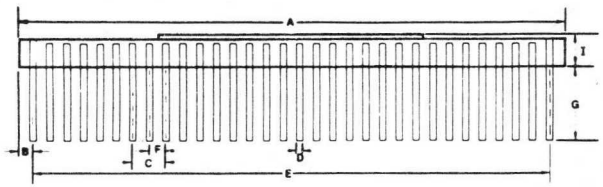
BUS_0-BUS_{13}	Address/Instruction Bus
$P0_0$	Input Port 0_0
$P0_1$/SCK	Input Port 0_1/Serial Clock
$P0_2$/SO	Input Port 0_2/Serial Output
$P0_3$/SI	Input Port 0_3/Serial Input
$P1_0$-$P1_3$	Input/Output Port 1
$P2_0$/STB	Output Port 2_0/Port 1 Strobe Output
$P2_1$/PT_{OUT}	Output Port 2_1/Timer Output
$P2_0$-$P2_3$	Output Port 2
$P3_0$-$P3_3$	Output Port 3
$P4_0$-$P4_3$	Input/Output Port 4
$P5_0$-$P5_3$	Input/Output Port 5
$P6_0$-$P6_3$	Input/Output Port 6
$P7_0$-$P7_3$	Input/Output Port 7
INT_0	Interrupt Input 0
INT_1	Interrupt Input 1
INT_2	Interrupt Input 2
CL_1, CL_2	System Clock Input, Output
X_1, X_2	Crystal Clock Input, Output
ALE	Address LATCH ENABLE
CSOUT	Chip Select Output
DOUT	
LCD CL	LCD Clock Output
PSEN	Program Store ENABLE
STB	Strobe 1
RESET	Reset
V_{DD}	Power Supply Positive
V_{SS}	Ground
TEST	Factory Test Pin
NC	No Connection

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BLOCK DIAGRAM

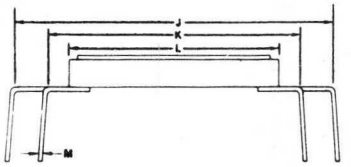


PACKAGE OUTLINE μPD7500B



Ceramic

ITEM	MILLIMETERS	INCHES
A	41.5	1.634 MAX
B	1.05	0.042
C	2.54	0.1
D	0.5 ± 0.1	0.2 ± 0.004
E	39.4	1.55
F	1.27	0.05
G	5.4 MIN	0.21 MIN
I	2.35 MAX	0.13 MAX
J	24.13	0.95
K	19.05	0.75
L	15.9	0.626
M	0.25 ± 0.05	0.01 ± 0.002



HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER ROM-LESS DEVELOPMENT DEVICE

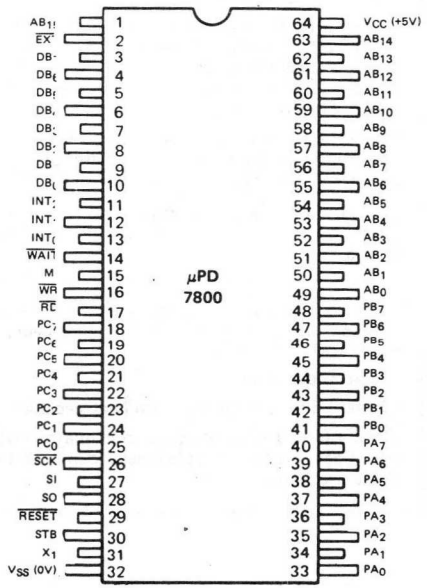
DESCRIPTION

The NEC μPD7800 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-channel Silicon Gate MOS Technology. Intended as a ROM-less development device for NEC μPD7801/7802 designs, the μPD7800 can also be used as a powerful microprocessor in volume production enabling program memory flexibility. Basic on-chip functional blocks include 128 bytes of RAM data memory, 8-bit ALU, 32 I/O lines, Serial I/O port, and 12-bit timer. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of 8080A/8085A peripheral and memory products. Total memory address space is 64K bytes.

FEATURES

- NMOS Silicon Gate Technology Requiring Single +5V Supply.
- Single-Chip Microcomputer with On-Chip ALU, RAM and I/O
  - 128 Bytes RAM
  - 32 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five-Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 64K Byte Memory Address Range
- Wait State Capability
- Alternate Z80™ Type Register Set
- Powerful 140 Instruction Set
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities

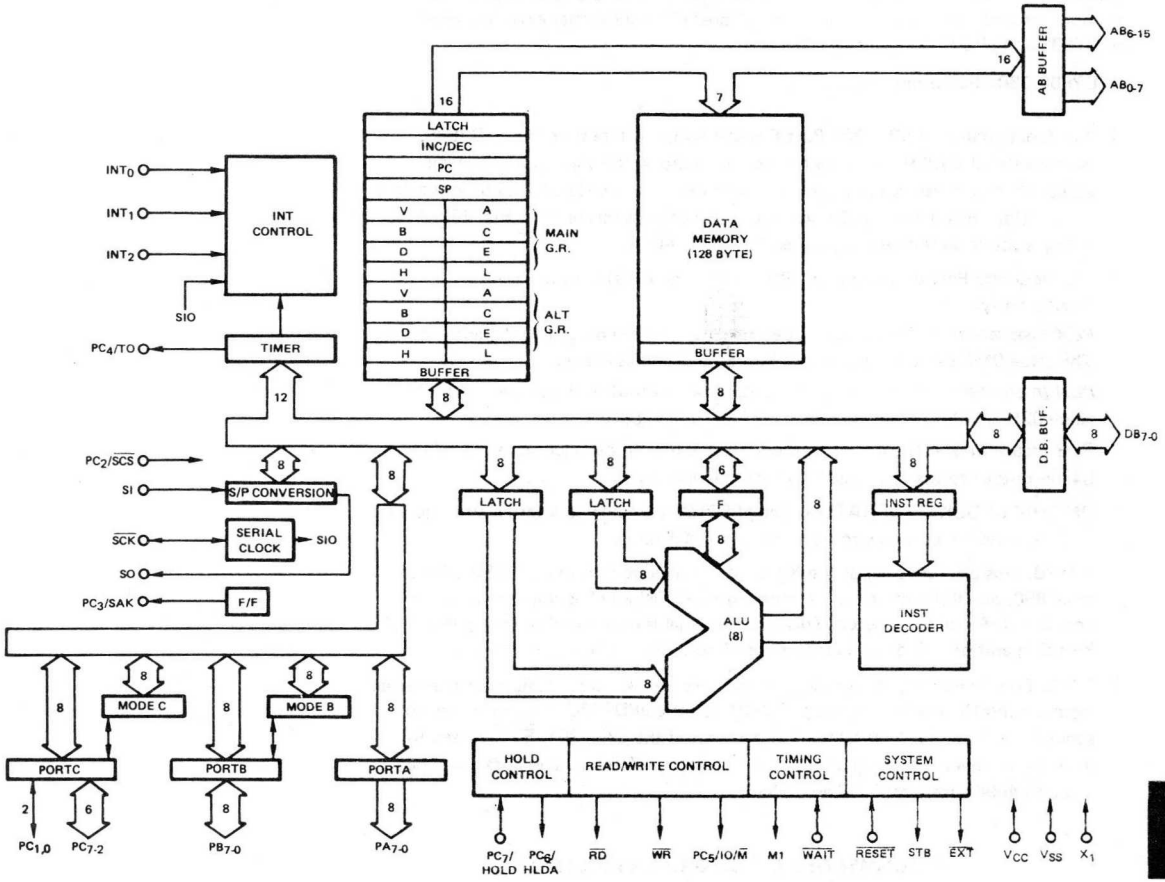
PIN CONFIGURATION



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PIN NO.	DESIGNATION	FUNCTION
1, 49-63	AB_0-AB_{15}	(Tri-State, Output) 16-bit address bus.
2	$\overline{EXT}$	(Output) $\overline{EXT}$ is used to simulate μPD7801/7802 external memory reference operation. $\overline{EXT}$ distinguishes between internal and external memory references, and goes low when locations 4096 through 65407 are accessed.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input.
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state TW and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices on the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of $\overline{SCK}$.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of $\overline{SCK}$, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7801.
30	STB	(Output) Used to simulate μPD7801 Port E operation, indicating that a Port E operation is being performed when active.
31	X_1	(Input) Clock Input
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

BLOCK DIAGRAM



μPD7800

Architecturally consistent with μPD7801/7802 devices, the μPD7800 uses a slightly different pin-out to accommodate for the address bus and lack of on-chip clock generator. For complete μPD7800 functional operation, please refer to μPD7801 product information. Listed below are functional differences that exist between μPD7800 and μPD7801 devices.

μPD7800/7801 Functional Differences

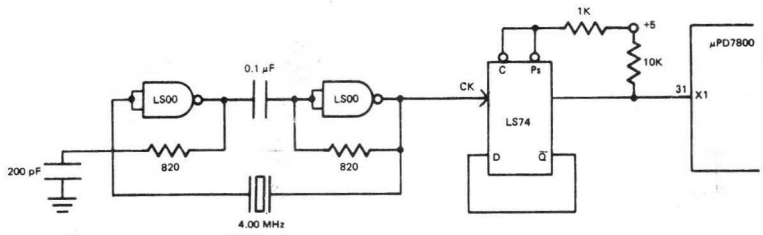
1. The functionality of μPD7801 Port E is somewhat different on the μPD7800. Because the μPD7800 contains no program memory, the address bus is made accessible to address external program memory. Thus, lines normally used for Port E operation with the μPD7801 are used as the address bus on the μPD7800. AB_0-AB_{15} is active during memory access 0 through 4095.
2. Consequently Port E instructions (PEX, PEN, and PER) have different functionality.

   PEX Instruction – The contents of B and C register are output to the address bus. The value 01H is output to the data bus. STB becomes active.

   PEN Instruction – B and C register contents are output to the address bus. The value 02H is output to the data bus. STB becomes active.

   PER Instruction – The address bus goes to the high impedance state. The value 04H is output to the data bus. STB becomes active.
3. ON-CHIP CLOCK GENERATOR. The μPD7800 contains no internal clock generator. An external clock source is input to the X_1 input.
4. PIN 30. This pin functions as the X_2 crystal connection on the μPD7801. On the μPD7800, pin 30 functions as a strobe output (STB) and becomes active when a Port E instruction is executed. This control signal is useful in simulating μPD7801 Port E operation – indicating that a port E operation is being performed.
5. PIN 2. Functions as the Φ out clock output used for synchronizing system external memory and I/O devices, on the μPD7801. On the μPD7800, this pin is used to simulate external memory reference operation of the μPD7801. $\overline{EXT}$ is used to distinguish between internal and external memory references and goes low when location 4096 through 65407 are accessed.

RECOMMENDED CLOCK DRIVE CIRCUIT



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Voltage On Any Pin . . . . . −0.3V to +7.0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10 ~ +70°C, V_{CC} = +5.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	200	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

T_a = −10 to +70°C, V_{CC} = +5.0V ± 10%

AC CHARACTERISTICS

CLOCK TIMING

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X_{OUT} Cycle Time	t_{CYX}	454	2000	ns	t_{CYX}
X_{OUT} Low Level Width	t_{XXL}	212		ns	t_{XXL}
X_{OUT} High Level Width	t_{XXH}	212		ns	t_{XXH}

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → X_{OUT} L.E.	t_{RX}	20		ns	
Address (PE_{0-15}) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	200(T3); 700(T4)		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address (PE_{0-15}) → WAIT L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from X_{OUT} L.E.)	t_{WTS}	180		ns	
$\overline{WAIT}$ Hold Time (Referenced from X_{OUT} L.E.)	t_{WTH}	0		ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	t_{CYX} = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
X_{OUT} L.E. → WR L.E.	t_{XW}		270	ns	
Address (PE_{0-15}) → X_{OUT} T.E.	t_{AX}		300	ns	
Address (PE_{0-15}) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address (PE_{0-15}) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

AC CHARACTERISTICS (CONT.)

SERIAL I/O OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		900	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	140		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

PEN, PEX, PER OPERATION

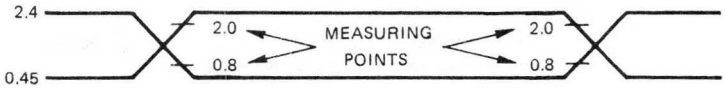
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
X_1 L.E. → $\overline{EXT}$	t_{XE}		250	ns	t_{CYX} = 500 ns
Address (AB_{0-15}) → STB L.E.	t_{AST}	200			
Data (DB_{0-7}) → STB L.E.	t_{DST}	200			
STB Hold Time	t_{STST}	300			
STB → Data	t_{STD}	400			

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from X_{OUT} L.E.)	t_{HDS_1}	100		ns	
	t_{HDS_2}	100		ns	
HOLD Hold Time (referenced from $\emptyset_{OUT}$ L.E.)	t_{HDH}	100		ns	
X_{OUT} L.E. → HLDA	t_{XHA}		100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)



② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

7

AC CHARACTERISTICS (CONT.)

t_{CYX} DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
t_{RX}	(1/25) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
t_{XW}	(27/50) T	MAX	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns
t_{AST}	(2/5) T	MIN	ns
t_{DST}	(2/5) T	MIN	ns
t_{STST}	(3/5) T	MIN	ns
t_{STD}	(4/5) T	MIN	ns

Notes: ① N = Number of Wait States

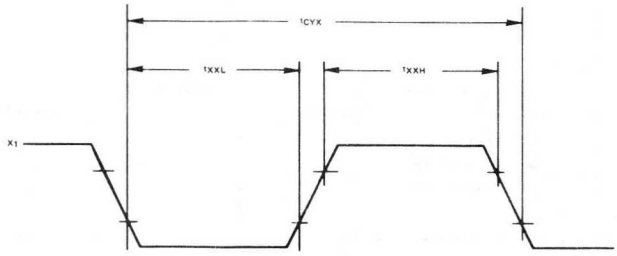
② T = t_{CYX}

③ Only above parameters are t_{CYX} dependent

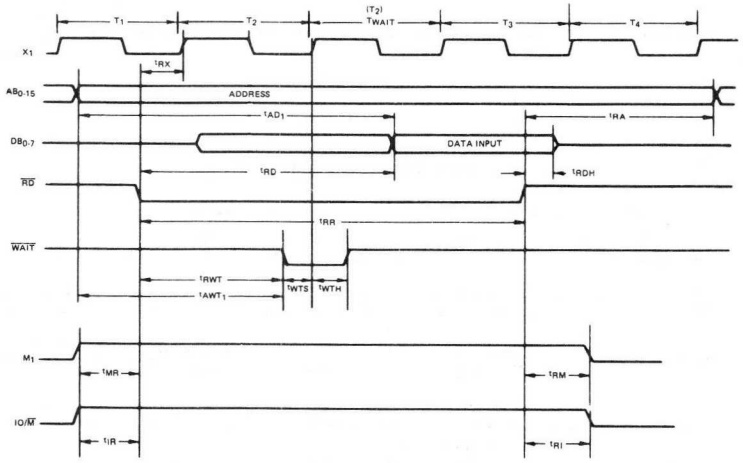
④ When a crystal frequency other than 4 MHz is used (t_{CYX} = 500 ns) the above equations can be used to calculate AC parameter values.

TIMING WAVEFORMS

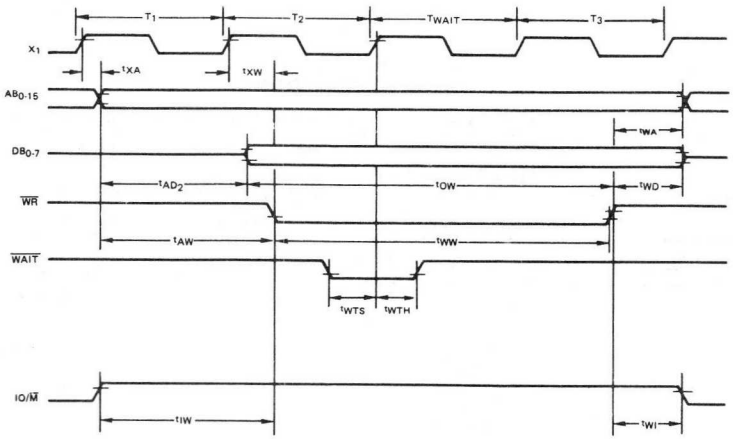
CLOCK TIMING



READ OPERATION



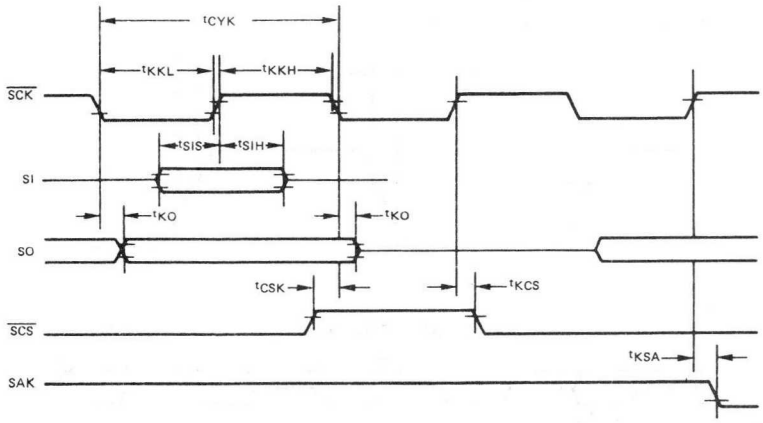
WRITE OPERATION



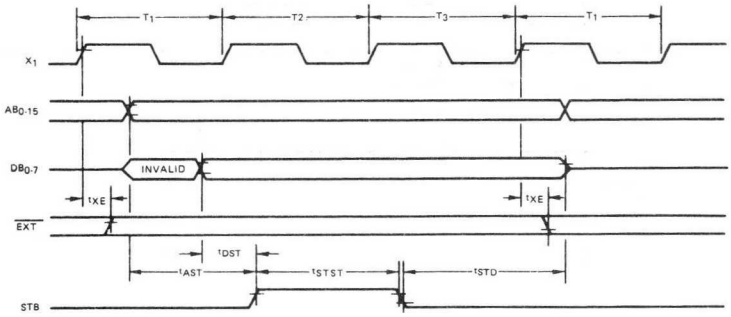
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TIMING WAVEFORMS (CONT.)

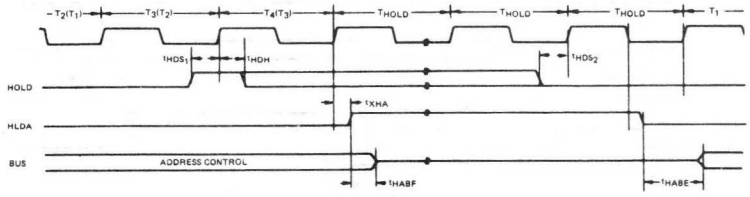
SERIAL I/O OPERATION



PEN, PEX, PER OPERATION

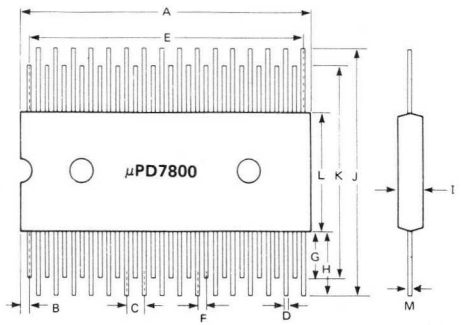


HOLD OPERATION



PACKAGE OUTLINE
μPD7800C

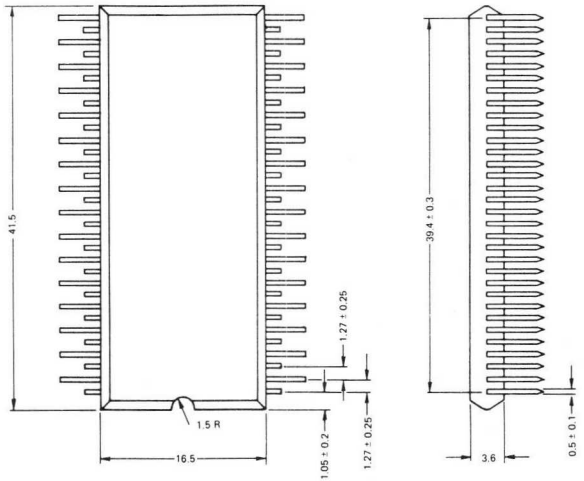
STRAIGHT LEADS



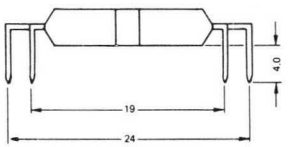
(Plastic)

ITEM	MILLIMETERS	INCHES
A	41.8 MAX.	1.65
B	1.22	0.05
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	39.37	1.55
F	1.27	0.05
G	6.75	0.27
H	9.3	0.37
I	3.6	0.14
J	35.1	1.38
K	30.0	1.18
L	16.5	0.65
M	0.25 ± 0.05	0.01 ± 0.002

BENT LEADS



(Unit:mm)



7800DS-12-80-CAT

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH 4K ROM

PRODUCT DESCRIPTION

The NEC μPD7801 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-Channel Silicon Gate MOS technology.

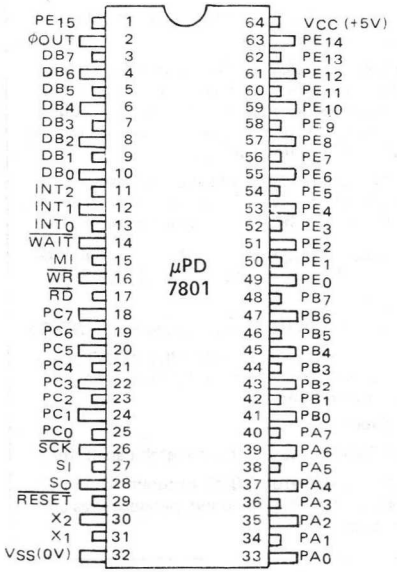
The NEC μPD7801 is intended to serve a broad spectrum of 8-bit designs ranging from enhanced single chip applications extending into the multi-chip microprocessor range. All the basic functional blocks – 4096 x 8 of ROM program memory, 128 x 8 of RAM data memory, 8-bit ALU, 48 I/O lines, Serial I/O port, 12-bit timer, and clock generator are provided on-chip to enhance stand-alone applications. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of the 8080A/8085A peripherals and memory products. Total memory space can be increased to 64K bytes.

The powerful 140 instruction set coupled with 4K bytes of ROM program memory and 128 bytes of RAM data memory greatly extends the range of single chip microcomputer applications. Five level vectored interrupt capability combined with a 2 microsecond cycle time enable the μPD7801 to compete with multi-chip microprocessor systems with the advantage that most of the support functions are on-chip.

FEATURES

- NMOS Silicon Gate Technology Requiring +5V Supply
- Complete Single-Chip Microcomputer with On-Chip ROM, RAM and I/O
  - 4K Bytes ROM
  - 128 Bytes RAM
  - 48 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 60K Bytes External Memory Address Range
- On-Chip Clock Generator
- Wait State Capability
- Alternate Z80™ Type Register Set
- Powerful 140 Instruction Set
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities

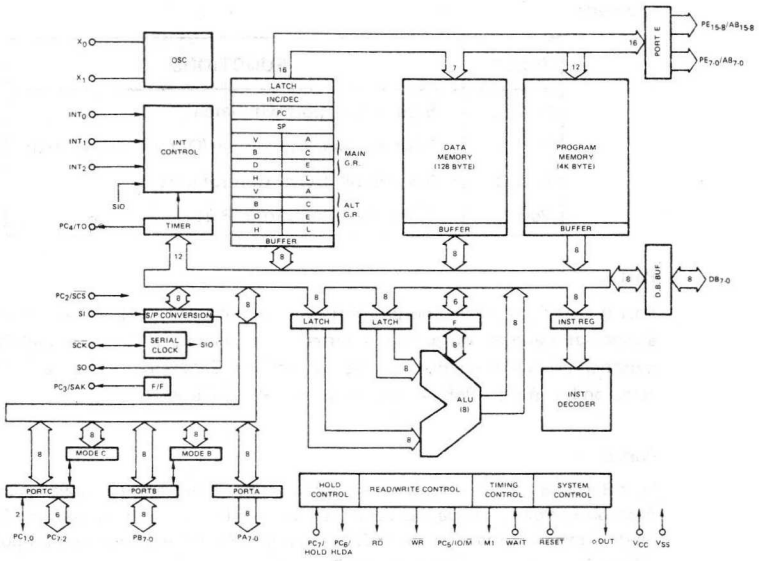
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
1, 49-63	AB_0-AB_{15}	(Tri-State, Output) 16-bit address bus.
2	$\overline{EXT}$	(Output) $\overline{EXT}$ is used to simulate μPD7801/7802 external memory reference operation. $\overline{EXT}$ distinguishes between internal and external memory references, and goes low when locations 4096 through 65407 are accessed.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input.
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state TW and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7801.
30	STB	(Output) Used to simulate μPD7801 Port E operation, indicating that a Port E operation is being performed when active.
31	X_1	(Input) Clock Input
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

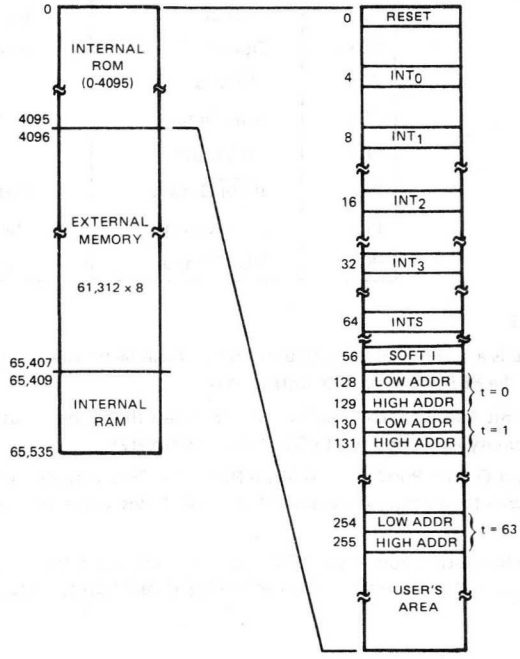
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Memory Map

The μPD7801 can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-4095) and RAM (65,408-65,535), any memory location can be used as either ROM or RAM. The following memory map defines the 0-64K byte memory space for the μPD7801 showing that the Reset Start Address, Interrupt Start Address, Call Tables, etc., are located in the internal ROM area.



I/O Ports

PORT	FUNCTIONS
Port A	8-bit output port with latch
Port B	8-bit programmable Input/Output port w/latch
Port C	8-bit nibble I/O or Control port
Port E	16-bit Address/Output Port

Port A

Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using Arithmetic and logic instructions. Data remains latched at Port A unless acted on by another Port A instruction or a RESET is issued.

Port B

Port B is an 8-bit I/O port. Data is latched at Port B in both the Input or Output modes. Each bit of Port B can be independently set to either Input or Output modes. The Mode B register programs the individual lines of Port B to be either an Input (Mode $B_{n=1}$) or an Output (Mode $B_{n=0}$).

Port C

Port C is an 8-bit I/O port. The Mode C register is used to program the upper 6 bits of Port C to provide control functions or to set the I/O structure per the following table.

	MODE $C_n = 0$	MODE $C_n = 1$
PC_0	Output	Input
PC_1	Output	Input
PC_2	$\overline{SCS}$ Input	Input
PC_3	SAK Output	Output
PC_4	To Output	Output
PC_5	IO/$\overline{M}$ Output	Output
PC_6	HLDA Output	Output
PC_7	HOLD Input	Input

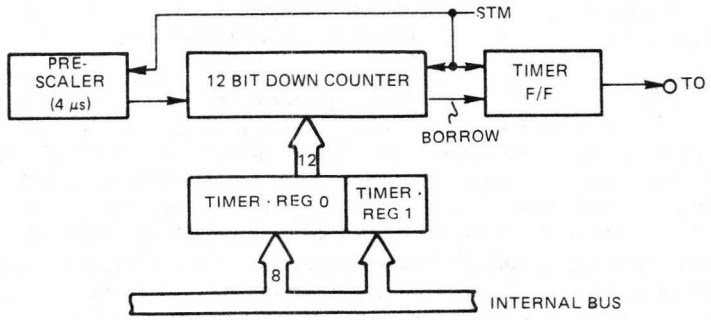
Port E

Port E is a 16-bit address bus/output port. It can be set to one of three operating modes using the PER, PEN, or PEX instructions.

- 16-Bit Address Bus – the Per instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).
- 4-Bit Output Port/12 Bit Address Bus – the PEN instruction sets this mode which allows for memory expansion of up to 4K bytes, externally, plus the transfer of 4-bit nibbles.
- 16-Bit Output Port – the PEX instruction sets Port E to a 16-bit output port. The contents of B and C registers appear on PE_{8-15} and PE_{0-7}, respectively.

FUNCTIONAL DESCRIPTION (CONT.)

Timer Operation



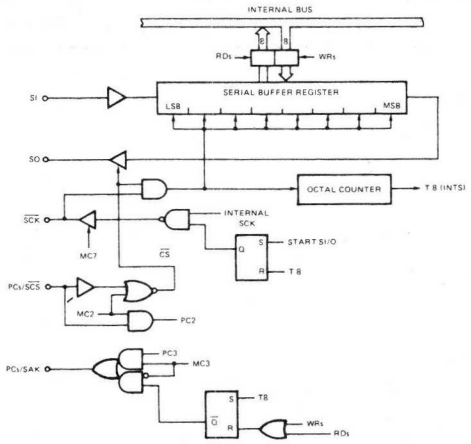
TIMER BLOCK DIAGRAM

A programmable 12-bit timer is provided on-chip for measuring time intervals, generating pulses, and general time-related control functions. It is capable of measuring time intervals from 4 μs to 16 μs in duration. The timer consists of a prescaler which decrements a 12-bit counter at a fixed 4 μs rate. Count pulses are loaded into the 12-bit down counter through timer register (TM0 and TM1). Count-down operation is initiated upon extension of the STM instruction when the contents of the down counter are fully decremented and a borrow operation occurs, an interval interrupt (INTT) is generated. At the same time, the contents of TM0 and TM1 are reloaded into the down-counter and countdown operation is resumed. Count operation may be restarted or initialized with the STM instruction. The duration of the timeout may be altered by loading new contents into the down counter.

The timer flip flop is set by the STM instruction and reset on a countdown operation. Its output (T0) is available externally and may be used in a single pulse mode or general external synchronization.

Timer interrupt (INTT) may be disabled through the interrupt.

Serial Port Operation



SERIAL PORT BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION (CONT.)

The on-chip serial port provides basic synchronous serial communication functions allowing the NEC μPD7801 to serially interface with external devices.

Serial Transfers are synchronized with either the internal clock or an external clock input ($\overline{SCK}$). The transfer rate is fixed at 1 Mbit/second if the internal clock is used or is variable between DC and 1 Mbit/second when an external clock is used. The Clock Source Select is determined by the Mode C register. The serial clock (internal or external $\overline{SCK}$) is enabled when the Serial Chip Select Signal ($\overline{SCS}$) goes low. At this time receive and transmit operations through the Serial Input port (SI)/Serial Output port (SO) are enabled. Receive and transmit operations are performed MSB first.

Serial Acknowledge (SAK) goes high when data transfers between the accumulator and Serial Register is completed. SAK goes low when the buffer becomes full after the completion of serial data receive or transmit operations. While SAK is low, no further data can be received.

Interrupt Structure

The μPD7801 provides a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from six different sources; three external interrupts, two internal interrupts, and non-maskable software interrupt. Each interrupt when activated branches to a designated memory vector location for that interrupt.

INT	VECTORED MEMORY LOCATION	PRIORITY	TYPE
INTT	8	3	Internal, Timer Overflow
INTS	64	6	Internal, Serial Buffer Full/Empty
INT0	4	2	Ext., level sensitive
INT1	16	4	Ext., Rising edge sensitive
INT2	32	5	Ext., Rising/Falling edge sensitive
SOFTI	96	1	Software Interrupt

FUNCTIONAL DESCRIPTION (CONT.)

$\overline{\text{RESET}}$ (Reset)

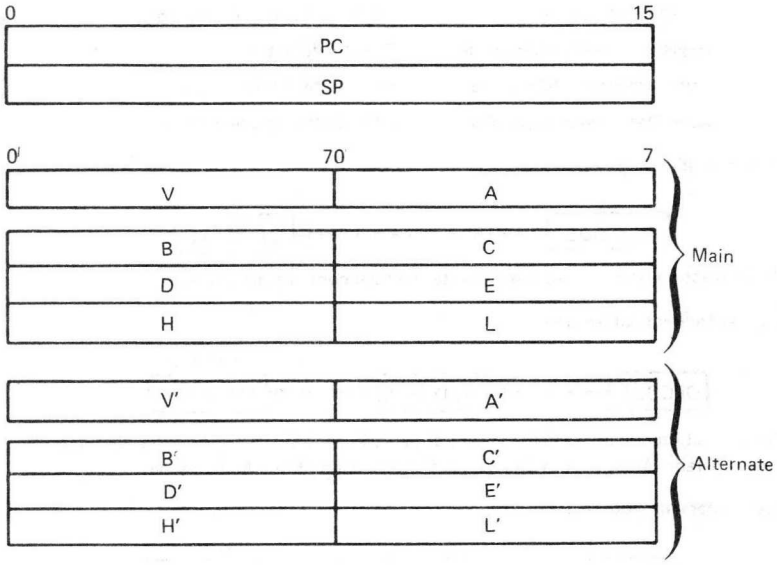
An active low-signal on this input for more than 4 μs forces the μPD7801 into a Reset condition. $\overline{\text{RESET}}$ affects the following internal functions:

- The Interrupt Enable Flags are reset, and Interrupts are inhibited.
- The Interrupt Request Flag is reset.
- The HALT flip flop is reset, and the Halt-state is released.
- The contents of the MODE B register are set to FF_H, and Port B becomes an input port.
- The contents of the MODE C register are set to FF_H. Port C becomes an I/O port and output lines go low.
- All Flags are reset to 0.
- The internal COUNT register for timer operation is set to FFF_H and the timer F/F is reset.
- The ACK F/F is set.
- The HLDA F/F is reset.
- The contents of the Program Counter are set to 0000_H.
- The Address Bus ($PE_{0\text{-}15}$), Data Bus ($DB_{0\text{-}7}$), $\overline{\text{RD}}$, and $\overline{\text{WR}}$ go to a high impedance state.

Once the $\overline{\text{RESET}}$ input goes high, the program is started at location 0000_H.

REGISTERS

The μPD7801 contains sixteen 8-bit registers and two 16-bit registers.



General Purpose Registers (B, C, D, E, H, L)

There are two sets of general purpose registers (Main: B, C, D, E, H, L: Alternate: B', C', D', H', L'). They can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL, B'C', D'E', H'L'). Auto Increment and Decrement addressing mode capabilities extend the uses for the DE, HL, D'E', and H'L' register-pairs. The contents of the BC, DE, and HL register-pairs can be exchanged with their Alternate Register counterparts using the EXX instruction.

FUNCTIONAL DESCRIPTION (CONT.)

Vector Register (V)

When defining a scratch pad area in the memory space, the upper 8-bit memory address is defined in the V-register and the lower 8-bits is defined by the immediate data of an instruction. Also the scratch pad indicated by the V-register can be used as 256 x 8-bit working registers for storing software flags, parameters and counters.

Accumulator (A)

All data transfers between the μPD7801 and external memory or I/O are done through the accumulator. The contents of the Accumulator and Vector Registers can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A reset sets the PC to 0000_H.

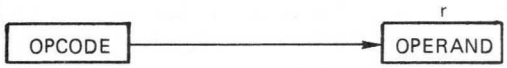
Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

ADDRESS MODES

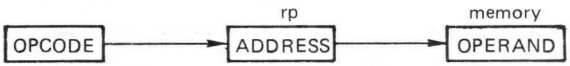
Register Addressing	Working Register Addressing
Register Indirect Addressing	Direct Addressing
Auto-Increment Addressing	Immediate Addressing
Auto-Decrement Addressing	Immediate Extended Addressing

Register Addressing



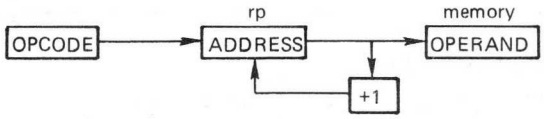
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

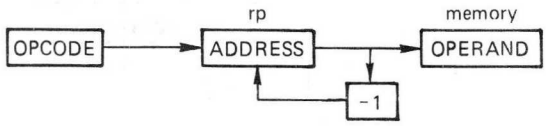
Auto-Increment Addressing



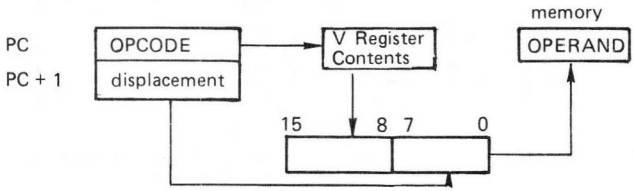
The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

ADDRESS MODES (CONT.)

Auto-Decrement Addressing

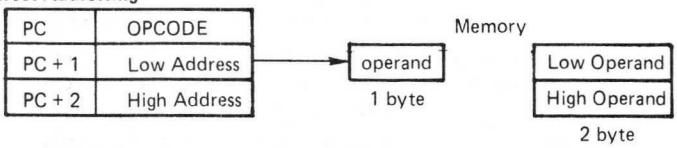


Working Register Addressing



The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix ending this address mode.

Direct Addressing



The two bytes following the opcode specify an address of a location containing the operand.

Immediate Addressing



Immediate Extended Addressing



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Operand Description

OPERAND	DESCRIPTION
r	V, A, B, C, D, E, H, L
r1	B, C, D, E, H, L
r2	A, B, C
sr	PA PB PC MK MB MC TM0 TM1 S
sr1	PA PB PC MK S
sr2	PA PB PC MK
rp	SP, B, D, H
rp1	V, B, D, H
rpa	B, D, H, D+, H+, D−, H−
rpa1	B, D, H
wa	8 bit immediate data
word	16 bit immediate data
byte	8 bit immediate data
bit	3 bit immediate data
f	F0, F1, F2, FT, FS,

Notes:
1. When special register operands sr, sr1, sr2 are used; PA=Port A, PB=Port B, PC=Port C, MK=Mask Register, MB=Mode B Register, MC=Mode C Register, TM0=Timer Register 0, TM1=Timer Register 1, S=Serial Register.
2. When register pair operands rp, rp1 are used; SP=Stack Pointer, B=BC, D=DE, H=HL, V=VA.
3. Operands rPa, rPa1, wa are used in indirect addressing and auto-increment/auto-decrement addressing modes.
   B=(BC), D=(DE), H=(HL)
   $D+=(DE)^+$, $H+=(HL)^+$, $D-=(DE)^-$, $H-=(HL)^-$.
4. When the interrupt operand f is used; F0=INTF0, F1=INTF1, F2=INTF2, FT=INTFT, FS=INTFS.

INSTRUCTION GROUPS

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
8-BIT DATA TRANSFER							
MOV	r1, A	1	4	r1 ← A			
MOV	A, r1	1	4	A ← r1			
MOV	sr, A	2	10	sr ← A			
MOV	A, sr1	2	10	A ← sr1			
MOV	r, word	4	17	r ← (word)			
MOV	word, r	4	17	(word) ← r			
MVI	r, byte	2	7	r ← byte			
MVIW	wa, byte	3	13	(V, wa) ← byte			
MVIX	rpa1, byte	2	10	(rpa1) ← byte			
STAW	wa	2	10	(V, wa) ← A			
LDAW	wa	2	10	A ← (V, wa)			
STAX	rpa	1	7	(rpa) ← A			
LDAX	rpa	1	7	A ← (rpa)			
EXX		1	4	Exchange register sets			
EX		1	4	V, A ↔ V, A			
BLOCK		1	13 (C+1)	$(DE)^+ \leftarrow (HL)^+$, C ← C − 1			
16-BIT DATA TRANSFER							
SBCD	word	4	20	(word) ← C, (word + 1) ← B			
SDED	word	4	20	(word) ← E, (word + 1) ← D			
SHLD	word	4	20	(word) ← L, (word + 1) ← H			
SSPD	word	4	20	(word) ← SP_L, (word + 1) ← SP_H			
LBCD	word	4	20	C ← (word), B ← (word + 1)			
LDED	word	4	20	E ← (word), D ← (word + 1)			
LHLD	word	4	20	L ← (word), H ← (word + 1)			
LSPD	word	4	20	SP_L ← (word), SP_H ← (word + 1)			
PUSH	rp1	2	17	(SP − 1) ← $rp1_H$, (SP − 2) ← $rp1_L$			
POP	rp1	2	15	$rp1_L$ ← (SP) $rp1_H$ ← (SP + 1), SP ← SP + 2			
LXI	rp, word	3	10	rp ← word			
TABLE		1	19	C ← (PC + 2 + A) B ← (PC + 2 + A + 1)			

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
ARITHMETIC							
ADD	A, r	2	8	A ← A + r		↕	↕
ADD	r, A	2	8	r ← r + A		↕	↕
ADDX	rpa	2	11	A ← A + (rpa)		↕	↕
ADC	A, r	2	8	A ← A + r + CY		↕	↕
ADC	r, A	2	8	r ← r + A + CY		↕	↕
ADCX	rpa	2	11	A ← A + (rpa) + CY		↕	↕
SUB	A, r	2	8	A ← A − r		↕	↕
SUB	r, A	2	8	r ← r − A		↕	↕
SUBX	rpa	2	11	A ← A − (rpa)		↕	↕
SBB	A, r	2	8	A ← A − r − CY		↕	↕
SBB	r, A	2	8	r ← r − A − CY		↕	↕
SBBX	rpa	2	11	A ← A − (rpa) − CY		↕	↕
ADDNC	A, r	2	8	A ← A + r	No Carry	↕	↕
ADDNC	r, A	2	8	r ← r + A	No Carry	↕	↕
ADDNCX	rpa	2	11	A ← A + (rpa)	No Carry	↕	↕
SUBNB	A, r	2	8	A ← A − r	No Borrow	↕	↕
SUBNB	r, A	2	8	r ← r − A	No Borrow	↕	↕
SUBNBX	rpa	2	11	A ← A − (rpa)	No Borrow	↕	↕
LOGICAL							
ANA	A, r	2	8	A ← A ∧ r			↕
ANA	r, A	2	8	r ← r ∧ A			↕
ANAX	rpa	2	11	A ← A ∧ (rpa)			↕
ORA	A, r	2	8	A ← A ∨ r			↕
ORA	r, A	2	8	r ← r ∨ A			↕
ORAX	rpa	2	11	A ← A ∨ (rpa)			↕
XRA	A, r	2	8	A ← A ∨̄ r			↕
XRA	r, A	2	8	A ← r ∨̄ A			↕
XRAX	rpa	2	11	A ← A ∨̄ (rpa)			↕
GTA	A, r	2	8	A − r − 1	No Borrow	↕	↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
LOGICAL (CONT.)							
GTAX	rpa	2	11	A – (rpa) – 1	No Borrow	↕	↕
LTA	A, r	2	8	A – r	Borrow	↕	↕
LTA	r, A	2	8	r – A	Borrow	↕	↕
LTAX	rpa	2	11	A – (rpa)	Borrow	↕	↕
ONA	A, r	2	8	A ∧ r	No Zero		↕
ONAX	rpa	2	11	A ∧ (rpa)	No Zero		↕
OFFA	A, r	2	8	A ∧ r	Zero		↕
OFFAX	rpa	2	11	A ∧ (rpa)	Zero		↕
NEA	A, r	2	8	A – r	No Zero	↕	↕
NEA	r, A	2	8	r – A	No Zero	↕	↕
NEAX	rpa	2	11	A – (rpa)	No Zero	↕	↕
EQA	A, r	2	8	A – r	Zero	↕	↕
EQA	r, A	2	8	r – A	Zero	↕	↕
EQAX	rpa	2	11	A – (rpa)	Zero	↕	↕
IMMEDIATE DATA TRANSFER (ACCUMULATOR)							
XRI	A, byte	2	7	A ← A ∨ byte			↕
ADINC	A, byte	2	7	A ← A + byte	No Carry	↕	↕
SUINB	A, byte	2	7	A ← A – byte	No Borrow	↕	↕
ADI	A, byte	2	7	A ← A + byte		↕	↕
ACI	A, byte	2	7	A ← A + byte + CY		↕	↕
SUI	A, byte	2	7	A ← A – byte		↕	↕
SBI	A, byte	2	7	A ← A – byte – CY		↕	↕
ANI	A, byte	2	7	A ← A ∧ byte			↕
ORI	A, byte	2	7	A ← A ∨ byte			↕
GTI	A, byte	2	7	A – byte – 1	No Borrow	↕	↕
LTI	A, byte	2	7	A – byte	Borrow	↕	↕
ONI	A, byte	2	7	A ∧ byte	No Zero		↕
OFFI	A, byte	2	7	A ∧ byte	Zero		↕
NEI	A, byte	2	7	A – byte	No Zero	↕	↕
EQI	A, byte	2	7	A – byte	Zero	↕	↕

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INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER							
XRI	r, byte	3	11	r ← r ∀ byte			↕
ADINC	r, byte	3	11	r ← r + byte	No Carry	↕	↕
SUINB	r, byte	3	11	r ← r – byte	No Borrow	↕	↕
ADI	r, byte	3	11	r ← r + byte		↕	↕
ACI	r, byte	3	11	r ← r + byte + CY		↕	↕
SUI	r, byte	3	11	r ← r – byte		↕	↕
SBI	r, byte	3	11	r ← r – byte – CY		↕	↕
ANI	r, byte	3	11	r ← r ∧ byte		↕	↕
ORJ	r, byte	3	11	r ← r ∨ byte			↕
GTI	r, byte	3	11	r – byte – 1	No Borrow	↕	↕
LTI	r, byte	3	11	r – byte	Borrow	↕	↕
ONI	r, byte	3	11	r ∧ byte	No Zero		↕
OFFI	r, byte	3	11	r ∧ byte	Zero		↕
NEI	r, byte	3	11	r – byte	No Zero	↕	↕
EQI	r, byte	3	11	r – byte	Zero	↕	↕
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER)							
XRI	sr2, byte	3	17	sr2 ← sr2 ∀ byte			↕
ADINC	sr2, byte	3	17	sr2 ← sr2 + byte	No Carry	↕	↕
SUINB	sr2, byte	3	17	sr2 ← sr2 – byte	No Borrow	↕	↕
ADI	sr2, byte	3	17	sr2 ← sr2 + byte		↕	↕
ACI	sr2, byte	3	17	sr2 ← sr2 + byte + CY		↕	↕
SUI	sr2, byte	3	17	sr2 ← sr2 – byte		↕	↕
SBI	sr2, byte	3	17	sr2 ← sr2 – byte – CY		↕	↕
ANI	sr2, byte	3	17	sr2 ← sr2 ∧ byte			↕
ORI	sr2, byte	3	17	sr2 ← sr2 ∨ byte			↕
GTI	sr2, byte	3	14	sr2 – byte – 1	No Borrow	↕	↕
LTI	sr2, byte	3	14	sr2 – byte	Borrow	↕	↕
ONI	sr2, byte	3	14	sr2 ∧ byte	No Zero		↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER) (CONT.)							
OFFI	sr2, byte	3	14	sr2 ∧ byte	Zero		↕
NEI	sr2, byte	3	14	sr2 – byte	No Zero	↕	↕
EQI	sr2, byte	3	14	sr2 – byte	Zero	↕	↕
WORKING REGISTER							
XRAW	wa	3	14	A ← A ∀ (V, wa)			↕
ADDNCW	wa	3	14	A ← A + (V, wa)	No Carry	↕	↕
SUBNBW	wa	3	14	A ← A – (V, wa)	No Borrow	↕	↕
ADDW	wa	3	14	A ← A + (V, wa)		↕	↕
ADCW	wa	3	14	A ← A + (V, wa) + CY		↕	↕
SUBW	wa	3	14	A ← A – (V, wa)		↕	↕
SBBW	wa	3	14	A ← A – (V, wa) – CW		↕	↕
ANAW	wa	3	14	A ← A ∧ (V, wa)			↕
ORAW	wa	3	14	A ← A ∨ (V, wa)			↕
GTAW	wa	3	14	A ← (V, wa) – 1	No Borrow	↕	↕
LTAW	wa	3	14	A – (V, wa)	Borrow	↕	↕
ONAW	wa	3	14	A ∧ (V, wa)	No Zero		↕
OFFAW	wa	3	14	A ∧ (V, wa)	Zero		↕
NEAW	wa	3	14	A – (V, wa)	No Zero	↕	↕
EQAW	wa	3	14	A – (V, wa)	Zero	↕	↕
ANIW	wa, byte	3	16	(V, wa) ← (V, wa) ∧ byte			↕
ORIW	wa, byte	3	16	(V, wa) ← (V, wa) ∨ byte			↕
GTIW	wa, byte	3	13	(V, wa) – byte – 1	No Borrow	↕	↕
LTIW	wa, byte	3	13	(V, wa) – byte	Borrow	↕	↕
ONIW	wa, byte	3	13	(V, wa) ∧ byte	No Zero		↕
OFFIW	wa, byte	3	13	(V, wa) ∧ byte	Zero		↕
NEIW	wa, byte	3	13	(V, wa) – byte	No Zero	↕	↕
EQIW	wa, byte	3	13	(V, wa) – byte	Zero	↕	↕
INCREMENT/DECREMENT							
INR	r2	1	4	r2 ← r2 + 1	Carry		↕
INRW	wa	2	13	(V, wa) ← (V, wa) + 1	Carry		↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
INCREMENT/DECREMENT (CONT.)							
DCR	r2	1	4	r2 ← r2 − 1	Borrow		↕
DCRW	wa	2	13	(V, wa) ← (V, wa) − 1	Borrow		↕
INX	rp	1	7	rp ← rp + 1			
DCX	rp	1	7	rp ← rp − 1			
DAA		1	4	Decimal Adjust Accumulator		↕	↕
STC		2	8	CY ← 1		1	
CLC		2	8	CY ← 0		0	
ROTATE AND SHIFT							
RLD		2	17	Rotate Left Digit			
RRD		2	17	Rotate Right Digit			
RAL		2	8	Am + 1 ← Am, A_0 ← CY, CY ← A_7		↕	
RCL		2	8	Cm + 1 ← Cm, C_0 ← CY, CY ← C_7		↕	
RAR		2	8	Am − 1 ← Am, A_7 ← CY, CY ← A_0		↕	
RCR		2	8	Cm − 1 ← Cm, C_7 ← CY, CY ← C_0		↕	
SHAL		2	8	Am + 1 ← Am, A_0 ← 0, CY ← A_7		↕	
SHCL		2	8	Cm + 1 ← CM, C_0 ← 0, CY ← C_7		↕	
SHAR		2	8	Am − 1 ← Am, A_7 ← 0, CY ← A_0		↕	
SHCR		2	8	Cm − 1 ← Cm, C_7 ← 0, CY ← C_0		↕	
JUMP							
JMP	word	3	10	PC ← word			
JB		1	4	PC_H ← B, PC_L ← C			
JR	word	1	13	PC ← PC + 1 + jdisp1			
JRE	word	2	13	PC ← PC + 2 + jdisp			
CALL							
CALL	word	3	16	(SP − 1) ← $(PC - 3)_H$, (SP − 2) ← $(PC - 3)_L$, PC ← word			
CALB		1	13	(SP − 1) ← $(PC - 1)_H$, (SP − 2) ← $(PC - 1)_L$, PC_H ← B, PC_L ← C			
CALF	word	2	16	$(SP-1)\leftarrow(PC-2)_H$, $(SP-2)\leftarrow(PC-2)_L$ PC15 ~ 11 ← 00001, PC10 ~ 0 ← fa			
CALT	word	1	19	$(SP-1)\leftarrow(PC-1)_H$, $(SP-2)\leftarrow(PC-1)_L$ $PC_L\leftarrow(128-2ta)$, $PC_H\leftarrow(129+2ta)$			
SOFTI		1	19	(SP − 1) ← PSW, SP − 2, (SP − 3) ← PC PC ← 0060_H, SIRQ ← 1			

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
RETURN							
RET		1	11	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1)$ $SP \leftarrow SP-2$			
RETS		1	11+a	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1)$, $SP \leftarrow SP+2, PC \leftarrow PC+n$			
RETI		1	15	$PC_L \leftarrow (SP), PC_H \leftarrow (SP+1)$ $PSW \leftarrow (SP+2), SP \leftarrow SP+3, SIRQ \leftarrow 0$			
SKIP							
BIT	bit, wa	2	10	Bit test	$(V, wa)_{bit} = 1$		
SKC		2	8	Skip if Carry	CY = 1		
SKNC		2	8	Skip if No Carry	CY = 0		
SKZ		2	8	Skip if Zero	Z = 1		
SKNZ		2	8	Skip if No Zero	Z = 0		
SKIT	f	2	8	Skip if INT X = 1, then reset INT X	f = 1		
SKNIT	f	2	8	Skip if No INT X otherwise reset INT X	f = 0		
CPU CONTROL							
NOP		1	4	No Operation			
EI		2	8	Enable Interrupt			
DI		2	8	Disable Interrupt			
HLT		1	6	Halt			
SERIAL PORT CONTROL							
SIO		1	4	Start (Trigger) Serial I/O			
STM		1	4	Start Timer			
INPUT/OUTPUT							
IN	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow$ byte $A \leftarrow DB_{7-0}$			
OUT	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow$ byte $DB_{7-0} \leftarrow A$			
PEX		2	11	$PE_{15-8} \leftarrow B, PE_{7-0} \leftarrow C$			
PEN		2	11	$PE_{15-12} \leftarrow B_{7-4}$			
PER		2	11	Port E AB Mode			

Program Status Word (PSW) Operation

OPERATION						D6	D5	D4	D3	D2	D0
REG, MEMORY			IMMEDIATE		SKIP	Z	SK	HC	L1	L0	CY
ADD ADC SUB SBB	ADDW ADCW SUBW SBBW	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			↕	0	↕	0	0	↕
ANA ORA XRA	ANAW ORAW XRAW	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		↕	0	•	0	0	•
ADDNC SUBNB GTA LTA	ADDNCW SUBNBW GTAW LTAW	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	 GTIW LTIW		↕	↕	↕	0	0	↕
ONA OFFA	ONAW OFFAW	ONAX OFFAX	ONI OFFI	ONIW OFFIW		↕	↕	•	0	0	•
NEA EQA	NEAW EQAW	NEAX EQAX	NEI EQI	NEIW EQIW		↕	↕	↕	0	0	↕
INR DCR	INRW DCRW					↕	↕	↕	0	0	•
DAA						↕	0	↕	0	0	↕
RAL, RAR, RCL, RCR SHAL, SHAR, SHCL, SHCR						•	0	•	0	0	↕
RLD, RRD						•	0	•	0	0	•
STC						•	0	•	0	0	1
CLC						•	0	•	0	0	0
			MVI A, byte			•	0	•	1	0	•
			MVI L, byte LXI H, word			•	0	•	0	1	•
					BIT SKC SKNC SKZ SKNZ SKIT SKNIT	•	↕	•	0	0	•
					RETS	•	1	•	0	0	•
All other instructions						•	0	•	0	0	•

↕ Flag affected according to result of operation
1 Flag set
0 Flag reset
• Flag not affected

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Voltage On Any Pin . . . . . −0.3V to +7.0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

−10 to +70°C, V_{CC} = +5.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	200	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

AC CHARACTERISTICS

-10 to $+70°C$, $V_{CC} = +5.0V \pm 10\%$

CLOCK TIMING

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X1 Input Cycle Time	t_{CYX}	227	1000	ns	
X1 Input Low Level Width	t_{XXL}	106		ns	
X1 Input High Level Width	t_{XXH}	106		ns	
ϕ_{OUT} Cycle Time	$t_{CY\phi}$	454	2000	ns	
ϕ_{OUT} Low Level Width	$t_{\phi\phi L}$	150		ns	
ϕ_{OUT} High Level Width	$t_{\phi\phi H}$	150		ns	
ϕ_{OUT} Rise/Fall Time	t_r, t_f		40	ns	

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → ϕ_{OUT} L.E.	$t_{R\phi}$	100		ns	
Address (PE_{0-15}) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	$200_{(T3)}$; $700_{(T4)}$		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address (PE_{0-15}) → WAIT L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from ϕ_{OUT} L.E.)	t_{WTS}	290		ns	
$\overline{WAIT}$ Hold Time (Referenced from ϕ_{OUT} L.E.)	t_{WTH}	0		ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	$t_{CY\phi}$ = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
ϕ_{OUT} L.E. → $\overline{WR}$ L.E.	$t_{\phi W}$	40	125	ns	
Address (PE_{0-15}) → ϕ_{OUT} T.E.	$t_{A\phi}$	100	300	ns	
Address (PE_{0-15}) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address (PE_{0-15}) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

SERIAL I/O OPERATION

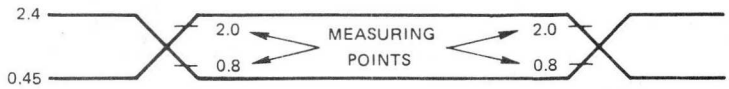
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		900	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	140		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from ϕ_{OUT} L.E.)	t_{HDS_1}	200		ns	$t_{CY\phi}$ = 500 ns
	t_{HDS_2}	200		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	0		ns	
ϕ_{OUT} L.E. → HLDA	t_{DHA}	110	100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)



② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

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AC CHARACTERISTICS (CONT.)

$t_{CY\phi}$ DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
$t_{R\phi}$	(1/5) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
$t_{\phi W}$	(1/4) T	MAX	ns
$t_{A\phi}$	(1/5) T	MIN	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns

Notes: ① N = Number of Wait States

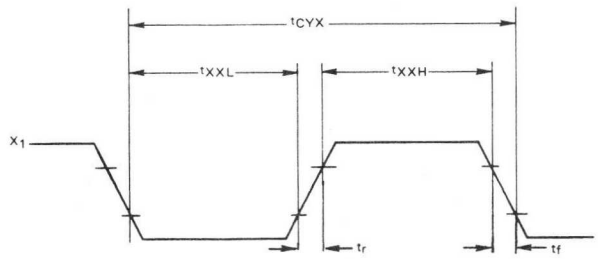
② $T = t_{CY\phi}$

③ Only above parameters are t_{CY_ϕ} dependent

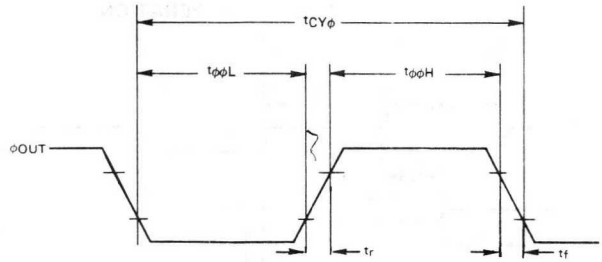
④ When a crystal frequency other than 4 MHz is used (t_{CY_ϕ} = 500 ns) the above equations can be used to calculate AC parameter values.

TIMING WAVEFORMS

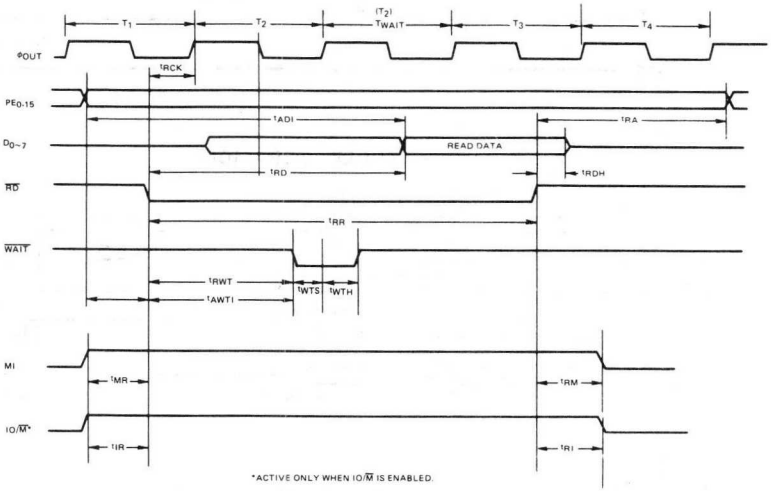
CLOCK TIMING



TIMING WAVEFORMS
(CONT.)

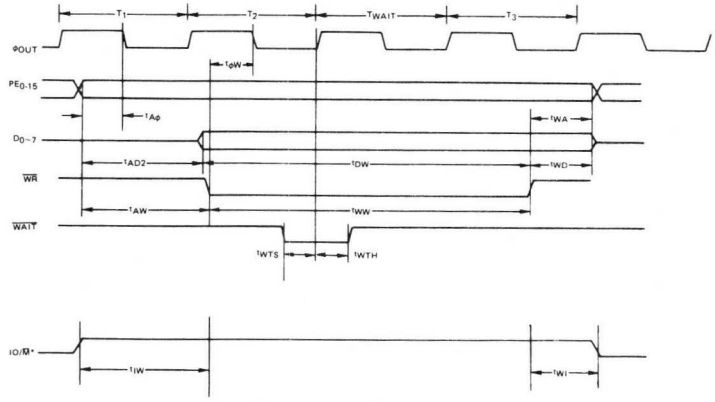


READ OPERATION



*ACTIVE ONLY WHEN IO/$\overline{M}$ IS ENABLED.

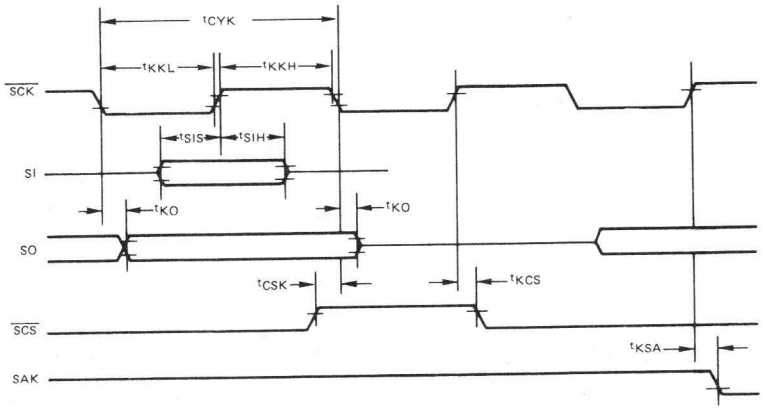
WRITE OPERATION



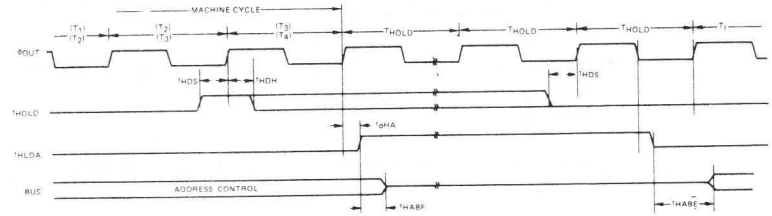
*ACTIVE ONLY WHEN IO/$\overline{M}$ IS ENABLED.

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SERIAL I/O OPERATION

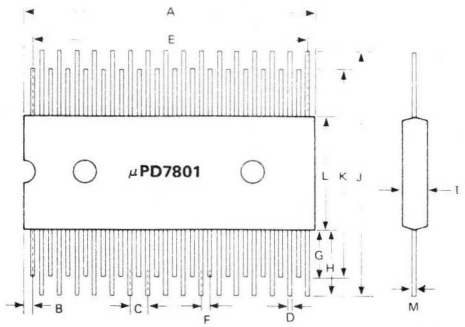


HOLD OPERATION



PACKAGE INFORMATION

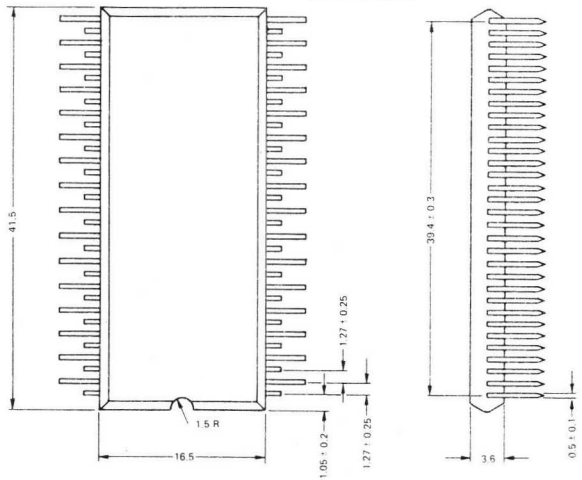
STRAIGHT LEADS



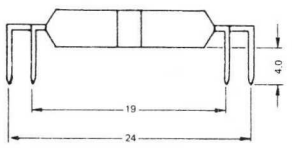
(Plastic)

ITEM	MILLIMETERS	INCHES
A	41.8 MAX	1.65
B	1.22	0.05
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	39.37	1.55
F	1.27	0.05
G	6.75	0.27
H	9.3	0.37
I	3.6	0.14
J	35.1	1.38
K	30.0	1.18
L	16.5	0.65
M	0.25 ± 0.05	0.01 ± 0.002

BENT LEADS



(Unit: mm)



7801DS-12-80-CAT

NOTES

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH 6K ROM

PRODUCT DESCRIPTION

The NEC μPD7802 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-Channel Silicon Gate MOS technology.

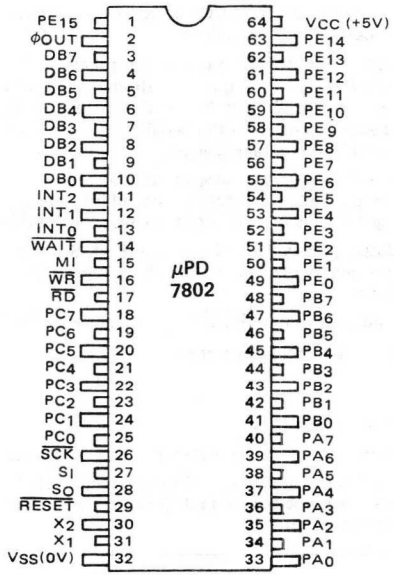
The NEC μPD7802 is intended to serve a broad spectrum of 8-bit designs ranging from enhanced single chip applications extending into the multi-chip microprocessor range. All the basic functional blocks – 6144 x 8 of ROM program memory, 64 x 8 of RAM data memory, 8-bit ALU, 48 I/O lines, Serial I/O port, 12-bit timer, and clock generator are provided on-chip to enhance stand-alone applications. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of the 8080A/8085A peripherals and memory products. Total memory space can be increased to 64K bytes.

The powerful 140 instruction set coupled with 6K bytes of ROM program memory and 64 bytes of RAM data memory greatly extends the range of single chip microcomputer applications. Five level vectored interrupt capability combined with a 2 microsecond cycle time enable the μPD7802 to compete with multi-chip microprocessor systems with the advantage that most of the support functions are on-chip.

FEATURES

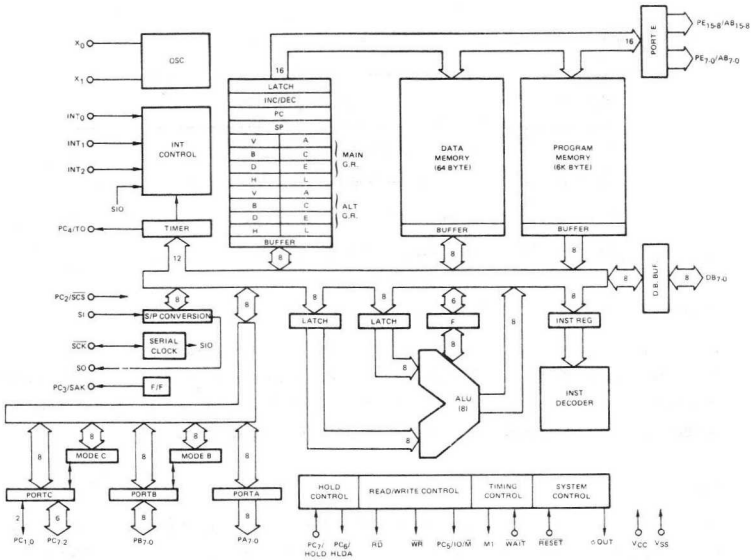
- NMOS Silicon Gate Technology Requiring +5V Supply
- Complete Single-Chip Microcomputer with On-Chip ROM, RAM and I/O
  - 6K Bytes ROM
  - 64 Bytes RAM
  - 48 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 58K Bytes External Memory Address Range
- On-Chip Clock Generator
- Wait State Capability
- Alternate Z80™ Type Register Set
- Powerful 140 Instruction Set
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities

PIN CONFIGURATION



PIN NO.	DESIGNATION	FUNCTION
1, 49-63	AB_0-AB_{15}	(Tri-State, Output) 16-bit address bus.
2	ϕOUT	(Output) ϕOUT provides a prescaled output clock for use with external I/O devices or memories. ϕOUT frequency is $f_{XTAL}/2$.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input.
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state T_W and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7801.
30	X_2	(Output) Oscillator output.
31	X_1	(Input) Clock Input
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

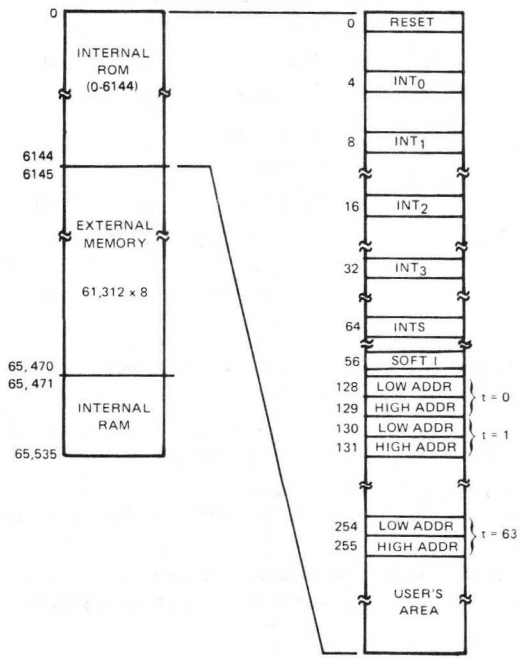
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Memory Map

The μPD7802 can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-6144) and RAM (65, 471-65, 535), any memory location can be used as either ROM or RAM. The following memory map defines the 0-64K byte memory space for the μPD7802 showing that the Reset Start Address, Interrupt Start Address, Call Tables, etc., are located in the Internal ROM area.



I/O PORTS

PORT	FUNCTIONS
Port A	8-bit output port with latch
Port B	8-bit programmable Input/Output port w/latch
Port C	8-bit nibble I/O or Control port
Port E	16-bit Address/Output Port

Port A

Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using Arithmetic and Logic instructions. Data remains latched at Port A unless acted on by another Port A instruction or a RESET is issued.

Port B

Port B is an 8-bit I/O port. Data is latched at Port B in both the Input or Output modes. Each bit of Port B can be independently set to either Input or Output modes. The Mode B register programs the individual lines of Port B to be either an Input (Mode $B_{n=1}$) or an Output (Mode $B_{n=0}$).

Port C

Port C is an 8-bit I/O port. The Mode C register is used to program the upper 6 bits of Port C to provide control functions or to set the I/O structure per the following table.

	MODE $C_n = 0$	MODE $C_n = 1$
PC_0	Output	Input
PC_1	Output	Input
PC_2	$\overline{SCS}$ Input	Input
PC_3	SAK Output	Output
PC_4	To Output	Output
PC_5	IO/$\overline{M}$ Output	Output
PC_6	HLDA Output	Output
PC_7	HOLD Input	Input

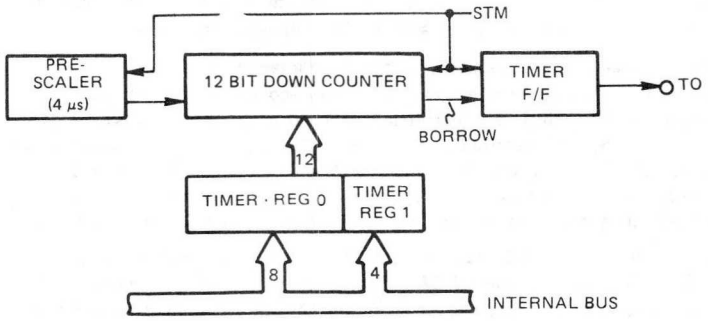
Port E

Port E is a 16-bit address bus/output port. It can be set to one of three operating modes using the PER, PEN, or PEX instructions.

- 16-Bit Address Bus – the PER instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).
- 4-Bit Output Port/12 Bit Address Bus – the PEN instruction sets this mode which allows for memory expansion of an additional 4K bytes, externally, plus the transfer of 4-bit nibbles.
- 16-Bit Output Port – the PEX instruction sets Port E to a 16-bit output port. The contents of B and C registers appear on PE_{8-15} and PE_{0-7}, respectively.

FUNCTIONAL DESCRIPTION (CONT.)

TIMER OPERATION



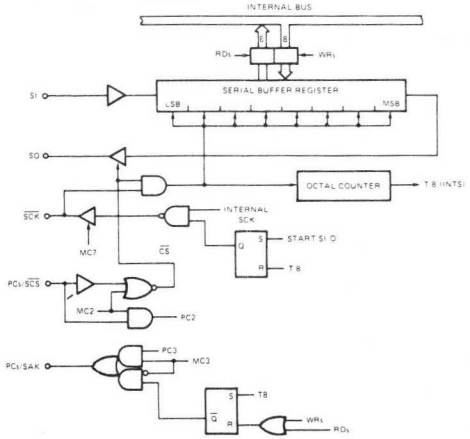
TIMER BLOCK DIAGRAM

A programmable 12-bit timer is provided on-chip for measuring time intervals, generating pulses, and general time-related control functions. It is capable of measuring time intervals from 4 μs to 16 ms in duration. The timer consists of a prescaler which decrements a 12-bit counter at a fixed 4 μs rate. Count pulses are loaded into the 12-bit down counter through timer register (TM0 and TM1). Count-down operation is initiated upon extension of the STM instruction when the contents of the down counter are fully decremented and a borrow operation occurs, an interval interrupt (INTT) is generated. At the same time, the contents of TM0 and TM1 are reloaded into the down-counter and countdown operation is resumed. Count operation may be restarted or initialized with the STM instruction. The duration of the timeout may be altered by loading new contents into the down counter.

The timer flip flop is set by the STM instruction and reset on a countdown operation. Its output (T0) is available externally and may be used in a single pulse mode or general external synchronization.

Timer interrupt (INTT) may be disabled through the interrupt.

SERIAL PORT OPERATION



SERIAL PORT BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION (CONT.)

The on-chip serial port provides basic synchronous serial communication functions allowing the NEC μPD7802 to serially interface with external devices.

Serial Transfers are synchronized with either the internal clock or an external clock input ($\overline{SCK}$). The transfer rate is fixed at 1 Mbit/second if the internal clock is used or is variable between DC and 1 Mbit/second when an external clock is used. The Clock Source Select is determined by the Mode C register. The serial clock (internal or external $\overline{SCK}$) is enabled when the Serial Chip Select Signal ($\overline{SCS}$) goes low. At this time receive and transmit operations through the Serial Input port (SI)/Serial Output port (SO) are enabled. Receive and transmit operations are performed MSB first.

Serial Acknowledge (SAK) goes high when data transfers between the accumulator and Serial Register is completed. SAK goes low when the buffer becomes full after the completion of serial data receive or transmit operations. While SAK is low, no further data can be received.

INTERRUPT STRUCTURE

The μPD7802 provides a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from six different sources; three external interrupts, two internal interrupts, and a non-maskable software interrupt. Each interrupt when activated branches to a designated memory vector location for that interrupt.

INT	VECTORED MEMORY LOCATION	PRIORITY	TYPE
INTT	8	3	Internal, Timer Overflow
INTS	64	6	Internal, Serial Buffer Full/Empty
INT0	4	2	Ext., level sensitive
INT1	16	4	Ext., Rising edge sensitive
INT2	32	5	Ext., Rising/Falling edge sensitive
SOFTI	96	1	Software Interrupt

FUNCTIONAL DESCRIPTION (CONT.)

$\overline{\text{RESET}}$ (Reset)

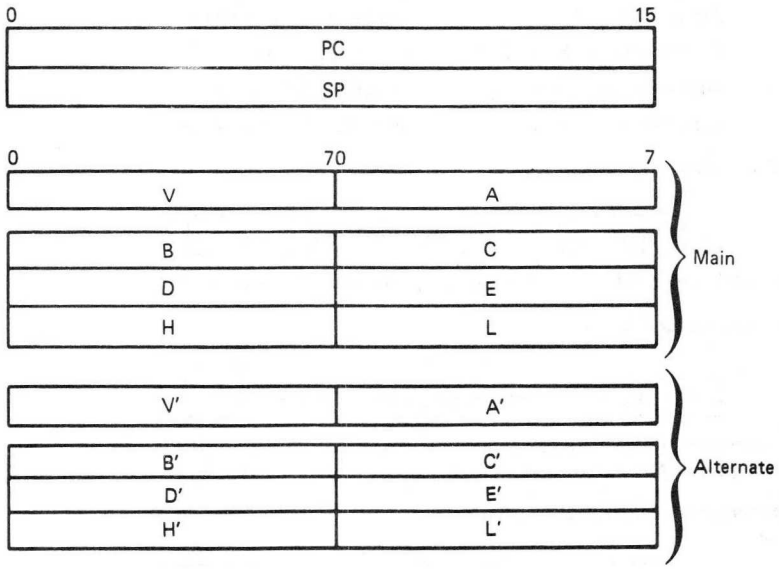
An active low-signal on this input for more than 4 μs forces the μPD7802 into a Reset condition. $\overline{\text{RESET}}$ affects the following internal functions:

- The Interrupt Enable Flags are reset, and Interrupts are inhibited.
- The Interrupt Request Flag is reset.
- The HALT flip flop is reset, and the Halt-state is released.
- The contents of the MODE B register are set to FF_H, and Port B becomes an input port.
- The contents of the MODE C register are set to FF_H. Port C becomes an I/O port and output lines go low.
- All Flags are reset to 0.
- The internal COUNT register for timer operation is set to FFF_H and the timer F/F is reset.
- The ACK F/F is set.
- The HLDA F/F is reset.
- The contents of the Program Counter are set to 0000_H.
- The Address Bus ($PE_{0\text{-}15}$), Data Bus ($DB_{0\text{-}7}$), $\overline{\text{RD}}$, and $\overline{\text{WR}}$ go to a high impedance state.

Once the $\overline{\text{RESET}}$ input goes high, the program is started at location 0000_H.

REGISTERS

The μPD7802 contains sixteen 8-bit registers and two 16-bit registers.



General Purpose Registers (B, C, D, E, H, L)

There are two sets of general purpose registers (Main: B, C, D, E, H, L: Alternate: B', C', D', H', L'). They can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL, B'C', D'E', H'L'). Auto Increment and Decrement addressing mode capabilities extend the uses for the DE, HL, D'E', and H'L' register-pairs. The contents of the BC, DE, and HL register-pairs can be exchanged with their Alternate Register counterparts using the EXX instruction.

FUNCTIONAL DESCRIPTION (CONT.)

Vector Register (V)

When defining a scratch pad area in the memory space, the upper 8-bit memory address is defined in the V-register and the lower 8-bits is defined by the immediate data of an instruction. Also the scratch pad indicated by the V-register can be used as 256 x 8-bit working registers for storing software flags, parameters and counters.

Accumulator (A)

All data transfers between the μPD7802 and external memory or I/O are done through the accumulator. The contents of the Accumulator and Vector Registers can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A reset sets the PC to 0000_H.

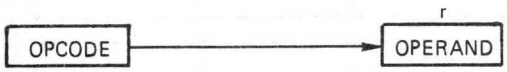
Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

ADDRESS MODES

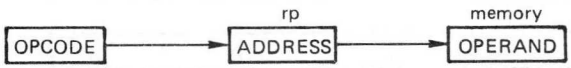
Register Addressing	Working Register Addressing
Register Indirect Addressing	Direct Addressing
Auto-Increment Addressing	Immediate Addressing
Auto-Decrement Addressing	Immediate Extended Addressing

Register Addressing



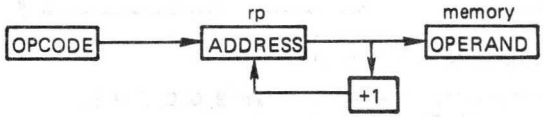
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

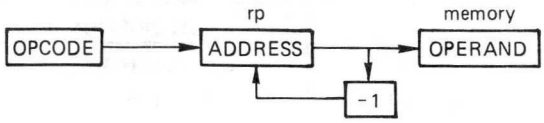
Auto-Increment Addressing



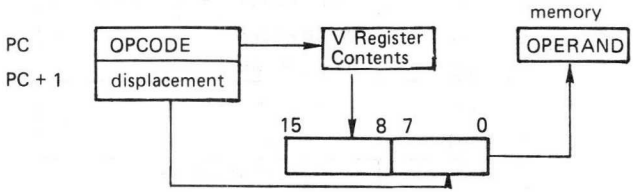
The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

ADDRESS MODES (CONT.)

Auto-Decrement Addressing

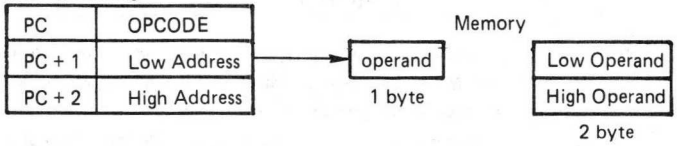


Working Register Addressing



The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix ending this address mode.

Direct Addressing



The two bytes following the opcode specify an address of a location containing the operand.

Immediate Addressing



Immediate Extended Addressing



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Operand Description

OPERAND	DESCRIPTION
r	V, A, B, C, D, E, H, L
r1	B, C, D, E, H, L
r2	A, B, C
sr	PA PB PC MK MB MC TM0 TM1 S
sr1	PA PB PC MK S
sr2	PA PB PC MK
rp	SP, B, D, H
rp1	V, B, D, H
rpa	B, D, H, D+, H+, D-, H-
rpa1	B, D, H
wa	8 bit immediate data
word	16 bit immediate data
byte	8 bit immediate data
bit	3 bit immediate data
f	F0, F1, F2, FT, FS,

Notes:
1. When special register operands sr, sr1, sr2 are used; PA=Port A, PB=Port B, PC=Port C, MK=Mask Register, MB=Mode B Register, MC=Mode C Register, TM0=Timer Register 0, TM1=Timer Register 1, S=Serial Register.
2. When register pair operands rp, rp1 are used; SP=Stack Pointer, B=BC, D=DE, H=HL, V=VA.
3. Operands rPa, rPa1, wa are used in indirect addressing and auto-increment/auto-decrement addressing modes.
   B=(BC), D=(DE), H=(HL)
   $D+=(DE)^+$, $H+=(HL)^+$, $D-=(DE)^-$, $H-=(HL)^-$.
4. When the interrupt operand f is used; F0=INTF0, F1=INTF1, F2=INTF2, FT=INTFT, FS=INTFS.

INSTRUCTION GROUPS

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
8-BIT DATA TRANSFER							
MOV	r1, A	1	4	r1 ← A			
MOV	A, r1	1	4	A ← r1			
MOV	sr, A	2	10	sr ← A			
MOV	A, sr1	2	10	A ← sr1			
MOV	r, word	4	17	r ← (word)			
MOV	word, r	4	17	(word) ← r			
MVI	r, byte	2	7	r ← byte			
MVIW	wa, byte	3	13	(V, wa) ← byte			
MVIX	rpa1, byte	2	10	(rpa1) ← byte			
STAW	wa	2	10	(V, wa) ← A			
LDAW	wa	2	10	A ← (V, wa)			
STAX	rpa	1	7	(rpa) ← A			
LDAX	rpa	1	7	A ← (rpa)			
EXX		1	4	Exchange register sets			
EX		1	4	V, A ↔ V, A			
BLOCK		1	13 (C+1)	$(DE)^+ \leftarrow (HL)^+$, C ← C − 1			
16-BIT DATA TRANSFER							
SBCD	word	4	20	(word) ← C, (word + 1) ← B			
SDED	word	4	20	(word) ← E, (word + 1) ← D			
SHLD	word	4	20	(word) ← L, (word + 1) ← H			
SSPD	word	4	20	(word) ← SP_L, (word + 1) ← SP_H			
LBCD	word	4	20	C ← (word), B ← (word + 1)			
LDED	word	4	20	E ← (word), D ← (word + 1)			
LHLD	word	4	20	L ← (word), H ← (word + 1)			
LSPD	word	4	20	SP_L ← (word), SP_H ← (word + 1)			
PUSH	rp1	2	17	(SP − 1) ← $rp1_H$, (SP − 2) ← $rp1_L$			
POP	rp1	2	15	$rp1_L$ ← (SP) $rp1_H$ ← (SP + 1), SP ← SP + 2			
LXI	rp, word	3	10	rp ← word			
TABLE		1	19	C ← (PC + 2 + A) B ← (PC + 2 + A + 1)			

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
ARITHMETIC							
ADD	A, r	2	8	A ← A + r		↕	↕
ADD	r, A	2	8	r ← r + A		↕	↕
ADDX	rpa	2	11	A ← A + (rpa)		↕	↕
ADC	A, r	2	8	A ← A + r + CY		↕	↕
ADC	r, A	2	8	r ← r + A + CY		↕	↕
ADCX	rpa	2	11	A ← A + (rpa) + CY		↕	↕
SUB	A, r	2	8	A ← A − r		↕	↕
SUB	r, A	2	8	r ← r − A		↕	↕
SUBX	rpa	2	11	A ← A − (rpa)		↕	↕
SBB	A, r	2	8	A ← A − r − CY		↕	↕
SBB	r, A	2	8	r ← r − A − CY		↕	↕
SBBX	rpa	2	11	A ← A − (rpa) − CY		↕	↕
ADDNC	A, r	2	8	A ← A + r	No Carry	↕	↕
ADDNC	r, A	2	8	r ← r + A	No Carry	↕	↕
ADDNCX	rpa	2	11	A ← A + (rpa)	No Carry	↕	↕
SUBNB	A, r	2	8	A ← A − r	No Borrow	↕	↕
SUBNB	r, A	2	8	r ← r − A	No Borrow	↕	↕
SUBNBX	rpa	2	11	A ← A − (rpa)	No Borrow	↕	↕
LOGICAL							
ANA	A, r	2	8	A ← A ∧ r			↕
ANA	r, A	2	8	r ← r ∧ A			↕
ANAX	rpa	2	11	A ← A ∧ (rpa)			↕
ORA	A, r	2	8	A ← A ∨ r			↕
ORA	r, A	2	8	r ← r ∨ A			↕
ORAX	rpa	2	11	A ← A ∨ (rpa)			↕
XRA	A, r	2	8	A ← A ∨̄ r			↕
XRA	r, A	2	8	A ← r ∨̄ A			↕
XRAX	rpa	2	11	A ← A ∨̄ (rpa)			↕
GTA	A, r	2	8	A − r − 1	No Borrow	↕	↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
LOGICAL (CONT.)							
GTAX	rpa	2	11	A – (rpa) – 1	No Borrow	↕	↕
LTA	A, r	2	8	A – r	Borrow	↕	↕
LTA	r, A	2	8	r – A	Borrow	↕	↕
LTAX	rpa	2	11	A – (rpa)	Borrow	↕	↕
ONA	A, r	2	8	A ∧ r	No Zero		↕
ONAX	rpa	2	11	A ∧ (rpa)	No Zero		↕
OFFA	A, r	2	8	A ∧ r	Zero		↕
OFFAX	rpa	2	11	A ∧ (rpa)	Zero		↕
NEA	A, r	2	8	A – r	No Zero	↕	↕
NEA	r, A	2	8	r – A	No Zero	↕	↕
NEAX	rpa	2	11	A – (rpa)	No Zero	↕	↕
EQA	A, r	2	8	A – r	Zero	↕	↕
EQA	r, A	2	8	r – A	Zero	↕	↕
EQAX	rpa	2	11	A – (rpa)	Zero	↕	↕
IMMEDIATE DATA TRANSFER (ACCUMULATOR)							
XRI	A, byte	2	7	A ← A ∨ byte			↕
ADINC	A, byte	2	7	A ← A + byte	No Carry	↕	↕
SUINB	A, byte	2	7	A ← A – byte	No Borrow	↕	↕
ADI	A, byte	2	7	A ← A + byte		↕	↕
ACI	A, byte	2	7	A ← A + byte + CY		↕	↕
SUI	A, byte	2	7	A ← A – byte		↕	↕
SBI	A, byte	2	7	A ← A – byte – CY		↕	↕
ANI	A, byte	2	7	A ← A ∧ byte			↕
ORI	A, byte	2	7	A ← A ∨ byte			↕
GTI	A, byte	2	7	A – byte – 1	No Borrow	↕	↕
LTI	A, byte	2	7	A – byte	Borrow	↕	↕
ONI	A, byte	2	7	A ∧ byte	No Zero		↕
OFFI	A, byte	2	7	A ∧ byte	Zero		↕
NEI	A, byte	2	7	A – byte	No Zero	↕	↕
EQI	A, byte	2	7	A – byte	Zero	↕	↕

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INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER							
XRI	r, byte	3	11	r ← r ∀ byte			↕
ADINC	r, byte	3	11	r ← r + byte	No Carry	↕	↕
SUINB	r, byte	3	11	r ← r − byte	No Borrow	↕	↕
ADI	r, byte	3	11	r ← r + byte		↕	↕
ACI	r, byte	3	11	r ← r + byte + CY		↕	↕
SUI	r, byte	3	11	r ← r − byte		↕	↕
SBI	r, byte	3	11	r ← r − byte − CY		↕	↕
ANI	r, byte	3	11	r ← r ∧ byte		↕	↕
ORJ	r, byte	3	11	r ← r ∨ byte			↕
GTI	r, byte	3	11	r − byte − 1	No Borrow	↕	↕
LTI	r, byte	3	11	r − byte	Borrow	↕	↕
ONI	r, byte	3	11	r ∧ byte	No Zero		↕
OFFI	r, byte	3	11	r ∧ byte	Zero		↕
NEI	r, byte	3	11	r − byte	No Zero	↕	↕
EQI	r, byte	3	11	r − byte	Zero	↕	↕
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER)							
XRI	sr2, byte	3	17	sr2 ← sr2 ∀ byte			↕
ADINC	sr2, byte	3	17	sr2 ← sr2 + byte	No Carry	↕	↕
SUINB	sr2, byte	3	17	sr2 ← sr2 − byte	No Borrow	↕	↕
ADI	sr2, byte	3	17	sr2 ← sr2 + byte		↕	↕
ACI	sr2, byte	3	17	sr2 ← sr2 + byte + CY		↕	↕
SUI	sr2, byte	3	17	sr2 ← sr2 − byte		↕	↕
SBI	sr2, byte	3	17	sr2 ← sr2 − byte − CY		↕	↕
ANI	sr2, byte	3	17	sr2 ← sr2 ∧ byte			↕
ORI	sr2, byte	3	17	sr2 ← sr2 ∨ byte			↕
GTI	sr2, byte	3	14	sr2 − byte − 1	No Borrow	↕	↕
LTI	sr2, byte	3	14	sr2 − byte	Borrow	↕	↕
ONI	sr2, byte	3	14	sr2 ∧ byte	No Zero		↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER) (CONT.)							
OFFI	sr2, byte	3	14	sr2 ∧ byte	Zero		↕
NEI	sr2, byte	3	14	sr2 – byte	No Zero	↕	↕
EQI	sr2, byte	3	14	sr2 – byte	Zero	↕	↕
WORKING REGISTER							
XRAW	wa	3	14	A ← A ⊻ (V, wa)			↕
ADDNCW	wa	3	14	A ← A + (V, wa)	No Carry	↕	↕
SUBNBW	wa	3	14	A ← A – (V, wa)	No Borrow	↕	↕
ADDW	wa	3	14	A ← A + (V, wa)		↕	↕
ADCW	wa	3	14	A ← A + (V, wa) + CY		↕	↕
SUBW	wa	3	14	A ← A – (V, wa)		↕	↕
SBBW	wa	3	14	A ← A – (V, wa) – CW		↕	↕
ANAW	wa	3	14	A ← A ∧ (V, wa)			↕
ORAW	wa	3	14	A ← A ∨ (V, wa)			↕
GTAW	wa	3	14	A ← (V, wa) – 1	No Borrow	↕	↕
LTAW	wa	3	14	A – (V, wa)	Borrow	↕	↕
ONAW	wa	3	14	A ∧ (V, wa)	No Zero		↕
OFFAW	wa	3	14	A ∧ (V, wa)	Zero		↕
NEAW	wa	3	14	A – (V, wa)	No Zero	↕	↕
EQAW	wa	3	14	A – (V, wa)	Zero	↕	↕
ANIW	wa, byte	3	16	(V, wa) ← (V, wa) ∧ byte			↕
ORIW	wa, byte	3	16	(V, wa) ← (V, wa) ∨ byte			↕
GTIW	wa, byte	3	13	(V, wa) – byte – 1	No Borrow	↕	↕
LTIW	wa, byte	3	13	(V, wa) – byte	Borrow	↕	↕
ONIW	wa, byte	3	13	(V, wa) ∧ byte	No Zero		↕
OFFIW	wa, byte	3	13	(V, wa) ∧ byte	Zero		↕
NEIW	wa, byte	3	13	(V, wa) – byte	No Zero	↕	↕
EQIW	wa, byte	3	13	(V, wa) – byte	Zero	↕	↕
INCREMENT/DECREMENT							
INR	r2	1	4	r2 ← r2 + 1	Carry		↕
INRW	wa	2	13	(V, wa) ← (V, wa) + 1	Carry		↕

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INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
INCREMENT/DECREMENT (CONT.)							
DCR	r2	1	4	r2 ← r2 − 1	Borrow		↕
DCRW	wa	2	13	(V, wa) ← (V, wa) − 1	Borrow		↕
INX	rp	1	7	rp ← rp + 1			
DCX	rp	1	7	rp ← rp − 1			
DAA		1	4	Decimal Adjust Accumulator		↕	↕
STC		2	8	CY ← 1		1	
CLC		2	8	CY ← 0		0	
ROTATE AND SHIFT							
RLD		2	17	Rotate Left Digit			
RRD		2	17	Rotate Right Digit			
RAL		2	8	Am + 1 ← Am, A_0 ← CY, CY ← A_7		↕	
RCL		2	8	Cm + 1 ← Cm, C_0 ← CY, CY ← C_7		↕	
RAR		2	8	Am − 1 ← Am, A_7 ← CY, CY ← A_0		↕	
RCR		2	8	Cm − 1 ← Cm, C_7 ← CY, CY ← C_0		↕	
SHAL		2	8	Am + 1 ← Am, A_0 ← 0, CY ← A_7		↕	
SHCL		2	8	Cm + 1 ← CM, C_0 ← 0, CY ← C_7		↕	
SHAR		2	8	Am − 1 ← Am, A_7 ← 0, CY ← A_0		↕	
SHCR		2	8	Cm − 1 ← Cm, C_7 ← 0, CY ← C_0		↕	
JUMP							
JMP	word	3	10	PC ← word			
JB		1	4	PC_H ← B, PC_L ← C			
JR	word	1	13	PC ← PC + 1 + jdisp1			
JRE	word	2	13	PC ← PC + 2 + jdisp			
CALL							
CALL	word	3	16	(SP − 1) ← $(PC - 3)_H$, (SP − 2) ← $(PC - 3)_L$, PC ← word			
CALB		1	13	(SP − 1) ← $(PC - 1)_H$, (SP − 2) ← $(PC - 1)_L$, PC_H ← B, PC_L ← C			
CALF	word	2	16	$(SP-1)\leftarrow(PC-2)_H$, $(SP-2)\leftarrow(PC-2)_L$ PC15 ~ 11 ← 00001, PC10 ~ 0 ← fa			
CALT	word	1	19	$(SP-1)\leftarrow(PC-1)_H$, $(SP-2)\leftarrow(PC-1)_L$ $PC_L\leftarrow(128-2ta)$, $PC_H\leftarrow(129+2ta)$			
SOFTI		1	19	(SP − 1) ← PSW, SP − 2, (SP − 3) ← PC PC ← 0060_H, SIRQ ← 1			

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
RETURN							
RET		1	11	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1)$ $SP \leftarrow SP - 2$			
RETS		1	11+a	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1),$ $SP \leftarrow SP + 2, PC \leftarrow PC + n$			
RETI		1	15	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1)$ $PSW \leftarrow (SP+2), SP \leftarrow SP+3, SIRQ \leftarrow 0$			
SKIP							
BIT	bit, wa	2	10	Bit test	$(V, wa)_{bit} = 1)$		
SKC		2	8	Skip if Carry	CY = 1		
SKNC		2	8	Skip if No Carry	CY = 0		
SKZ		2	8	Skip if Zero	Z = 1		
SKNZ		2	8	Skip if No Zero	Z = 0		
SKIT	f	2	8	Skip if INT X = 1, then reset INT X	f = 1		
SKNIT	f	2	8	Skip if No INT X otherwise reset INT X	f = 0		
CPU CONTROL							
NOP		1	4	No Operation			
EI		2	8	Enable Interrupt			
DI		2	8	Disable Interrupt			
HLT		1	6	Halt			
SERIAL PORT CONTROL							
SIO		1	4	Start (Trigger) Serial I/O			
STM		1	4	Start Timer			
INPUT/OUTPUT							
IN	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow$ byte $A \leftarrow DB_{7-0}$			
OUT	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow$ byte $DB_{7-0} \leftarrow A$			
PEX		2	11	$PE_{15-8} \leftarrow B, PE_{7-0} \leftarrow C$			
PEN		2	11	$PE_{15-12} \leftarrow B_{7-4}$			
PER		2	11	Port E AB Mode			

Program Status Word (PSW) Operation

OPERATION						D6	D5	D4	D3	D2	D0
REG, MEMORY			IMMEDIATE		SKIP	Z	SK	HC	L1	L0	CY
ADD ADC SUB SBB	ADDW ADCW SUBW SBBW	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			↕	0	↕	0	0	↕
ANA ORA XRA	ANAW ORAW XRAW	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		↕	0	•	0	0	•
ADDNC SUBNB GTA LTA	ADDNCW SUBNBW GTAW LTAW	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	 GTIW LTIW		↕	↕	↕	0	0	↕
ONA OFFA	ONAW OFFAW	ONAX OFFAX	ONI OFFI	ONIW OFFIW		↕	↕	•	0	0	•
NEA EQA	NEAW EQAW	NEAX EQAX	NEI EQI	NEIW EQIW		↕	↕	↕	0	0	↕
INR DCR	INRW DCRW					↕	↕	↕	0	0	•
DAA						↕	0	↕	0	0	↕
RAL, RAR, RCL, RCR SHAL, SHAR, SHCL, SHCR						•	0	•	0	0	↕
RLD, RRD						•	0	•	0	0	•
STC						•	0	•	0	0	1
CLC						•	0	•	0	0	0
			MVI A, byte			•	0	•	1	0	•
			MVI L, byte LXI H, word			•	0	•	0	1	•
					BIT SKC SKNC SKZ SKNZ SKIT SKNIT	•	↕	•	0	0	•
					RETS	•	1	•	0	0	•
All other instructions						•	0	•	0	0	•

↕ Flag affected according to result of operation
1 Flag set
0 Flag reset
• Flag not affected

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Voltage On Any Pin . . . . . −0.3V to +7.0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

−10 to +70°C, V_{CC} = +5.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	200	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

AC CHARACTERISTICS

-10 to $+70°C$, $V_{CC} = +5.0V \pm 10\%$

CLOCK TIMING

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X1 Input Cycle Time	t_{CYX}	227	1000	ns	
X1 Input Low Level Width	t_{XXL}	106		ns	
X1 Input High Level Width	t_{XXH}	106		ns	
ϕ_{OUT} Cycle Time	$t_{CY\phi}$	454	2000	ns	
ϕ_{OUT} Low Level Width	$t_{\phi\phi L}$	150		ns	
ϕ_{OUT} High Level Width	$t_{\phi\phi H}$	150		ns	
ϕ_{OUT} Rise/Fall Time	t_r, t_f		40	ns	

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → ϕ_{OUT} L.E.	$t_{R\phi}$	100		ns	
Address ($PE_{0\text{-}15}$) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	200(T3); 700(T4)		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address ($PE_{0\text{-}15}$) → $\overline{WAIT}$ L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from ϕ_{OUT} L.E.)	t_{WTS}	290		ns	
$\overline{WAIT}$ Hold Time (Referenced from ϕ_{OUT} L.E.)	t_{WTH}	0		ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	$t_{CY\phi}$ = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
ϕ_{OUT} L.E. → $\overline{WR}$ L.E.	$t_{\phi W}$	40	125	ns	
Address ($PE_{0\text{-}15}$) → ϕ_{OUT} T.E.	$t_{A\phi}$	100	300	ns	
Address ($PE_{0\text{-}15}$) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address ($PE_{0\text{-}15}$) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

SERIAL I/O OPERATION

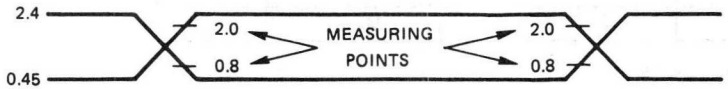
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		900	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	140		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from ϕ_{OUT} L.E.)	t_{HDS_1}	200		ns	$t_{CY\phi}$ = 500 ns
	t_{HDS_2}	200		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	0		ns	
ϕ_{OUT} L.E. → HLDA	t_{DHA}	110	100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)



② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

AC CHARACTERISTICS (CONT.)

$t_{CY\phi}$ DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
$t_{R\phi}$	(1/5) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
$t_{\phi W}$	(1/4) T	MAX	ns
$t_{A\phi}$	(1/5) T	MIN	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns

Notes: ① N = Number of Wait States

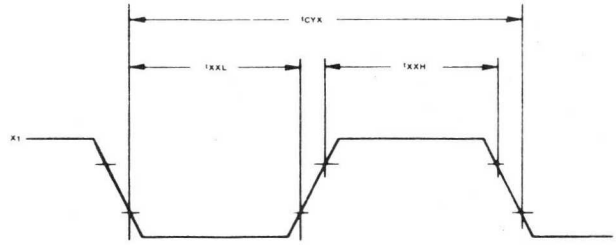
② T = $t_{CY\phi}$

③ Only above parameters are t_{CY_ϕ} dependent

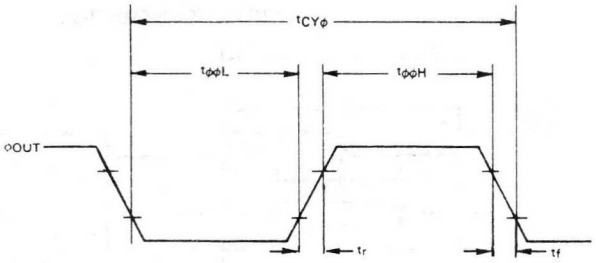
④ When a crystal frequency other than 4 MHz is used (t_{CY_ϕ} = 500 ns) the above equations can be used to calculate AC parameter values.

TIMING WAVEFORMS

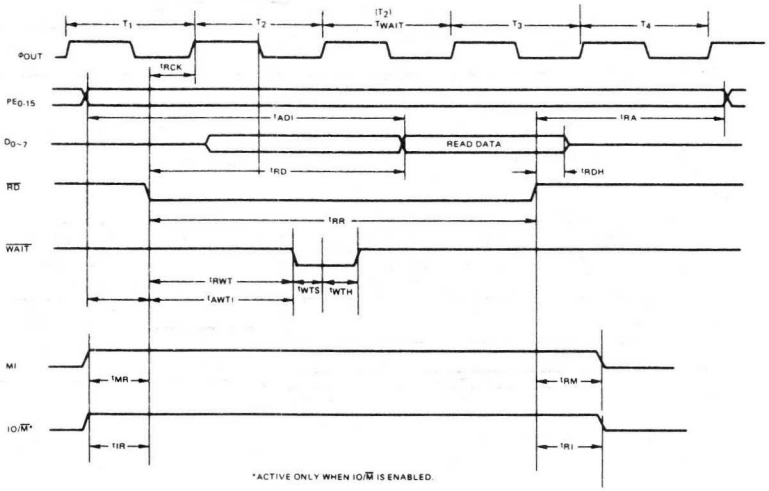
CLOCK TIMING



TIMING WAVEFORMS
(CONT.)

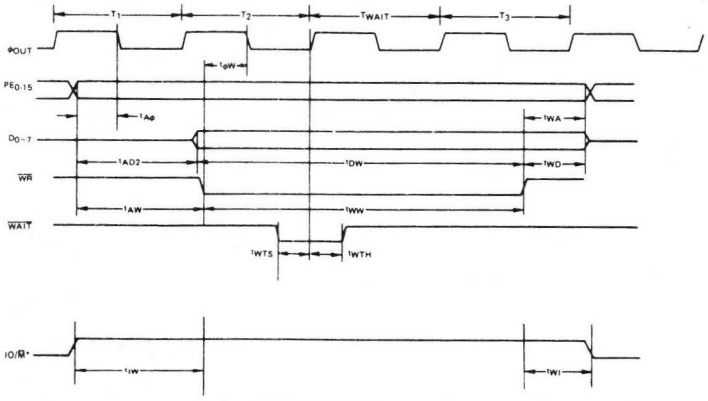


READ OPERATION



*ACTIVE ONLY WHEN IO/M IS ENABLED.

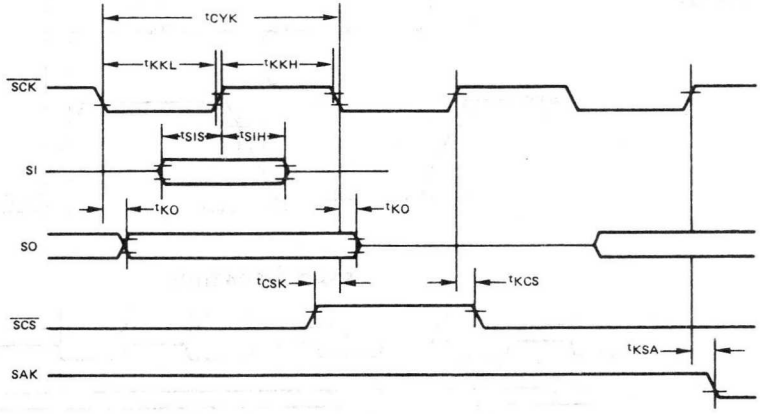
WRITE OPERATION



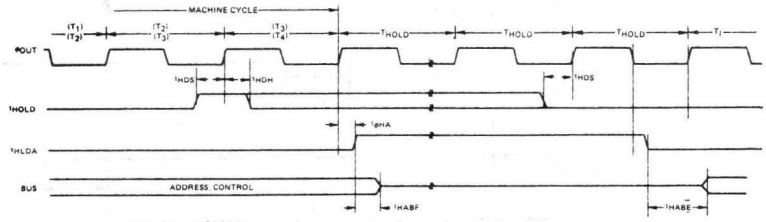
*ACTIVE ONLY WHEN IO/M IS ENABLED.

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SERIAL I/O OPERATION

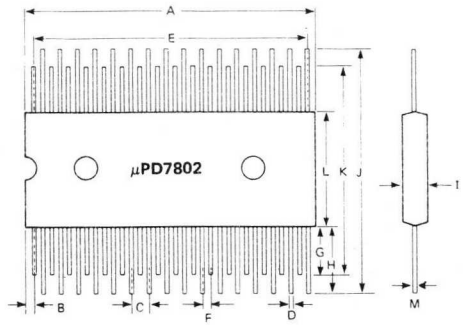


HOLD OPERATION



PACKAGE INFORMATION

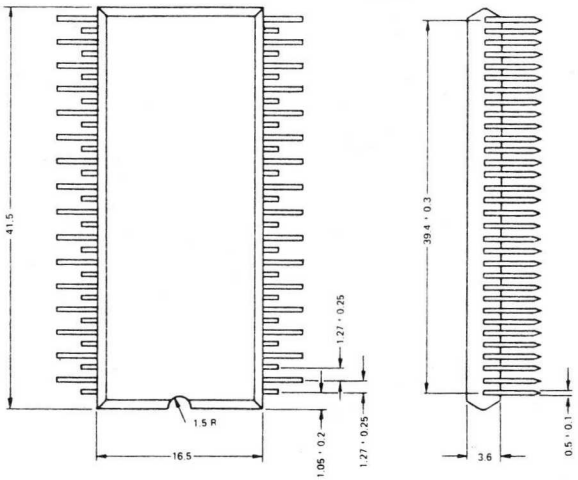
STRAIGHT LEADS



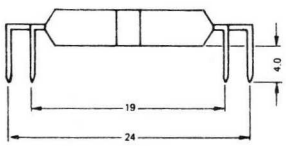
(Plastic)

ITEM	MILLIMETERS	INCHES
A	41.8 MAX	1.65
B	1.22	0.05
C	2.54	0.1
D	0.5 ± 0.1	0.02 + 0.004
E	39.37	1.55
F	1.27	0.05
G	6.75	0.27
H	9.3	0.37
I	3.6	0.14
J	35.1	1.38
K	30.0	1.18
L	16.5	0.65
M	0.25 ± 0.05	0.01 ± 0.002

BENT LEADS



(Unit: mm)



7802DS-12-80-CAT

NOTES

SINGLE CHIP 8-BIT MICROCOMPUTER

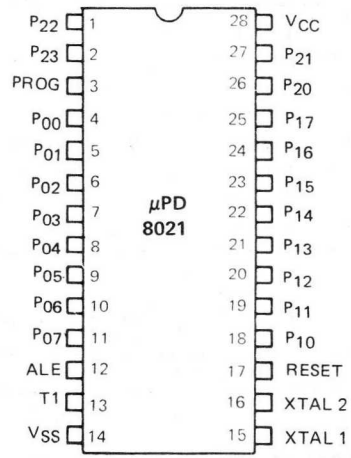
DESCRIPTION

The NEC μPD8021 is a stand alone 8-bit parallel microcomputer incorporating the following features usually found in external peripherals. The μPD8021 contains: 1K x 8 bits of mask ROM program memory, 64 x 8 bits of RAM data memory, 21 I/O lines, an 8-bit interval timer/event counter, and internal clock circuitry.

FEATURES

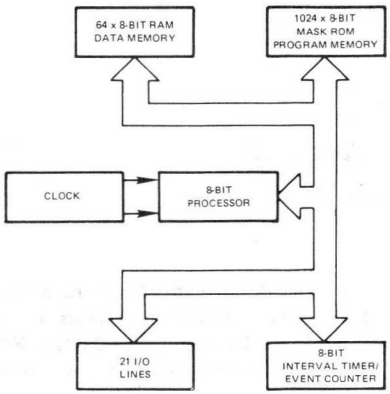
- 8-Bit Processor, ROM, RAM, I/O, Timer/Counter
- Single +5V Supply (+4.5V to +6.5V)
- NMOS Silicon Gate Technology
- 8.38 μs Instruction Cycle Time
- All Instructions 1 or 2 Cycles
- Instructions are Subset of μPD8048/8748/8035
- High Current Drive Capability – 2 I/O Pins
- Clock Generation Using Crystal or Single Inductor
- Zero-Cross Detection Capability
- Expandable I/O Using μ8243's
- Available in 28 Pin Plastic Package

PIN CONFIGURATION



7

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature (Ceramic Package) . . . . . -65°C to +150°C
(Plastic Package) . . . . . -65°C to +125°C
Voltage on Any Pin . . . . . -0.5 to +7 Volts ①
Power Dissipation. . . . . 1 Watt

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5.5V \pm 1V$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	-0.5		+ 0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2)	V_{IH}	2.0		V_{CC}	V	$V_{CC} = 5.0V \pm 10\%$
Input High Voltage (All Except XTAL 1, XTAL 2)	V_{IH1}	3.0		V_{CC}	V	$V_{CC} = 5.5V \pm 1V$
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 1.6$ mA
Output Low Voltage (P_{10}, P_{11})	V_{OL1}			2.5	V	$I_{OL} = 7$ mA
Output High Voltage (All Unless Open Drain)	V_{OH}	2.4			V	$I_{OH} = 50\,\mu A$
Output Leakage Current (Open Drain Option – Port 0)	I_{OL}			-10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V
V_{CC} Supply Current	I_{CC}			60	mA	

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = 5.5V \pm 1V$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Cycle Time	T_{CY}	8.38		50.0	μs	3.58 MHz XTAL ① for T_{CY} Min.
Oscillator Frequency Variation (Resistor Mode)	ΔF	-20		+20	%	F = 2.5 MHz ①

Note: ① Control outputs: $C_L = 80$ pF; $R_L = 2.2K/4.3K$

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1-2, 26-27	P_{20}-P_{23} (Port 2)	P_{20}-P_{23} comprise the 4-bit bi-directional I/O port which is also used as the expander bus for the μPD8243.
3	PROG	PROG is the output strobe pin for the μPD8243.
4-11	P_{00}-P_{07} (Port 0)	One of the two 8-bit quasi bi-directional I/O ports.
12	ALE	Address Latch Enable output (active-high). Occurring once every 30 input clock periods, ALE can be used as an output clock.
13	T1	Testable input using transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction. T1 also provides zero-cross sensing for low-frequency AC input signals.
14	V_{SS}	Processor's ground potential.
15	XTAL 1	One side of frequency source input using resistor, inductor, crystal or external source. (non-TTL compatible V_{IH}).
16	XTAL 2	The other side of frequency source input.
17	RESET	Active high input that initializes the processor and starts the program at location zero.
18-25	P_{10}-P_{17} (Port 1)	The second of two 8-bit quasi bi-directional I/O ports.
28	V_{CC}	+5V power supply input.

FUNCTIONAL DESCRIPTION

The NEC μPD8021 is a single component, 8-bit, parallel microprocessor using N-channel silicon gate MOS technology. The self-contained 1K x 8-bit ROM, 64 x 8-bit RAM, 8-bit timer/counter, and clock circuitry allow the μPD8021 to operate as a single-chip microcomputer in applications ranging from controllers to arithmetic processors.

The instruction set, a subset of the μPD8048/8748/8035, is optimum for high-volume, low cost applications where I/O flexibility and instruction set power are required. The μPD8021 instruction set is comprised mostly of single-byte instructions with no instructions over two bytes.

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAG C
DATA MOVES													
MOV A, = data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
MOV A, Rr	(A) ← (Rr); r = 0 - 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1	
MOV A, @ Rr	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1	
MOV Rr, = data	(Rr) ← data; r = 0 - 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2	
MOV Rr, A	(Rr) ← (A); r = 0 - 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1	
MOV @ Rr, A	((Rr)) ← (A); r = 0 - 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1	
MOV @ Rr, = data	((Rr)) ← data; r = 0 - 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2	
MOVP A, @ A	(PC 0 - 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1	
XCH A, Rr	(A) ⇄ (Rr); r = 0 - 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1	
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1	
XCHD A, @ Rr	(A 0 - 3) ⇄ ((Rr)) 0 - 3)); r = 0 - 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1	
FLAGS													
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•
INPUT/OUTPUT													
ANLD P_p, A	(P_p) ← (P_p) AND (A 0 - 3) p = 4 - 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1	
IN A, P_p	(A) ← (P_p); p = 1 - 2	Input data from designated port (1 - 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1	
MOVD A, P_p	(A 0 - 3) ← (P_p); p = 4 - 7 (A 4 - 7) ← 0	Move contents of designated port (4 - 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1	
MOVD P_p, A	(P_p) ← A 0 - 3; p = 4 - 7	Move contents of Accumulator to designated port (4 - 7).	0	0	1	1	1	1	p	p	1	1	
ORLD P_p, A	(P_p) ← (P_p) OR (A 0 - 3) p = 4 - 7	Logical or contents of Accumulator with designated port (4 - 7).	1	0	0	0	1	1	p	p	1	1	
OUTL P_p, A	(P_p) ← (A); p = 1 - 2	Output contents of Accumulator to designated port (1 - 2).	0	0	1	1	1	0	p	p	1	1	
REGISTERS													
INC Rr	(Rr) ← (Rr) + 1; r = 0 - 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1	
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 - 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1	
SUBROUTINE													
CALL addr	((SP)) ← (PC), (PSW 4 - 7) (SP) ← (SP) + 1 (PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2	
RET	(SP) ← (SP) - 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1	
TIMER/COUNTER													
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1	
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1	
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1	
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1	
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1	
MISCELLANEOUS													
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1	

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

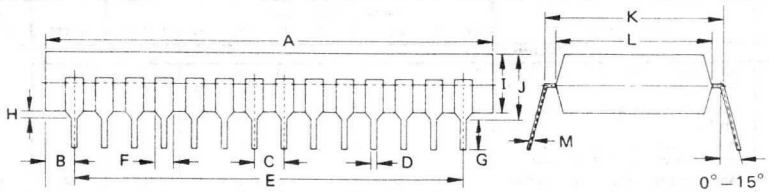
Symbol Definitions

SYMBOL	DESCRIPTION
A	The Accumulator
addr	Program Memory Address (12 bits)
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
P	"In-Page" Operation Designator
P_p	Port Designator (p = 1, 2 or 4 - 7)
Rr	Register Designator (r = 0, 1 or 0 - 7)

SYMBOL	DESCRIPTION
T	Timer
• T_1	Testable Flag 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location
←	Replaced By

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAG C
ACCUMULATOR													
ADD A, = data	(A) ← (A) + data	Add immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•
Add A, Rr	(A) ← (A) + (Rr) for r = 0 - 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 - 1	Add indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•
ADDC A, = data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 - 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 - 1	Add indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 - 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1	
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 - 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1	
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1	
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1	
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•
DEC A	(A) ← (A) - 1	DECREMENT by 1 the Accumulator's contents.	0	0	0	0	0	1	1	1	1	1	
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents.	0	0	0	1	0	1	1	1	1	1	
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 - 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1	
ORL A @ Rr	(A) ← (A) OR ((Rr)) for r = 0 - 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1	
RL A	(AN + 1)← (AN) (A_0) ← (A_7) for N = 0 - 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1	
RLC A	(AN + 1) ← (AN); N = 0 - 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•
RR A	(AN) ← (AN + 1); N = 0 - 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1	
RRC A	(AN) ← (AN +1); N = 0 - 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•
SWAP A	(A_{4-7}) ⇄ (A_0 - 3)	Swap the 24-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1	
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 - 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1	
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 - 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1	
BRANCH													
DJNZ Rr, addr	(Rr) ← (Rr) - 1; r = 0 - 7 If (Rr) ≠ 0 (PC 0 - 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2	
JC addr	(PC 0 - 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JMP addr	(PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2	
JMPP @ A	(PC 0 - 7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1	
JNC addr	(PC 0 - 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JNT1 addr	(PC 0 - 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JNZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JTF addr	(PC 0 - 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JT1 addr	(PC 0 - 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	

PACKAGE OUTLINE
μPD8021C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

SINGLE CHIP 8-BIT MICROCOMPUTER WITH ON-CHIP A/D CONVERTER

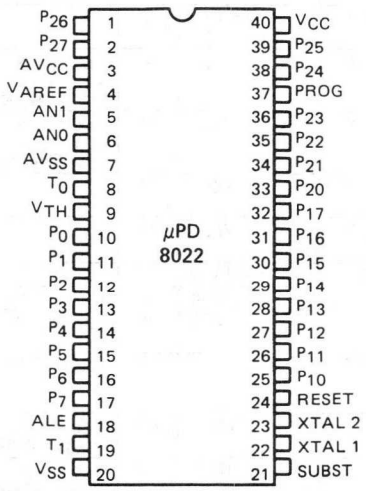
DESCRIPTION

The NEC μPD8022 is designed for low cost, high volume applications requiring large ROM space, analog to digital conversion capability, a capacitive touchpanel keyboard interface and/or a power line time base. The μPD8022 satisfies these requirements by integrating on one chip, an 8-bit μPD8021 type processor with 2K of ROM, a 2 channel 8-bit A/D converter, a high impedance comparator input port, and a zero crossing detector.

FEATURES

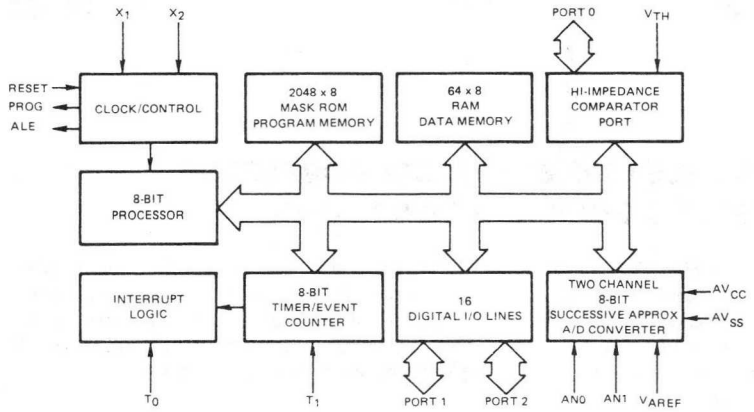
- 8-Bit Processor, ROM, RAM, I/O and Clock Generator
- Single +5V Supply (4.5V to 6.5V)
- NMOS Silicon Gate Technology
- 2K x 8 ROM, 64 x 8 RAM, 26 I/O Lines
- On Chip 8-Bit A/D Converter with 2 Input Channels
- 8.3 μs Instruction Cycle Timer
- Instructions are a Subset of μPD8048; Superset of μPD8021
- Internal Timer/Event Counter
- External and Timer/Counter Interrupts
- On-Chip Zero-Cross Detector
- High Impedance Comparator Port with Variable Threshold
- Clock Generator Using a Crystal or Single Inductor
- High Current Drive Capability on 2 I/O Pins
- Expandable I/O Utilizing the μPD8243
- Available in 40-Pin Plastic Dual-In-Line Package

PIN CONFIGURATION



7

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Plastic Package)	-65°C to +125°C
Voltage on Any Pin	-0.5 to +7 Volts①
Power Dissipation	1 Watt

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5.5V ± 1V, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage	V_{IL}	-0.5		0.8	V	V_{TH} Floating
Input Low Voltage (Port 0)	V_{IL1}	-0.5		V_{TH}-0.1	V	
Input High Voltage (All except XTAL 1, RESET)	V_{IH}	2.0		V_{CC}	V	V_{CC} = 5.0V ± 10% V_{TH} Floating
Input High Voltage (All except XTAL 1, RESET)	V_{IH1}	3.0		V_{CC}	V	V_{CC} = 5.5V ± 1V V_{TH} Floating
Input High Voltage (Port 0)	V_{IH2}	V_{TH}+0.1		V_{CC}	V	
Input High Voltage (RESET, XTAL 1)	V_{IH3}	3.0		V_{CC}	V	
Port 0 Threshold Voltage	V_{TH}	0		0.4 V_{CC}	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.6 mA
Output Low Voltage (P_{10}, P_{11})	V_{OL1}			0.25	V	I_{OL} = 7 mA
Output High Voltage (All unless open drain option for Port 0)	V_{OH}	2.4			V	I_{OH} = 50 μA
Input Current (T1)	I_{L1}			±200	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V
Output Leakage Current (Open drain option for Port 0)	I_{LO}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V
V_{CC} Supply Current	I_{CC}			100	mA	

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
8	T_0	Active low interrupt input if enabled. Also testable using the conditional jump instructions JTO and JNTO.
19	T_1	Zero-cross detector input. After executing a STRT CNT instruction this becomes the event counter input. Also testable using the conditional jump instructions JT1 and JNT1. Optional ROM mask pull-up resistor available.
6	AN0	Analog input to the A/D converter after execution of the SEL AN0 instruction.
5	AN1	Analog input to the A/D converter after execution of the SEL AN1 instruction.
22	XTAL 1	Input for internal oscillator connected to one side of a crystal or inductor. Serves as an external frequency input also (Non-TTL compatible V_{IH}).
23	XTAL 2	Input for internal oscillator connected to the other side of a crystal or inductor. This pin is not used when employing an external frequency source.
37	PROG	Strobe output for the μPD8243 I/O expander.
18	ALE	Active high address latch enable output occurring once every instruction cycle. Can be used as an output clock.
24	RESET	Active high input that initializes the processor to a defined state and starts the program at memory location zero.
40	V_{CC}	+5V power supply.
3	AV_{CC}	+5V A/D converter power supply.
20	V_{SS}	Power supply ground potential.
7	AV_{SS}	A/D converter power supply ground potential. Sets conversion range lower limit.
4	VA_{REF}	Reference voltage for A/D converter. Sets conversion range upper limit.
9	V_{TH}	Port 0 comparator threshold reference input.
21	SUBST	Substrate connection used with bypass capacitor to V_{SS} for substrate voltage stabilization and improvement of A/D accuracy.
10-17	P_{00}-P_{07}	Port 0. 8-bit open drain I/O port with comparator inputs. The reference threshold is set via V_{TH}. Optional ROM mask pull-up resistors available.
25-32	P_{10}-P_{17}	Port 1. 8-bit quasi-bidirectional port. TTL compatible.
1-2 33-36 38-39	P_{20}-P_{27}	Port 2. 8-bit quasi-bidirectional port. TTL compatible. P_{20}-P_{23} also function as an I/O expander port for the μPD8243.

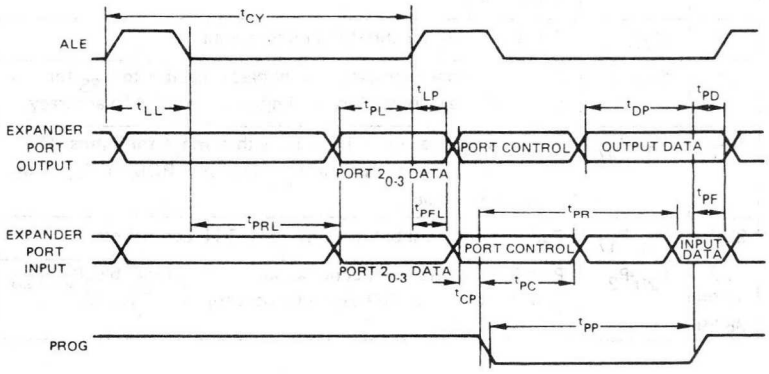
AC CHARACTERISTICS

$T_a = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Cycle Time	t_{CY}	8.38		50.0	μs	3.58 MHz XTAL for t_{CY} min.
Zero-Cross Detection Input (T1)	V_{T1}	1		3	VAC_{pp}	AC coupled
Zero-Cross Accuracy	A_{ZC}			±135	mV	60 Hz Sine Wave
Zero-Cross Detection Input Frequency (T1)	F_{T1}	0.06		1	kHz	
Port Control Setup Before Falling Edge of PROG	t_{CP}	0.5			μs	$t_{CY} = 8.38$ μs, $C_L = 80$ pF
Port Control Hold After Falling Edge of PROG	t_{PC}	0.8			μs	$t_{CY} = 8.38$ μs, $C_L = 80$ pF
PROG to Time P2 Input Must be Valid	t_{PR}			1.0	μs	$t_{CY} = 8.38$ μs, $C_L = 80$ pF
Output Data Setup Time	t_{PP}	7.0			μs	$t_{CY} = 8.38$ μs, $C_L = 80$ pF
Output Data Hold Time	t_{PD}	8.3			μs	$t_{CY} = 8.38$ μs, $C_L = 80$ pF
Input Data Hold Time	t_{PF}	0		150	μs	$t_{CY} = 8.38$ μs, $C_L = 80$ pF
PROG Pulse Width	t_{PP}	8.3			μs	$t_{CY} = 8.38$ μs, $C_L = 80$ pF
ALE to Time P2 Input Must be Valid	t_{PRL}			3.6	μs	$t_{CY} = 8.38$ μs, $C_L = 80$ pF
Output Data Setup Time	t_{PL}	0.8			μs	$t_{CY} = 8.38$ μs, $C_L = 80$ pF
Output Data Hold Time	t_{LP}	1.6			μs	$t_{CY} = 8.38$ μs, $C_L = 80$ pF
Input Data Hold Time	t_{PFL}	0			μs	$t_{CY} = 8.38$ μs, $C_L = 80$ pF
ALE Pulse Width	t_{LL}	3.9		23.0	μs	$t_{CY} = 8.38$ μs for min.

TIMING WAVEFORM

PORT 2 TIMING



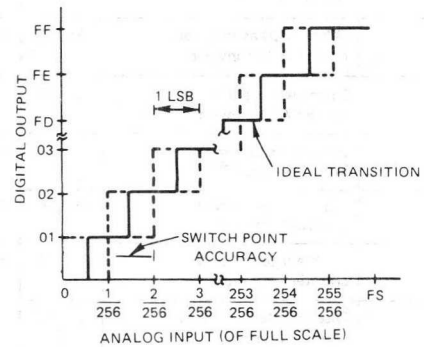
A/D CONVERTER CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5.5V ± 1V, V_{SS} = 0V, AV_{CC} = 5.5V ± 1V, AV_{SS} = 0V
$AV_{CC}/2 \leqslant V_{AREF} \leqslant AV_{CC}$

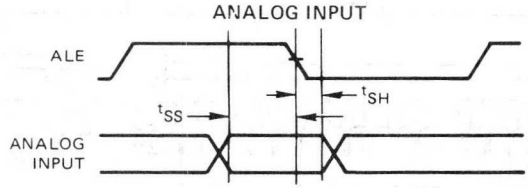
PARAMETER	SYMBOL	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
Resolution		8			BITS	
Switch Point Accuracy	A_{SP}		±½		LSB	②
Absolute Accuracy	A_{AB}		±1		LSB	
Sample Setup Before Falling Edge of ALE	t_{SS}		0.20		t_{CY}	①
Sample Hold After Falling Edge of ALE	t_{SH}		0.10		t_{CY}	①
Input Capacitance (AN0, AN1)	C_{AD}		1		pF	
Conversion Time	t_{CNV}	4		4	t_{CY}	
Conversion Range		AV_{SS}		V_{AREF}	V	
Reference Voltage	V_{AREF}	$AV_{CC}/2$		AV_{CC}	V	

Note: ① The analog signal on AN0 and AN1 must remain constant during the sample time $t_{SS} + t_{SH}$.

②



TIMING WAVEFORM



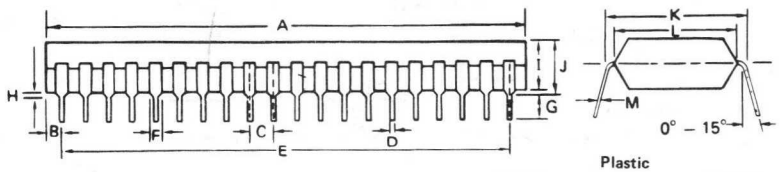
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INSTRUCTION SET

The instruction set of the μPD8022 is a subset of the μPD8048 instruction set except for three instructions, SEL AN0, SEL AN1, and RAD, which are unique to the μPD8022. The μPD8022 instruction set is also a superset of the μPD8021, meaning that the μPD8022 will execute ALL of the μPD8021 instructions PLUS some additional instructions which are listed below. For a summary of the μPD8021 instruction set, please refer to that section. Symbols used below are defined in the same manner as in that section. Also note that the instructions listed below do not affect any status flags.

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								CYCLES	BYTES
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
JTO addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if T0 is high	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNTO addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if T0 is low	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
RAD	(A) ← (CRR)	Move to A the contents of the A/D conversion result register (CRR)	1	0	0	0	0	0	0	0	2	1
SEL AN0		Select AN0 as the input for the A/D converter	1	0	0	0	0	1	0	1	1	1
SEL AN1		Select AN1 as the input for the A/D converter	1	0	0	1	0	1	0	1	1	1
EN I		Enable the external interrupt input T0	0	0	0	0	0	1	0	1	1	1
DIS I		Disable the external interrupt input T0	0	0	0	1	0	1	0	1	1	1
EN TCNTI		Enable internal timer/ counter interrupt	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disable internal timer/ counter interrupt	0	0	1	1	0	1	0	1	1	1
RETI	(SP) ← (SP) − 1 (PC) ← ((SP))	Return from interrupt and re-enable interrupt input logic	1	0	0	1	0	0	1	1	2	1

PACKAGE OUTLINE μPD8022C



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

8022DS-12-80-CAT

UNIVERSAL PROGRAMMABLE PERIPHERAL INTERFACE — 8-BIT MICROCOMPUTER

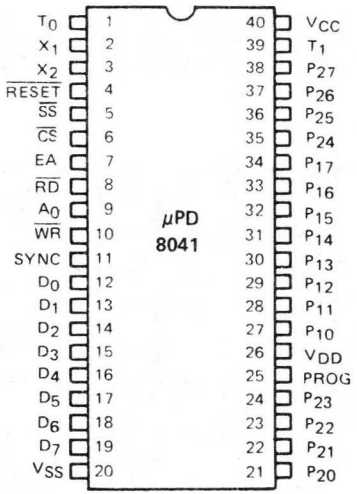
DESCRIPTION

The μPD8041 is a programmable peripheral interface intended for use in a wide range of microprocessor systems. Functioning as a totally self-sufficient controller, the μPD8041 contains an 8-bit CPU, 1K x 8 program memory, 64 x 8 data memory, I/O lines, counter/timer, and clock generator in a 40-pin DIP. The bus structure, data register, and status register enable easy interface to 8048, 8080A, or 8085A based systems.

FEATURES

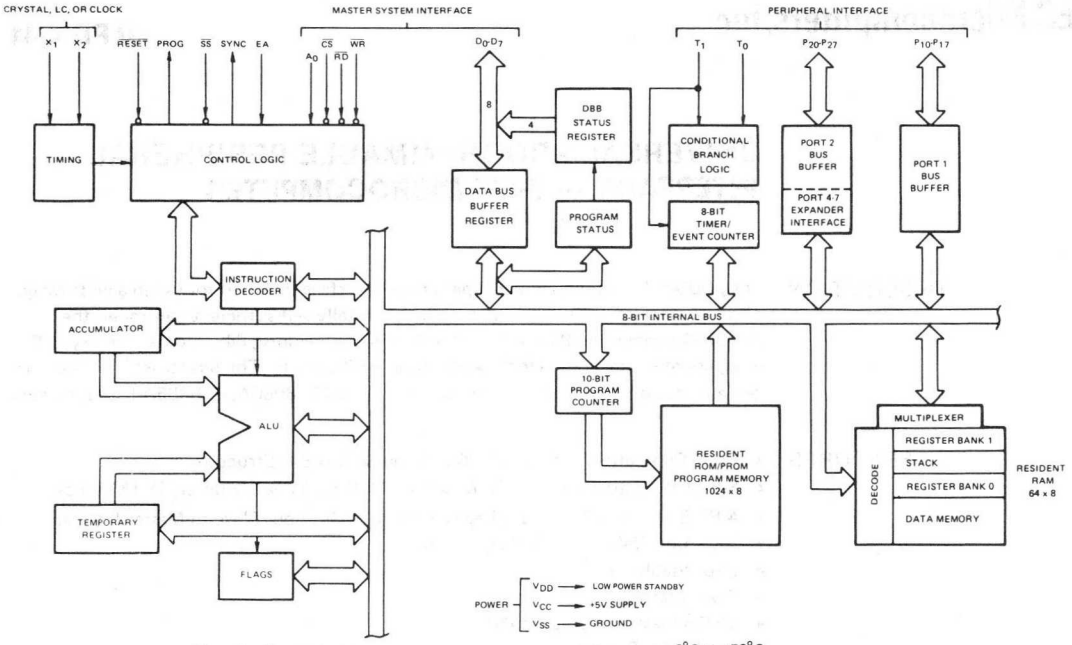
- Fully Compatible with 8048, 8080A and 8085A Bus Structure
- 8-Bit CPU with 1K x 8 ROM, 64 x 8 RAM, 8-Bit Timer/Counter, 18 I/O Lines
- 4-Bit Status and 8-Bit Data Register for Asynchronous Slave-to-Master Interface
- Interrupt, DMA, or Polled Operation
- Expandable I/O
- Two Interrupts
- 40-Pin Plastic or Ceramic DIP
- Single +5V Supply

PIN CONFIGURATION



7

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +125°C
Voltage on Any Pin	−0.5 to +7 Volts ①
Power Dissipation	1.5 Watt

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: ① With respect to ground.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{DD} = V_{CC} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage (All except X_1 and X_2)	V_{IL}	−0.5		+0.8	V	
Input Low Voltage (X_1 and X_2, $\overline{RESET}$)	V_{IL1}	−0.5		0.6	V	
Input High Voltage (All except X_1, X_2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage (X_1, X_2, $\overline{RESET}$)	V_{IH1}	3.8		V_{CC}	V	
Output Low Voltage (D_0-D_7, SYNC)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (All other outputs except PROG)	V_{OL1}			0.45	V	I_{OL} = 1.0 mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	I_{OL} = 1.0 mA
Output High Voltage (D_0-D_7)	V_{OH}	2.4			V	I_{OH} = −400 μA
Output High Voltage (All other outputs)	V_{OH1}	2.4			V	I_{OH} = −50 μA
Input Leakage Current (T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, EA, A_0)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Output Leakage Current (D_0-D_7; High Z State)	I_{OL}			±10	μA	V_{SS} + 0.45 ≤ $V_{IN} \leq V_{CC}$
V_{DD} Supply Current	I_{DD}			15	mA	
Total Supply Current	$I_{CC} + I_{DD}$			125	mA	
Low Input Source Current (P_{10}-P_{17}; P_{20}-P_{27})	I_{LI}			0.5	mA	V_{IL} = 0.8V
Low Input Source Current (SS; $\overline{RESET}$)	I_{LI1}			0.2	mA	V_{IL} = 0.8V

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1,39	T_0, T_1	Testable input pins using conditional transfer functions JT0, JNT0, JT1, JNT1. T_1 can be made the counter/timer input using the STRT CNT instruction.
2	X_1	One side of the crystal input for external oscillator or frequency source.
3	X_2	The other side of the crystal input.
4	$\overline{RESET}$	Active-low input for processor initialization. RESET is also used for power down.
5	$\overline{SS}$	Single Step input (active-low). SS together with SYNC output allows the μPD8041 to "single-step" through each instruction in program memory.
6	$\overline{CS}$	Chip Select input (active-low). CS is used to select the appropriate μPD8041 on a common data bus.
7	EA	External Access input (active-high) is used for ROM verification.
8	$\overline{RD}$	Read strobe input (active-low). RD will pulse low when the master processor reads data and status words from the DATA BUS BUFFER or Status Register.
9	A_0	Address input which the master processor uses to indicate if a byte transfer is a command or data.
10	$\overline{WR}$	Write strobe input (active-low). WR will pulse low when the master processor writes data or status words to the DATA BUS BUFFER or Status Register.
11	SYNC	The SYNC output pulses once for each μPD8041 instruction cycle. It can function as a strobe for external circuitry. SYNC can also be used together with SS to "single-step" through each instruction in program memory.
12-19	D_0-D_7 BUS	The 8-bit, bi-directional, tri-state DATA BUS BUFFER lines by which the μPD8041 interfaces to the 8-bit master system data bus.
20	V_{SS}	Processor's ground potential.
21-24, 35-38	P_{20}-P_{27}	PORT 2 is the second of two 8-bit, quasi-bi-directional I/O ports. P_{20}-P_{23} contain the four most significant bits of the program counter during external memory fetches. P_{20}-P_{23} also serve as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	Program Pulse. PROG is used as an output strobe for the μPD8243.
26	V_{DD}	V_{DD} is +5V for normal operation of the μPD8041. V_{DD} is also the Low Power Standby input.
27-34	P_{10}-P_{17}	PORT 1 is the first of two 8-bit quasi-bi-directional I/O ports.
40	V_{CC}	Primary power supply. V_{CC} must be +5V for the operation of the μPD8041.

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{DD} = V_{CC} = +5V; V_{SS} = 0V

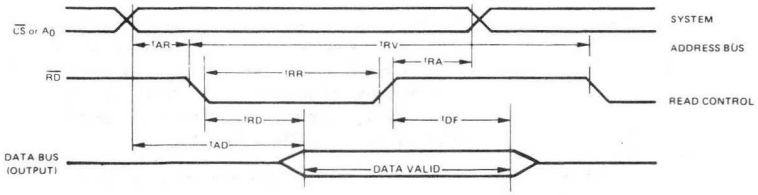
PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
DBB READ					
CS, A_0 Setup to $\overline{RD}$ ↓	t_{AR}	0		ns	
CS, A_0 Hold after $\overline{RD}$ ↑	t_{RA}	0		ns	
RD Pulse Width	t_{RR}	250		ns	t_{CY} = 2.5 μs
CS, A_0 to Data Out Delay	t_{AD}		150	ns	
RD ↓ to Data Out Delay	t_{RD}		150	ns	
RD ↑ to Data Float Delay	t_{DF}	10	100	ns	
Recovery Time between Reads and/or Writes	t_{RV}	1		μs	
Cycle Time	t_{CY}	2.5		μs	6 MHz Crystal
DBB WRITE					
CS, A_0 Setup to WR ↓	t_{AW}	0		ns	
CS, A_0 Hold after $\overline{WR}$ ↑	t_{WA}	0		ns	
WR Pulse Width	t_{WW}	250		ns	t_{CY} = 2.5 μs
Data Setup to $\overline{WR}$ ↑	t_{DW}	150		ns	
Data Hold after $\overline{WR}$ ↑	t_{WD}	0		ns	

FUNCTIONAL DESCRIPTION

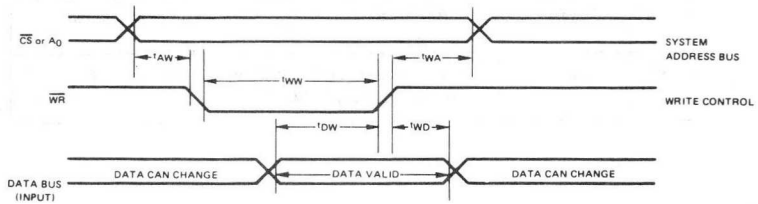
The μPD8041 is a programmable peripheral controller intended for use in master/slave configurations with 8048, 8080A, 8085A, 8086 as well as most other 8-bit and 16-bit microprocessors. The μPD8041 functions as a totally self-sufficient controller with its own program and data memory to unburden the master CPU effectively from I/O handling and peripheral control functions. The μPD8041 is an intelligent peripheral device which connects directly to the master processor bus to perform control tasks which offload main system processing and more efficiently distribute processing functions.

TIMING WAVEFORMS

READ OPERATION – DATA BUS BUFFER REGISTER



WRITE OPERATION – DATA BUS BUFFER REGISTER



MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF
ACCUMULATOR																		
ADD A, = data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•					
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•					
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•					
ADDC A, = data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•					
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•					
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•					
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2						
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1						
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1						
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1						
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1						
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1						
DEC A	(A) ← (A) 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1						
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1						
ORL A, = data	(A) ← (A) OR data	Logical OR or specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2						
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1						
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1						
RL A	(AN + 1) ← (AN) $(A_0) \leftarrow (A_7)$ for N = 0 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1						
RLC A	(AN + 1) ← (AN); N = 0 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•					
RR A	(AN) ← (AN + 1); N = 0 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1						
RRC A	(AN) ← (AN + 1); N = 0 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•					
SWAP A	(A_{4-7}) ↔ (A_{0-3})	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1						
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2						
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1						
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1						
BRANCH																		
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 if (Rr) ≠ 0 (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2						
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2						
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JF0 addr	(PC 0 – 7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JF1 addr	(PC 0 – 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2						
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1						
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JNIBF addr	(PC 0 – 7) ← addr if IBF = (PC) ← (PC) + 2 if IBF = 1	Jump to specified address if input buffer full flag is low.	1 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JOBF	(PC 0 – 7) ← addr if OBF = 1 (PC) ← (PC) + 2 if OBF = 0	Jump to specified address if output buffer full flag is set.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						

MNEMONIC	FUNCTION		INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF
BRANCH (CONT.)																		
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
CONTROL																		
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1						
DIS I		Disable the External Interrupt input	0	0	0	1	0	1	0	1	1	1						
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1						
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 – 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1						
DATA MOVES																		
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2						
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1						
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1						
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1						
MOV Rr, # data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2						
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1						
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1						
MOV @ Rr, # data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2						
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1						
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1						
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1						
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1						
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1						
XCHD A, @ Rr	(A 0 – 3) ⇄ ((Rr)) 0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1						
FLAGS																		
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•					
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•			
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1	1	0	1	1	0	1	0	1	1	1				•		
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•					
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•			
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•		

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF
INPUT/OUTPUT																		
ANL Pp, = data	(Pp) ← (Pp) AND data p = 1 2	Logical and Immediate specified data with designated port (1 or 2)	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2						
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 3) p = 4 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1						
IN A, Pp	(A) ← (Pp); p = 1 2	Input data from designated port (1 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1						
IN A, DBB	(A) ← (DBB)	Input strobed DBB data into Accumulator and clear IBF	0	0	1	0	0	0	1	0	1	1						
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 7 (A 4 7) ← 0	Move contents of designated port (4 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1						
MOVD Pp, A	(Pp) ← A 0 3; p = 4 7	Move contents of Accumulator to designated port (4 7).	0	0	1	1	1	1	p	p	1	1						
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 3) p = 4 7	Logical or contents of Accumulator with designated port (4 7)	1	0	0	0	1	1	p	p	1	1						
ORL Pp, = data	(Pp) ← (Pp) OR data p = 1 2	Logical or Immediate specified data with designated port (1 2)	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2						
OUT DBB, A	(DBB) (A)	Output contents of Accumulator onto DBB and set OBF.	0	0	0	0	0	0	1	0	1	1						
OUTL Pp, A	(Pp) ← (A); p = 1 2	Output contents of Accumulator to designated port (1 2).	0	0	1	1	1	0	p	p	1	1						
REGISTERS																		
DEC Rr (Rr)	(Rr) ← (Rr) 1; r = 0 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1						
INC Rr	(Rr) ← (Rr) +1; r = 0 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1						
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1						
SUBROUTINE																		
CALL addr	((SP)) ← (PC), (PSW 4 7) (SP) ← (SP) + 1 (PC 8 10) ← addr 8 10 (PC 0 7) ← addr 0 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2						
RET	(SP) ← (SP) 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1						
RETR	(SP) ← (SP) 1 (PC) ← ((SP)) (PSW 4 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1						
TIMER/COUNTER																		
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1						
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1						
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1						
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1						
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1						
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1						
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1						
MISCELLANEOUS																		
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1						

Notes
① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

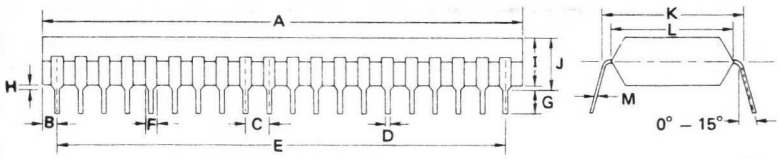
Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator
IBF	Input Buffer Full Flag

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By
OBF	Output Buffer Full
DBB	Data Bus Buffer

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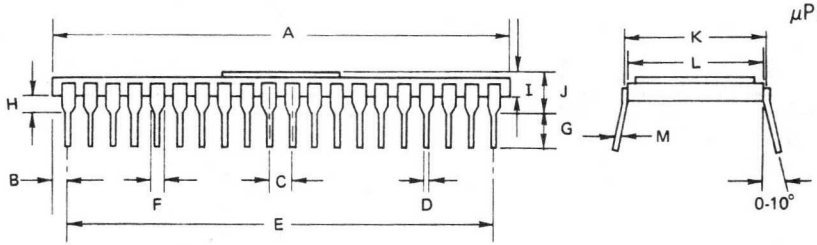
PACKAGE OUTLINE
μPD8041C



(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

μPD8041D



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.03 MAX.
B	1.62 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.0019

UNIVERSAL PROGRAMMABLE PERIPHERAL INTERFACE — 8-BIT MICROCOMPUTER

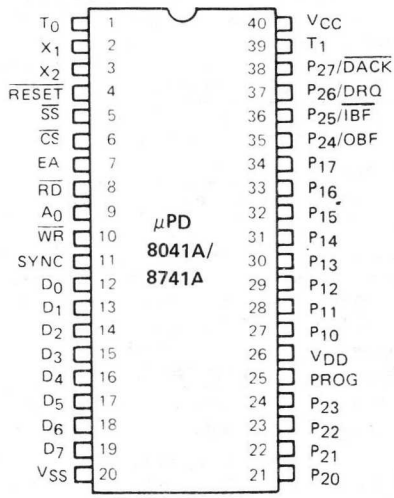
DESCRIPTION

The μPD8041A/8741A is a programmable peripheral interface intended for use in a wide range of microprocessor systems. Functioning as a totally self-sufficient controller, the μPD8041A/8741A contains an 8-bit CPU, 1K x 8 program memory, 64 x 8 data memory, I/O lines, counter/timer, and clock generator in a 40-pin DIP. The bus structure, data registers, and status register enable easy interface to 8048, 8080A or 8085A based systems. The μPD8041A's program memory is factory mask programmed, while the μPD8741A's program memory is UV EPROM to enable user flexibility.

FEATURES

- Fully Compatible with 8048, 8080A, 8085A and 8086 Bus Structure
- 8-Bit CPU with 1K x 8 ROM, 64 x 8 RAM, 8-Bit Timer/Counter, 18 I/O Lines
- 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface
- Interchangeable EPROM and ROM Versions
- Interrupt, DMA or Polled Operation
- Expandable I/O
- 40-Pin Plastic or Ceramic Dip
- Single +5V Supply

PIN CONFIGURATION



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PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1,39	T_0, T_1	Testable input pins using conditional transfer functions JT0, JNT0, JT1, JNT1. T_1 can be made the counter/timer input using the STRT CNT instruction. The PROM programming and verification on the μPD8741A uses T_0.
2	X_1	One side of the crystal input for external oscillator or frequency source.
3	X_2	The other side of the crystal input.
4	$\overline{RESET}$	Active-low input for processor initialization. $\overline{RESET}$ is also used for PROM programming, verification, and power down.
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with SYNC output allows the μPD8741A to "single-step" through each instruction in program memory.
6	$\overline{CS}$	Chip Select input (active-low). $\overline{CS}$ is used to select the appropriate μPD8041A/8741A on a common data bus.
7	EA	External Access input (active-high). A logic "1" at this input commands the μPD8041A/8741A to perform all program memory fetches from external memory.
8	$\overline{RD}$	Read strobe input (active-low). $\overline{RD}$ will pulse low when the master processor reads data and status words from the DATA BUS BUFFER or Status Register.
9	A_0	Address input which the master processor uses to indicate if a byte transfer is a command or data.
10	$\overline{WR}$	Write strobe input (active-low). $\overline{WR}$ will pulse low when the master processor writes data or status words to the DATA BUS BUFFER or Status Register.
11	SYNC	The SYNC output pulses once for each μPD8041A/8741A instruction cycle. It can function as a strobe for external circuitry. SYNC can also be used together with $\overline{SS}$ to "single-step" through each instruction in program memory.
12-19	D_0-D_7 BUS	The 8-bit, bi-directional, tri-state DATA BUS BUFFER lines by which the μPD8041A/8741A interfaces to the 8-bit master system data bus.
20	V_{SS}	Processor's ground potential.
21-24, 35-38	P_{20}-P_{27}	PORT 2 is the second of two 8-bit, quasi-bi-directional I/O ports. P_{20}-P_{23} contain the four most significant bits of the program counter during external memory fetches. P_{20}-P_{23} also serve as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER. P_{24}-P_{27} can be used as port lines or can provide Interrupt Request (IBF and OBF) and DMA handshake lines (DRG and DACK).
25	PROG	Program Pulse. PROG is used in programming the μPD8741A. It is also used as an output strobe for the μPD8243.
26	V_{DD}	V_{DD} is the programming supply voltage for programming the μPD8741A. It is +5V for normal operation of the μPD8041A/8741A. V_{DD} is also the Low Power Standby input for the ROM version.
27-34	P_{10}-P_{17}	PORT 1 is the first of two 8-bit quasi-bi-directional I/O ports.
40	V_{CC}	Primary power supply. V_{CC} must be +5V for programming and operation of the μPD8741A and for the operation of the μPD8041A.

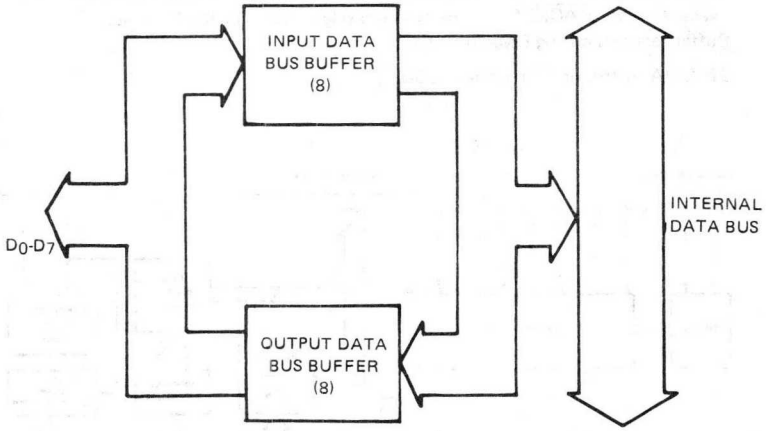
FUNCTIONAL DESCRIPTION

The μPD8041A/8741A is a programmable peripheral controller intended for use in master/slave configurations with 8048, 8080A, 8085A, 8086 -- as well as most other 8-bit and 16-bit microprocessors. The μPD8041A/8741A functions as a totally self-sufficient controller with its own program and data memory to effectively unburden the master CPU from I/O handling and peripheral control functions. The μPD8041A/8741A is an intelligent peripheral device which connects directly to the master processor bus to perform control tasks which off load main system processing and more efficiently distribute processing functions.

μPD8041A/8741A FUNCTIONAL ENHANCEMENTS

The μPD8041A/8741A features several functional enhancements to the earlier μPD8041 part. These enhancements enable easier master/slave interface and increased functionality.

1. Two Data Bus Buffers. Separate Input and Output data bus buffers have been provided to enable smoother data flow to and from master processors.

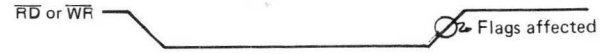


2. 8-Bit Status Register. Four user-definable status bits, ST_4-ST_7, have been added to the status register. ST_4-ST_7 bits are defined with the MOV STS, A instruction which moves accumulator bits 4-7 to bits 4-7 of the status register. ST_0-ST_3 bits are not affected.

ST_7	ST_6	ST_5	ST_4	F_1	F_0	IBF	OBF
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MOV STS, A Instruction OP Code 90H

3. $\overline{RD}$ and $\overline{WR}$ inputs are edge-sensitive. Status bits IBF, OBF, F1 and INT are affected on the trailing edge at $\overline{RD}$ or $\overline{WR}$.



μPD8041A/8741A
FUNCTIONAL
ENHANCEMENTS (CONT.)

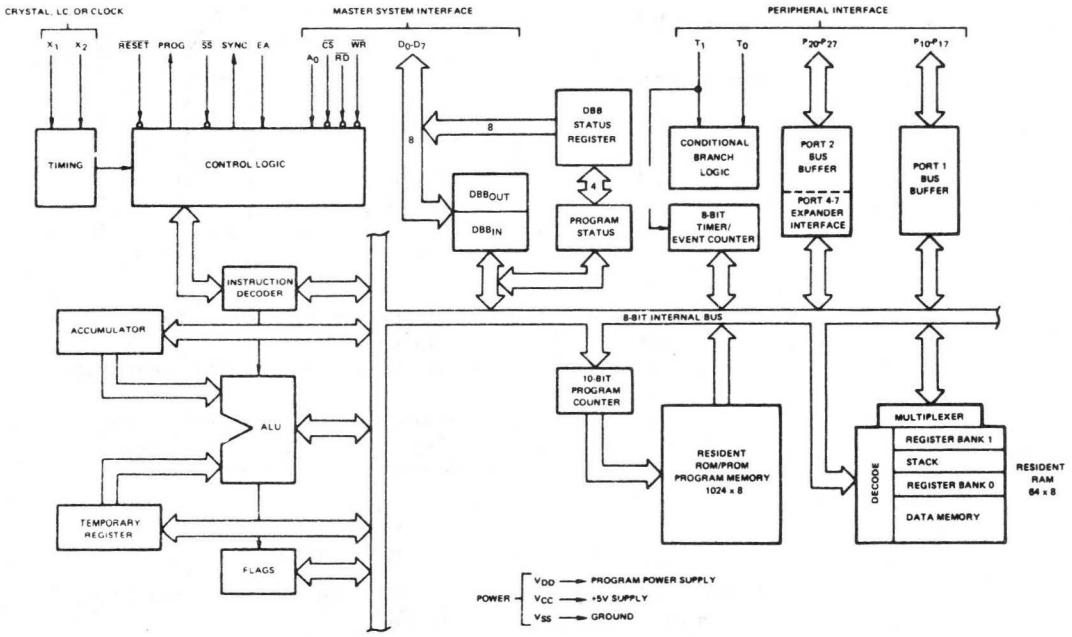
4. P_{24} and P_{25} can be used as either port lines or Buffer Status Flag pins. This feature allows the user to make OBF and IBF status available externally to interrupt the master processor. Upon execution of the EN Flags instruction, P_{24} becomes the OBF pin. When a "1" is written to P_{24}, the OBF pin is enabled and the status of OFB is output. A "0" written to P_{24} disables the OBF pin and the pin remains low. This pin indicates valid data is available from the μPD8041A/8741A. EN Flags instruction execution also enables P_{25} indicate that the μPD8041A/8741A is ready to accept data. A "1" written to P_{25} enables the IBF pin and the status of IBF is available on P25. A "0" written to P_{25} disables the IBF pin.

   EN Flags Instruction Op code – F5H.

5. P_{26} and P_{27} can be used as either port lines or DMA handshake lines to allow DMA interface. The EN DMA instruction enables P_{26} and P_{27} to be used as DRQ (DMA Request) and $\overline{DACK}$ (DMA acknowledge) respectively. When a "1" is written to P_{26}, DRQ is activated and a DMA request is issued. Deactivation of DRQ is accomplished by the execution of the EN DMA instruction, $\overline{DACK}$ anded with $\overline{RD}$, or $\overline{DACK}$ anded with $\overline{WR}$. When EM DMA has been executed, P_{27} ($\overline{DACK}$) functions as a chip select input for the Data Bus Buffer registers during DMA transfers.

   EN DMA Instruction Op Code – E5H.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +125°C
Voltage on Any Pin	−0.5 to +7 Volts ①
Power Dissipation	1.5 Watt

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: ① With respect to ground.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{DD} = V_{CC} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage (All except X_1 and X_2)	V_{IL}	−0.5		+0.8	V	
Input Low Voltage (X_1 and X_2, $\overline{RESET}$)	V_{IL1}	−0.5		0.6	V	
Input High Voltage (All except X_1, X_2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage (X_1, X_2, $\overline{RESET}$)	V_{IH1}	3.8		V_{CC}	V	
Output Low Voltage (D_0-D_7, SYNC)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (All other outputs except PROG)	V_{OL1}			0.45	V	I_{OL} = 1.0 mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	I_{OL} = 1.0 mA
Output High Voltage (D_0-D_7)	V_{OH}	2.4			V	I_{OH} = −400 μA
Output High Voltage (All other outputs)	V_{OH1}	2.4			V	I_{OH} = −50 μA
Input Leakage Current (T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, EA, A_0)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Output Leakage Current (D_0-D_7; High Z State)	I_{OL}			±10	μA	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$
V_{DD} Supply Current	I_{DD}			15	mA	
Total Supply Current	$I_{CC} + I_{DD}$			125	mA	
Low Input Source Current (P_{10}-P_{17}; P_{20}-P_{27})	I_{LI}			0.5	mA	V_{IL} = 0.8V
Low Input Source Current (SS; $\overline{RESET}$)	I_{LI1}			0.2	mA	V_{IL} = 0.8V

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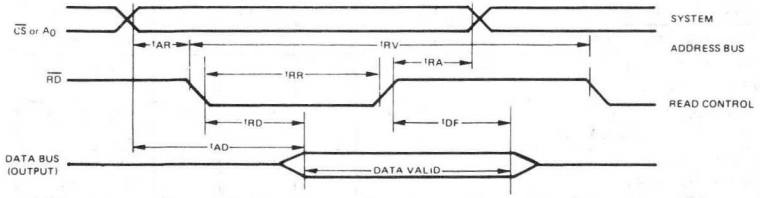
AC CHARACTERISTICS

T_a = 0°C to +70°C; $V_{DD} = V_{CC}$ = +5V ± 10%; V_{SS} = 0V

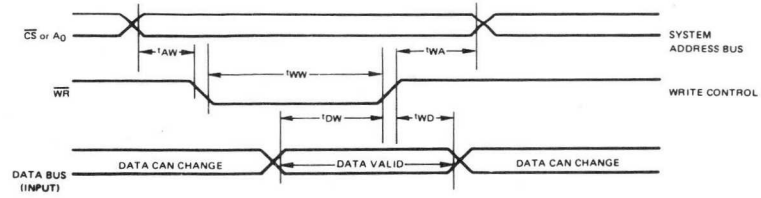
PARAMETER	SYMBOL	LIMITS μPD8041A MIN	LIMITS μPD8041A MAX	LIMITS μPD8741A MIN	LIMITS μPD8741A MAX	UNITS	TEST CONDITIONS
DBB READ							
$\overline{CS}$, A_0 Setup to $\overline{RD}$ ↓	t_{AR}	0		60		ns	
$\overline{CS}$, A_0 Hold after $\overline{RD}$ ↑	t_{RA}	0		30		ns	
$\overline{RD}$ Pulse Width	t_{RR}	250		300	2 x t_{CY}	ns	t_{CY} = 2.5 μs
$\overline{CS}$, A_0 to Data Out Delay	t_{AD}		225		370	ns	C_L = 150 pF
$\overline{RD}$ ↓ to Data Out Delay	t_{RD}		225		200	ns	C_L = 150 pF
$\overline{RD}$ ↑ to Data Float Delay	t_{DF}		100		140	ns	
Cycle Time	t_{CY}	2.5	15	2.5	15	μs	6 MHz Crystal
DBB WRITE							
$\overline{CS}$, A_0 Setup to $\overline{WR}$ ↓	t_{AW}	0		60		ns	
$\overline{CS}$, A_0 Hold after $\overline{WR}$ ↑	t_{WA}	0		30		ns	
$\overline{WR}$ Pulse Width	t_{WW}	250		300	2 x t_{CY}	ns	t_{CY} = 2.5 μs
Data Setup to $\overline{WR}$ ↑	t_{DW}	150		250		ns	
Data Hold after $\overline{WR}$ ↑	t_{WD}	0		30		ns	

TIMING WAVEFORMS

READ OPERATION – DATA BUS BUFFER REGISTER



WRITE OPERATION – DATA BUS BUFFER REGISTER



INSTRUCTION SET

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF	ST_{4-7}
ACCUMULATOR																			
ADD A, = data	(A) ← (A) + data	Add immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•						
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•						
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•						
ADDC A, = data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•						
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•						
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•						
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2							
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1							
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 1	Logical and Indirect the contents of data memory with Accumulator	0	1	0	1	0	0	0	r	1	1							
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1							
CLR A	(A) ← 0	CLEAR the contents of the Accumulator	0	0	1	0	0	1	1	1	1	1							
DA A		DECIMAL ADJUST the contents of the Accumulator	0	1	0	1	0	1	1	1	1	1	•						
DEC A	(A) ← (A) 1	DECREMENT by 1 the accumulator's contents	0	0	0	0	0	1	1	1	1	1							
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents	0	0	0	1	0	1	1	1	1	1							
ORL A, = data	(A) ← (A) OR data	Logical OR or specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2							
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1							
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 1	Logical OR Indirect the contents of data memory location with Accumulator	0	1	0	0	0	0	0	r	1	1							
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 6	Rotate Accumulator left by 1 bit without carry	1	1	1	0	0	1	1	1	1	1							
RLC A	(AN + 1) ← (AN), N = 0 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1 bit through carry	1	1	1	1	0	1	1	1	1	1	•						
RR A	(AN) ← (AN + 1), N = 0 6 (A_7) ← (A_0)	Rotate Accumulator right by 1 bit without carry	0	1	1	1	0	1	1	1	1	1							
RRC A	(AN) ← (AN + 1), N = 0 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1 bit through carry	0	1	1	0	0	1	1	1	1	1	•						
SWAP A	(A_{4-7}) ↔ (A_{0-3})	Swap the 2 4 bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1							
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2							
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1							
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator	1	1	0	1	0	0	0	r	1	1							
BRANCH																			
DJNZ Rr, addr	(Rr) ← (Rr) 1, r = 0 – 7 If (Rr) ≠ 0 (PC 0 7) ← addr	Decrement the specified register and test contents	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2							
JBb addr	(PC 0 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2							
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JF0 addr	(PC 0 7) ← addr if F0 = 1 (PC) ←)(PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JF1 addr	(PC 0 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JMP addr	(PC 8 10) ← addr 8 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2							
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1							
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JNIBF addr	(PC 0 – 7) ← addr if IBF = (PC) ← (PC) + 2 if IBF = 1	Jump to specified address if input buffer full flag is low.	1 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JOBF	(PC 0 – 7) ← addr if OBF = 1 (PC) ← (PC) + 2 if OBF = 0	Jump to specified address if output buffer full flag is set.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							

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INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION		INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF	ST_{4-7}
BRANCH (CONT.)																			
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
CONTROL																			
EN I		Enable the External Interrupt Input	0	0	0	0	0	1	0	1	1	1							
DIS I		Disable the External Interrupt Input	0	0	0	1	0	1	0	1	1	1							
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1							
SEL RB1	(BS) ← 1	Select Bank 0 (locations 24 – 31) of Data Memory	1	1	0	1	0	1	0	1	1	1							
EN DMA		Enable DMA Handshake	1	1	1	1	0	1	0	1	1	1							
EN FLAGS		Enable Interrupt to Master Device	1	1	1	0	0	1	0	1	1	1							
DATA MOVES																			
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2							
MOV A, Rr	(A) ← (Rr), r = 0 – 7	Move the contents of the designated registers into the Accumulator	1	1	1	1	1	r	r	r	1	1							
MOV A, @ Rr	(A) ← ((Rr)), r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator	1	1	1	1	0	0	0	r	1	1							
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator	1	1	0	0	0	1	1	1	1	1							
MOV Rr, # data	(Rr) ← data, r = 0 – 7	Move Immediate the specified data into the designated register	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2							
MOV Rr, A	(Rr) ← (A), r = 0 – 7	Move Accumulator Contents into the designated register	1	0	1	0	1	r	r	r	1	1							
MOV @ Rr, A	((Rr)) ← (A), r = 0 – 1	Move Indirect Accumulator Contents into data memory location	1	0	1	0	0	0	0	r	1	1							
MOV @ Rr, # data	((Rr)) ← data, r = 0 – 1	Move Immediate the specified data into data memory	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2							
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word	1	1	0	1	0	1	1	1	1	1							
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator	1	0	1	0	0	0	1	1	2	1							
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator	1	1	1	0	0	0	1	1	2	1							
XCH A, Rr	(A) ⇄ (Rr), r = 0 – 7	Exchange the Accumulator and designated register's contents	0	0	1	0	1	r	r	r	1	1							
XCH A, @ Rr	(A) ⇄ ((Rr)), r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory	0	0	1	0	0	0	0	r	1	1							
XCHD A, @ Rr	(A 0 – 3) ⇄ ((Rr)) 0 – 3)), r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory	0	0	1	1	0	0	0	r	1	1							
FLAGS																			
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•						
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0	1	0	0	1	0	1	0	1	1	1			•				
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1	1	0	1	1	0	1	0	1	1	1				•			
CLR C	(C) ← 0	Clear content of carry bit to 0	1	0	0	1	0	1	1	1	1	1	•						
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•				
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0	1	0	1	0	0	1	0	1	1	1				•			
MOV STS, A	ST_4-ST_7 ← A_4-A_7	Move high order 4 bits of Accumulator into status register bits 4-7	1	0	0	1	0	0	0	0	1	1							•

INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF	ST4-7
INPUT/OUTPUT																			
ANL Pp, #data	(Pp) ← (Pp) AND data p = 1 2	Logical and Immediate specified data with designated port (1 or 2)	1	0	0	1	1	0	p	p	2	2							
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 3) p = 4 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1							
IN A, Pp	(A) ← (Pp), p = 1 2	Input data from designated port (1 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1							
IN A, DBB	(A) ← (DBB)	Input strobed DBB data into Accumulator and clear IBF	0	0	1	0	0	0	1	0	1	1					•		
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 - 7 (A 4 7) ← 0	Move contents of designated port (4 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1							
MOVD Pp, A	(Pp) ← A 0 - 3; p = 4 7	Move contents of Accumulator to designated port (4 7).	0	0	1	1	1	1	p	p	1	1							
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 3) p = 4 7	Logical or contents of Accumulator with designated port (4 7).	1	0	0	0	1	1	p	p	1	1							
ORL Pp, #data	(Pp) ← (Pp) OR data p = 1 2	Logical or Immediate specified data with designated port (1 2)	1	0	0	0	1	0	p	p	2	2							
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
OUT DBB, A	(DBB) (A)	Output contents of Accumulator onto DBB and set OBF.	0	0	0	0	0	0	1	0	1	1						•	
OUTL Pp, A	(Pp) ← (A), p = 1 2	Output contents of Accumulator to designated port (1 2).	0	0	1	1	1	0	p	p	1	1							
REGISTERS																			
DEC Rr (Rr)	(Rr) ← (Rr) 1; r = 0 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1							
INC Rr	(Rr) ← (Rr) +1; r = 0 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1							
INC @ Rr	((Rr)) ← ((Rr)) + 1, r = 0 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1							
SUBROUTINE																			
CALL addr	((SP)) ← (PC), (PSW 4 7) (SP) ← (SP) + 1 (PC 8 10) ← addr 8 10 (PC 0 7) ← addr 0 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10}	a_9	a_8	1	0	1	0	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
RET	(SP) ← (SP) 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1							
RETR	(SP) ← (SP) 1 (PC) ← ((SP)) (PSW 4 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1							
TIMER/COUNTER																			
EN TCNTI		Enable Internal Interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1							
DIS TCNTI		Disable Internal Interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1							
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1							
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1							
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1							
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1							
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1							
MISCELLANEOUS																			
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1							

Notes
① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

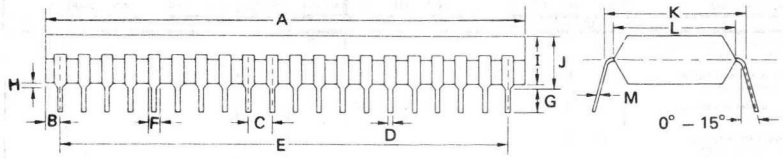
Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator
IBF	Input Buffer Full Flag

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By
OBF	Output Buffer Full
DBB	Data Bus Buffer

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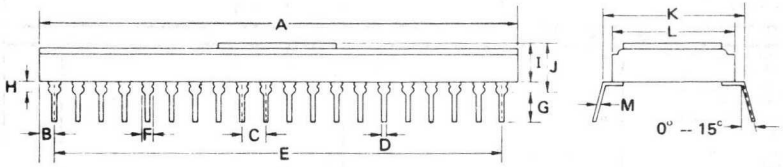
PACKAGE OUTLINE
μPD8041AC
μPD8741AC



(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

μPD8041AD
μPD8741AD



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

μPD8048 FAMILY OF SINGLE CHIP 8-BIT MICROCOMPUTERS

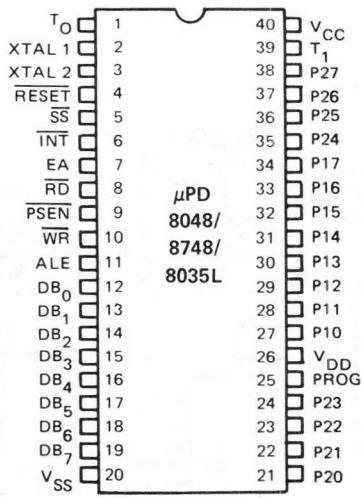
DESCRIPTION

The μPD8048 family of single chip **8-bit microcomputers** is comprised of the μPD8048, μPD8748 and μPD8035L. The processors in this family differ only in their internal program memory options: The μPD8048 with 1K x 8 bytes of mask ROM, the μPD8748 with 1K x 8 bytes of UV erasable EPROM and the μPD8035L with external memory.

FEATURES

- Fully Compatible With Industry Standard 8048/8748/8035
- NMOS Silicon Gate Technology Requiring a Single +5V Supply
- 2.5 μs Cycle Time. All Instruction 1 or 2 Bytes
- Interval Timer/Event Counter
- 64 x 8 Byte RAM Data Memory
- Single Level Interrupt
- 96 Instructions: 70% Single Byte
- 27 I/O Lines
- Internal Clock Generator
- 8 Level Stack
- Compatible With 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40 Pin Packages

PIN CONFIGURATION



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FUNCTIONAL DESCRIPTION

The NEC μPD8048, μPD8748 and μPD8035L are single component, 8-bit, parallel microprocessors using N-channel silicon gate MOS technology. The μPD8048/8748/8035L efficiently function in control as well as arithmetic applications. The flexibility of the instruction set allows for the direct set and reset of individual data bits within the accumulator and the I/O port structure. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

The μPD8048/8748/8035L instruction set is comprised of 1 and 2 byte instructions with over 70% single-byte and requiring only 1 or 2 cycles per instruction with over 50% single-cycle.

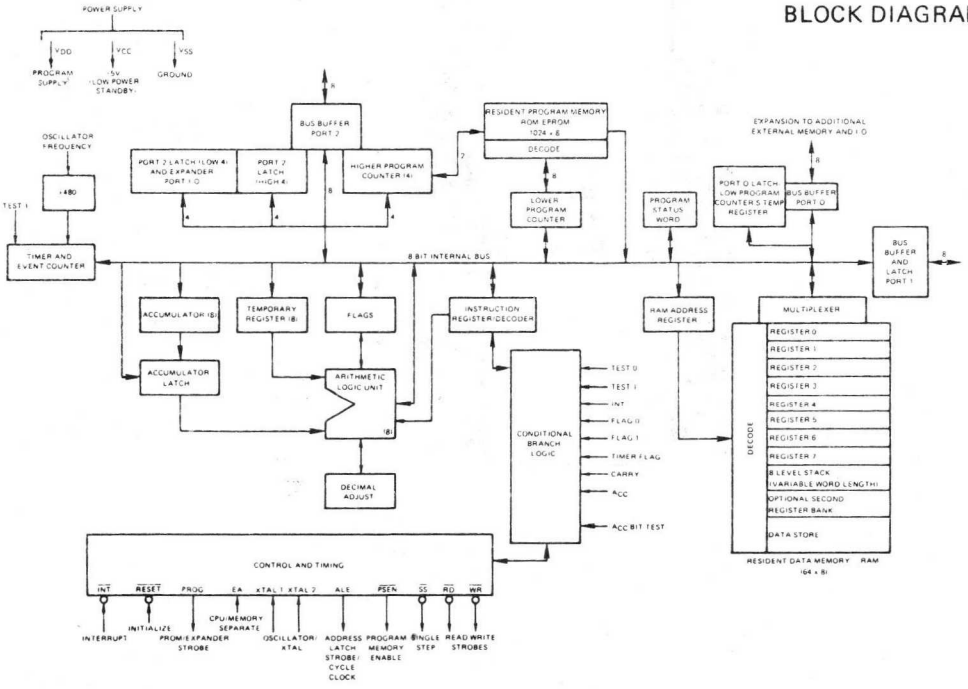
The μPD8048 series of microprocessors will function as stand alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8048 contains the following functions usually found in external peripheral devices: 1024 x 8 bits of ROM program memory; 64 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

The μPD8748 differs from the μPD8048 only in its 1024 x 8-bit UV erasable EPROM program memory instead of the 1024 x 8-bit ROM memory. It is useful in preproduction or prototype applications where the software design has not yet been finalized or in system designs whose quantities do not require a mask ROM.

The μPD8035L is intended for applications using external program memory only. It contains all the features of the μPD8048 except the 1024 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENT0 CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non TTL compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{RESET}$	Active low input for processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe output (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active high). Occurring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12 – 19	$D_0 - D_7$ BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the $D_0 - D_7$ BUS can be latched in a static mode. During an external memory fetch, the $D_0 - D_7$ BUS holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the $D_0 - D_7$ BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21 – 24, 35 – 38	$P_{20} - P_{27}$: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in $P_{20} - P_{23}$. Bits $P_{20} - P_{23}$ are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	Program Pulse. A +25V pulse applied to this input is used for programming the μPD8748. PROG is also used as an output strobe for the μPD8243.
26	V_{DD}	Programming Power Supply. V_{DD} must be set to +25V for programming the μPD8748, and to +5V for the ROM and PROM versions for normal operation. V_{DD} functions as the Low Power Standby input for the μPD8048.
27 – 34	$P_{10} - P_{17}$: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power Supply. V_{CC} must be +5V for programming and operation of the μPD8748, and for operation of the μPD8035L and μPD8048.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +125°C
Voltage on Any Pin	− 0.5 to +7 Volts ①
Power Dissipation	1.5 W

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −0°C to +70°C; V_{CC} = V_{DD} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	−0.5		0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}	3.8		V_{CC}	V	
Output Low Voltage (BUS)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage ($\overline{RD}$, $\overline{WR}$, PSEN, ALE)	V_{OL1}			0.45	V	I_{OL} = 1.8 mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	I_{OL} = 1.0 mA
Output Low Voltage (All Other Outputs)	V_{OL3}			0.45	V	I_{OL} = 1.6 mA
Output High Voltage (BUS)	V_{OH}	2.4			V	I_{OH} = −400 μA
Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH1}	2.4			V	I_{OH} = −100 μA
Output High Voltage (All Other Outputs)	V_{OH2}	2.4			V	I_{OH} = −40 μA
Input Leakage Current (T_1, INT)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Input Leakage Current (P_{10}-P_{17}, P_{20}-P_{27}, EA, $\overline{SS}$)	I_{IL1}			−500	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V
Output Leakage Current (BUS, T_0 — High Impedance State)	I_{OL}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V
Power Down Supply Current	I_{DD}		7	15	mA	T_a = 25°C
Total Supply Current	$I_{DD} + I_{CC}$		60	135	mA	T_a = 25°C

DC CHARACTERISTICS PROGRAMMING THE μPD8748

T_a = 25°C ± 5°C; V_{CC} = +5V ± 10%; V_{DD} = +25V ± 1V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{DD} Program Voltage High-Level	V_{DDH}	24.0		26.0	V	
V_{DD} Voltage Low-Level	V_{DDL}	4.75		5.25	V	
PROG Voltage High-Level	V_{PH}	21.5		24.5	V	
PROG Voltage Low-Level	V_{PL}			0.2	V	
EA Program or Verify Voltage High-Level	V_{EAH}	21.5		24.5	V	
EA Voltage Low-Level	V_{EAL}			5.25	V	
V_{DD} High Voltage Supply Current	I_{DD}			30.0	mA	
PROG High Voltage Supply Current	I_{PROG}			16.0	mA	
EA High Voltage Supply Current	I_{EA}			1.0	mA	

READ, WRITE AND INSTRUCTION FETCH – EXTERNAL DATA AND PROGRAM MEMORY

AC CHARACTERISTICS $T_a = 0°C$ to $+70°C$; $V_{CC} = V_{DD} = +5V \pm 10\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST ① CONDITIONS
ALE Pulse Width	t_{LL}	400			ns	
Address Setup before ALE	t_{AL}	120			ns	
Address Hold from ALE	t_{LA}	80			ns	
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}	700			ns	
Data Setup before $\overline{WR}$	t_{DW}	500			ns	
Data Hold after $\overline{WR}$	t_{WD}	120			ns	C_L = 20 pF
Cycle Time	t_{CY}	2.5		15.0	μs	6 MHz XTAL
Data Hold	t_{DR}	0		200	ns	
$\overline{PSEN}$, $\overline{RD}$ to Data In	t_{RD}			500	ns	
Address Setup before $\overline{WR}$	t_{AW}	230			ns	
Address Setup before Data In	t_{AD}			950	ns	
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	0			ns	
Control Pulse to ALE	t_{CA}	10			ns	

Notes: ① For Control Outputs: C_L = 80 pF
For Bus Outputs: C_L = 150 pF
t_{CY} = 2.5 μs

PORT 2 TIMING

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Port Control Setup before Falling Edge of $\overline{PROG}$	t_{CP}	110			ns	
Port Control Hold after Falling Edge of $\overline{PROG}$	t_{PC}	100			ns	
$\overline{PROG}$ to Time P2 Input must be Valid	t_{PR}			810	ns	
Output Data Setup Time	t_{DP}	250			ns	
Output Data Hold Time	t_{PD}	65			ns	
Input Data Hold Time	t_{PF}	0		150	ns	
$\overline{PROG}$ Pulse Width	t_{PP}	1200			ns	
Port 2 I/O Data Setup	t_{PL}	350			ns	
Port 2 I/O Data Hold	t_{LP}	150			ns	

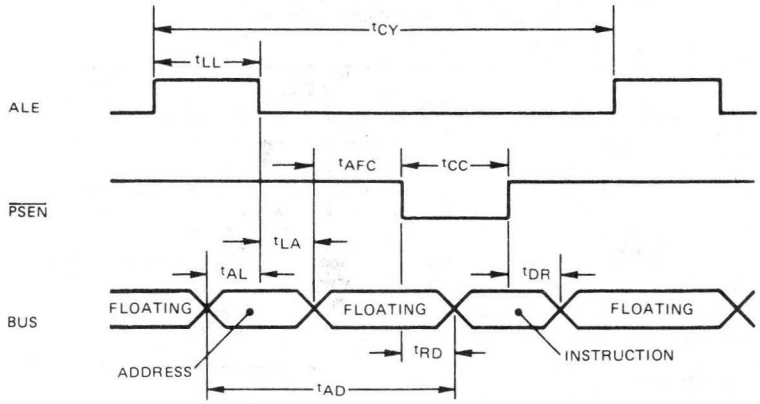
PROGRAMMING SPECIFICATIONS – μPD8748

$T_a = 25°C \pm 5°C$; $V_{CC} = +5V \pm 10\%$; $V_{DD} = +25V \pm 1V$

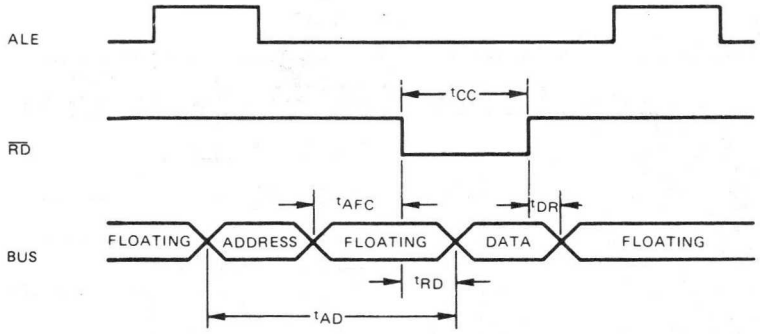
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Setup Time before $\overline{RESET}$ ↑	t_{AW}	4 t_{CY}				
Address Hold Time after $\overline{RESET}$ ↑	t_{WA}	4 t_{CY}				
Data In Setup Time before $\overline{PROG}$ ↑	t_{DW}	4 t_{CY}				
Data In Hold Time after $\overline{PROG}$ ↓	t_{WD}	4 t_{CY}				
RESET Hold Time to VERIFY	t_{PH}	4 t_{CY}				
V_{DD}	t_{VDDW}	4 t_{CY}				
V_{DD} Hold Time after $\overline{PROG}$ ↓	t_{VDDH}	0				
Program Pulse Width	t_{PW}	50		60	ms	
Test 0 Setup Time before Program Mode	t_{TW}	4 t_{CY}				
Test 0 Hold Time after Program Mode	t_{WT}	4 t_{CY}				
Test 0 to Data Out Delay	t_{DO}			4 t_{CY}		
$\overline{RESET}$ Pulse Width to Latch Address	t_{WW}	4 t_{CY}				
V_{DD} and $\overline{PROG}$ Rise and Fall Times	t_r,t_f	0.5		2.0	μs	
Processor Operation Cycle Time	t_{CY}	5.0			μs	
$\overline{RESET}$ Setup Time before EA ↑	t_{RE}	4 t_{CY}				

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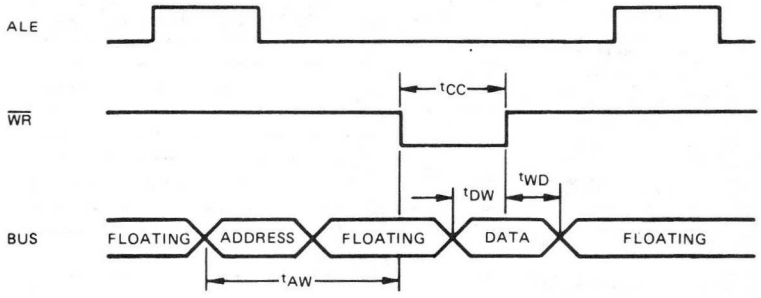
TIMING WAVEFORMS



INSTRUCTION FETCH FROM EXTERNAL MEMORY

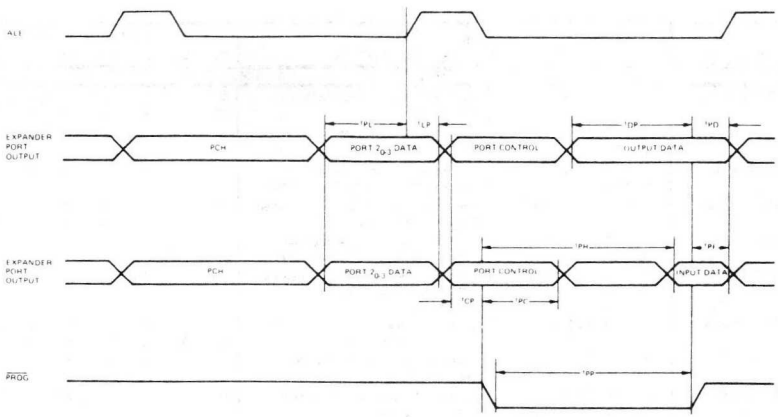


READ FROM EXTERNAL DATA MEMORY

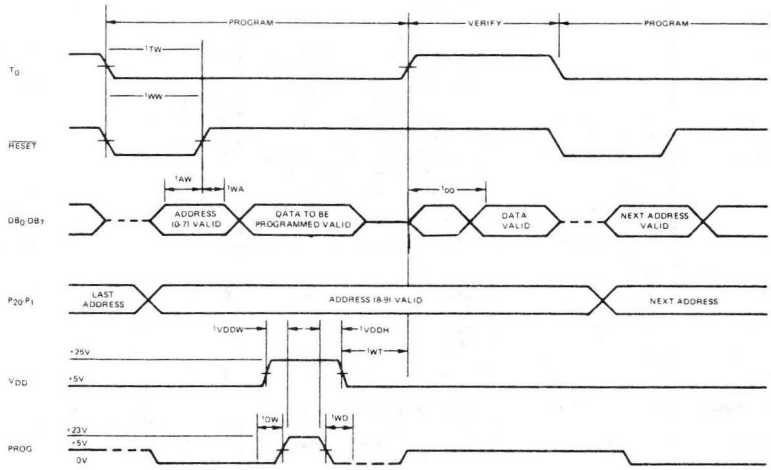


WRITE TO EXTERNAL MEMORY

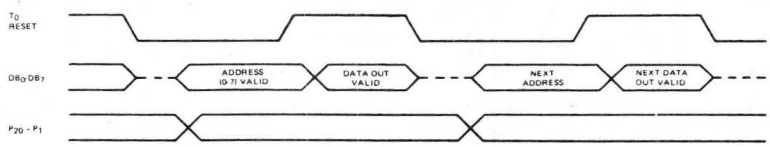
TIMING WAVEFORMS (CONT.)



PORT 2 TIMING



PROGRAM/VERIFY TIMING
(μPD8748 ONLY)



VERIFY MODE TIMING
(μPD8048/8748 ONLY)

Notes ① Conditions $\overline{CS}$: TTL Logic "1", A0: TTL Logic "0" must be met. Use 10K resistor to V_{CC} for $\overline{CS}$, and 10K resistor to V_{SS} for A0.

② t_{CY}: 5 μs can be achieved using a 3 MHz frequency source (LC, XTAL or external) at the XTAL 1 and XTAL 2 inputs.

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
ACCUMULATOR																
ADD A, # data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 – 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, # data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 – 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 – 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, # data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 – 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 – 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) – 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 – 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 – 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 – 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_{4-7}) ↔ (A_0 – 3)	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
BRANCH																
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 If (Rr) ≠ 0: (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC 0 – 7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC 0 – 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2*	1				
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 – 7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
BRANCH (CONT.)																
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
CONTROL																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 – 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 – 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 – 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
DATA MOVES																
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, # data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, # data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0 – 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ↔ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ↔ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ↔ ((Rr)) 0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
FLAGS																
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1
INPUT/OUTPUT																
ANL BUS, = data	(BUS) ← (BUS) AND data	Logical and Immediate-specified data with contents of BUS.	1	0	0	1	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANL Pp, = data	(Pp) ← (Pp) AND data p = 1, 2	Logical and Immediate specified data with designated port (1 or 2)	1	0	0	1	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANLD Pp, A	(Pp) ← (Pp) AND (A 0–3) p = 4–7	Logical and contents of Accumulator with designated port (4–7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1, 2	Input data from designated port (1, 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0–3) ← (Pp); p = 4–7 (A 4–7) ← 0	Move contents of designated port (4–7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0–3; p = 4–7	Move contents of Accumulator to designated port (4–7).	0	0	1	1	1	1	p	p	1	1				
ORL BUS, = data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS.	1	0	0	0	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ORLD Pp, A	(Pp) ← (Pp) OR (A 0–3) p = 4–7	Logical or contents of Accumulator with designated port (4–7).	1	0	0	0	1	1	p	p	1	1				
ORL Pp, = data	(Pp) ← (Pp) OR data p = 1, 2	Logical or Immediate specified data with designated port (1, 2)	1	0	0	0	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto BUS.	0	0	0	0	0	0	1	0	1	1				
OUTL Pp, A	(Pp) ← (A); p = 1, 2	Output contents of Accumulator to designated port (1, 2).	0	0	1	1	1	0	p	p	1	1				
REGISTERS																
DEC Rr (Rr)	(Rr) ← (Rr) −1; r = 0–7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) +1; r = 0–7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @Ri	((Ri)) ← ((Ri)) + 1; r = 0, 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
SUBROUTINE																
CALL addr	((SP)) ← (PC), (PSW 4–7) (SP) ← (SP) + 1 (PC 8–10) ← addr 8–10 (PC 0–7) ← addr 0–7 (PC 11) ← DBF	Call designated Subroutine.	a_{10}	a_9	a_8	1	0	1	0	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
RET	(SP) ← (SP) −1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) −1 (PC) ← ((SP)) (PSW 4–7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
TIMER/COUNTER																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1				
MISCELLANEOUS																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

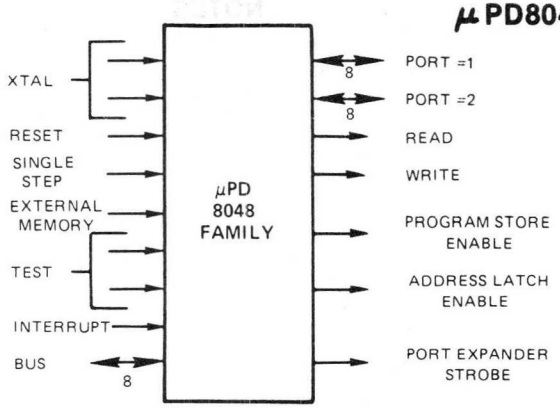
Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions:

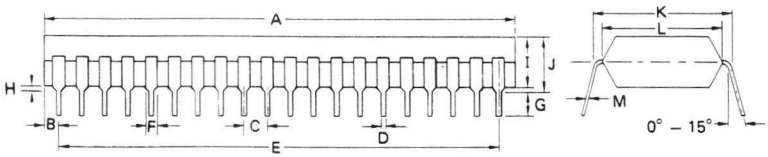
SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By

LOGIC SYMBOL



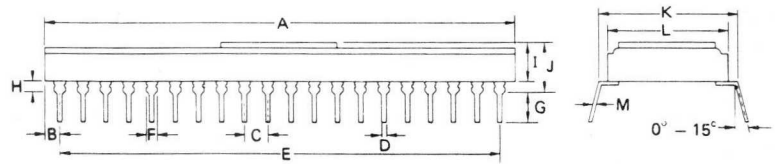
PACKAGE OUTLINES
μPD8048C
μPD8035LC



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{0.05}$	$0.010^{+0.004}_{0.002}$

μPD8048D
μPD8748D
μPD8035LD



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5	2.03
B	1.62	0.06
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26	1.9
F	1.02	0.04
G	3.2	0.13
H	1.0	0.04
I	3.5	0.14
J	4.5	0.18
K	15.24	0.6
L	14.93	0.59
M	0.25 ± 0.05	0.01 ± 0.0019

NEC
μPD80C48
μPD80C35
PRELIMINARY

CMOS SINGLE CHIP 8-BIT MICROCOMPUTER

DESCRIPTION

The NEC μPD80C48 is a true stand alone 8-bit microcomputer fabricated with CMOS technology. The μPD80C48 contains all the functional blocks – 1K bytes ROM, 64 bytes RAM, 27 I/O lines, on-chip 8-bit Timer/Event counter, on-chip clock generator-to enable its use in stand alone applications. For designs requiring extra capability the μPD80C48 can be expanded using industry standard μPD8080A/ μPD8085A peripherals and memory products. The μPD80C35 differs from the μPD80C48 only in that the μPD80C35 contains no internal program memory (ROM).

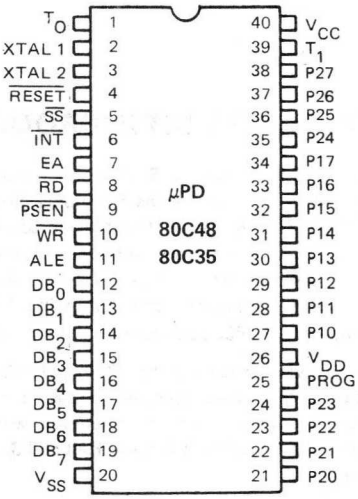
Compatible with the industry standard 8048, 8748, and 8035, the CMOS fabricated μPD80C48 provides significant power consumption savings in applications requiring low power and portability. In addition to the inherent power savings gained through CMOS technology, the NEC μPD80C48 features Halt and Stop modes to further minimize power drain.

FEATURES

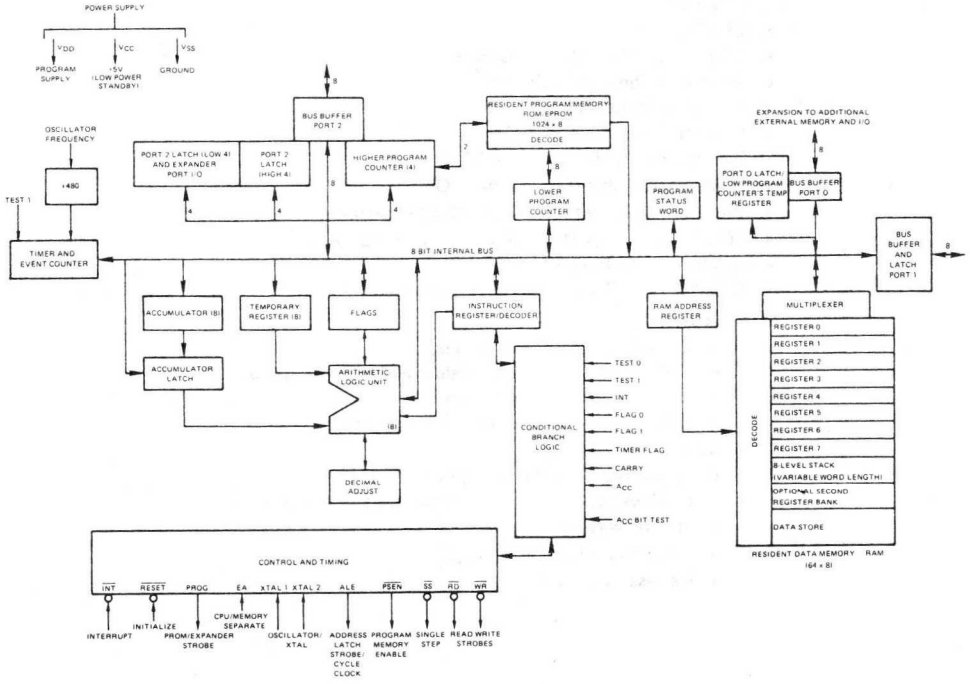
- 8-Bit CPU, ROM, RAM, I/O in a Single Package
- Hardware/Software Compatible with Industry Standard 8048, 8748, 8035 Products
- 1K x 8 ROM
- 64 x 8 RAM
- 27 I/O Lines
- 2.5 μs Cycle Time (6 MHz Crystal)
- All Instructions 1 or 2 Cycles
- 97 Instructions: 70% Single Byte
- Internal Timer/Event Counter
- Two Interrupts (External and Timer)
- Easily Expandable Memory and I/O
- Bus Compatible with 8080A/8085A Peripherals
- CMOS Technology Requiring a Single +5V Supply
- Available in 40-Pin DIP
- Effective Low Power Standby Functions
  - Halt Mode
    - 2 mA Typical Supply Current
    - Maintains Internal Logic Values and Control Status
    - Initiated by Halt Instruction
    - Released by External Interrupt or Reset
  - Stop Mode
    - 20 μA Maximum Supply Current
    - Disables Internal Clock Generation and Internal Logic
    - Maintains RAM
    - Initiated via Hardware (V_{DD})
    - Released via Reset

7

PIN CONFIGURATION



BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non TTL compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{RESET}$	Active low input for processor initialization. $\overline{RESET}$ is also used for Halt/Stop Mode release (non TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe output (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	**Address Latch Enable output (active high). Occurring once** each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12 – 19	$D_0 - D_7$ BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the $D_0 - D_7$ BUS can be latched in a static mode. During an external memory fetch, the $D_0 - D_7$ BUS holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the $D_0 - D_7$ BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21 – 24, 35 – 38	$P_{20} - P_{27}$: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in $P_{20} - P_{23}$. Bits $P_{20} - P_{23}$ are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	PROG is used as an output strobe for the μPD8243.
26	V_{DD}	Power Supply; +5V during normal operation for ROM. V_{DD} is also used in the stop mode. By forcing V_{DD} low during a reset, processor enters the stop mode.
27 – 34	$P_{10} - P_{17}$: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power Supply. V_{CC} must be +5V for operation of the μPD80C48 and μPD80C35.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . -40°C to +85°C
Storage Temperature (Ceramic Package) . . . . . -65°C to +150°C
Storage Temperature (Plastic Package) . . . . . -65°C to +125°C
Voltage on Any Pin . . . . . V_{CC} - 0.3V to V_{CC} + 0.3V
Supply Voltage . . . . . V_{SS} - 0.3 to +10V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = -40°C to +85°C; V_{CC} = V_{DD} = +5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	-0.3		0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2, RESET)	V_{IH}	V_{CC}-2		V_{CC}	V	
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}	V_{CC}-1		V_{CC}	V	
Output Low Voltage (BUS, RD, WR, PSEN, ALE)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (All Other Outputs Except PROG)	V_{OL1}			0.45	V	I_{OL} = 1.6 mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	
Output High Voltage (BUS, RD, WR, PSEN, ALE)	V_{OH}	2.4			V	I_{OH} = -100 μA
Output High Voltage (All Other Outputs)	V_{OH1}	2.4			V	I_{OH} = -50 μA
Input Current (Port 1, Port 2)	I_{ILP}	-160			μA	$V_{IN} \leq V_{IL}$
Input Current ($\overline{SS}$, $\overline{RESET}$)	I_{ILC}	-40			μA	$V_{IN} \leq V_{IL}$
Input Leakage Current (T_1, EA, INT)	I_{IL}		±1		μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Output Leakage Current (BUS, T_0 – High Impedance State)	I_{OL}		±1		μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Total Supply Current	$I_{DD} + I_{CC}$			10	mA	T_a = 25°C 6 MHz
Halt Power Supply Current	I_{CC}		2		mA	6 MHz
Stop Mode Supply Current	I_{CC}			20	μA	6 MHz

AC CHARACTERISTICS

READ, WRITE AND INSTRUCTION FETCH – EXTERNAL DATA AND PROGRAM MEMORY

T_a = -40°C to +85°C; V_{CC} = V_{DD} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST ① CONDITIONS
ALE Pulse Width	t_{LL}	400			ns	
Address Setup before ALE	t_{AL}	150			ns	
Address Hold from ALE	t_{LA}	80			ns	
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}	900			ns	
Data Setup before $\overline{WR}$	t_{DW}	500			ns	
Data Hold after $\overline{WR}$	t_{WD}	120			ns	C_L = 20 pF
Cycle Time	t_{CY}	2.5		15.0	μs	6 MHz XTAL
Data Hold	t_{DR}	0		200	ns	
$\overline{PSEN}$, $\overline{RD}$ to Data In	t_{RD}			500	ns	
Address Setup before $\overline{WR}$	t_{AW}	230			ns	
Address Setup before Data In	t_{AD}			950	ns	
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	0			ns	

Notes: ① For Control Outputs: C_L = 80 pF
For Bus Outputs: C_L = 150 pF

AC CHARACTERISTICS (CONT.)

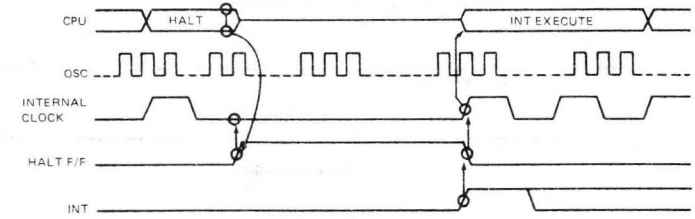
PORT 2 TIMING

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%

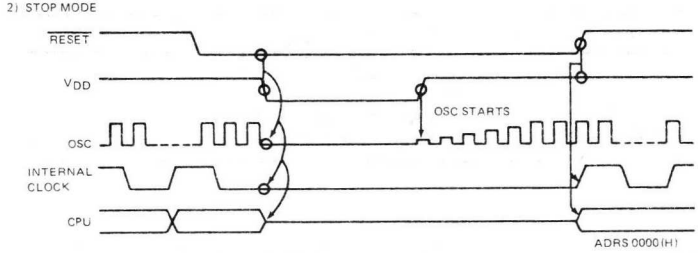
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Port Control Setup before Falling Edge of $\overline{PROG}$	t_{CP}	110			ns	
Port Control Hold after Falling Edge of $\overline{PROG}$	t_{PC}	140			ns	
$\overline{PROG}$ to Time P2 Input must be Valid	t_{PR}			810	ns	
Output Data Setup Time	t_{DP}	220			ns	
Output Data Hold Time	t_{PD}	65			ns	
Input Data Hold Time	t_{PF}			150	ns	
$\overline{PROG}$ Pulse Width	t_{PP}	1510			ns	
Port 2 I/O Data Setup	t_{PL}	400			ns	
Port 2 I/O Data Hold	t_{LP}	150			ns	

TIMING WAVEFORMS

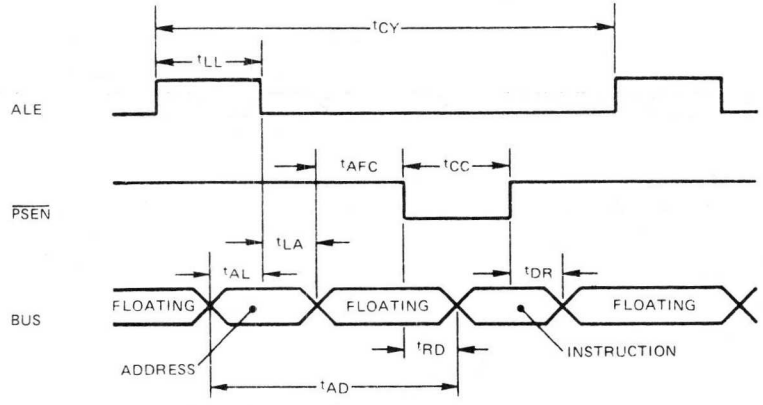
1) HALT MODE (WHEN EI)



2) STOP MODE



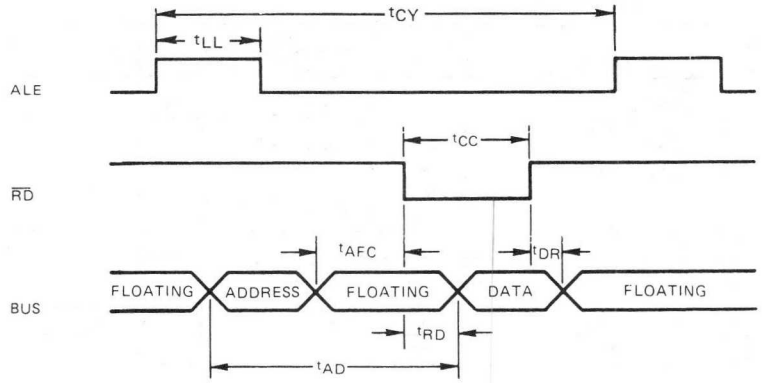
LOW POWER STANDBY OPERATION



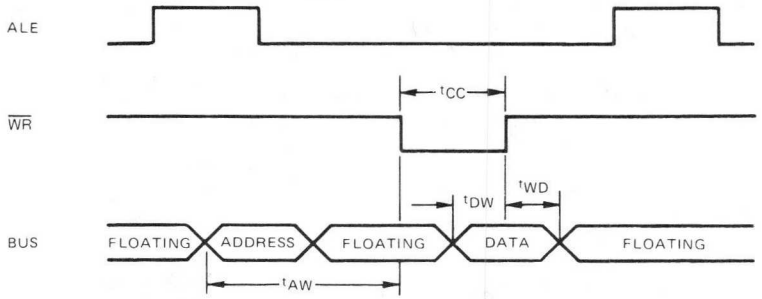
INSTRUCTION FETCH FROM EXTERNAL MEMORY

TIMING WAVEFORMS (CONT.)

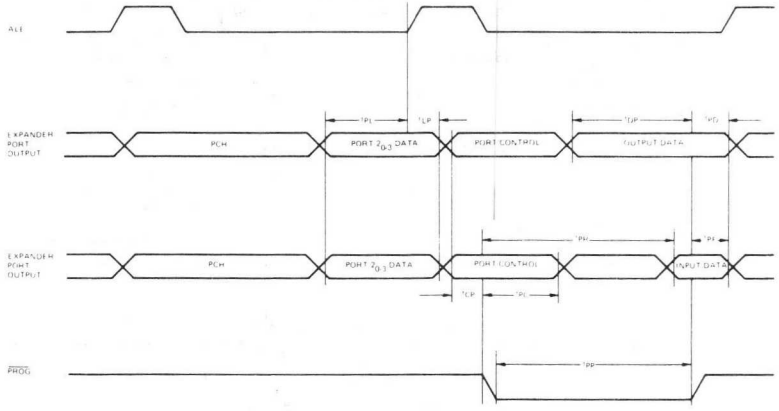
READ FROM EXTERNAL DATA MEMORY



WRITE TO EXTERNAL MEMORY



PORT 2 TIMING



NEW FEATURES

The NEC μPD80C48/μPD80C35 contains all the functional features of the industry standard 8048/8035. The power down mode of the μPD8048 is replaced with two additional power standby features for added power savings. Depending on desired power consumption savings and internal logic status maintenance, the Halt Mode or Stop Mode may be used.

Halt Mode

The μPD80C48/80C35 includes a Halt instruction (01H) — an addition to the standard 8048 instruction set. Upon execution of the Halt instruction, the μPD80C48 enters a Halt mode where the internal clocks and internal logic are disabled. The oscillator, however, continues its operation. The state of all internal logic values and control status prior to the halt state is maintained. Under the Halt mode of operation, power consumption is less than 10% of normal μPD80C48 operation, and 1% of 8048 operation.

The Halt mode is released through either of two methods: an active input on the INT line or a reset operation. Under the Interrupt Release mode, if interrupts are enabled (EI Mode), the INT input restarts the internal clocks to the internal logic. The μPD80C48 then executes the interrupt service routine.

If interrupts are disabled (DI Mode), an $\overline{INT}$ active signal causes the program operation to resume, beginning from the next sequential address after the Halt instruction.

A RESET input causes the normal reset function which starts the program at address 0H.

Note: The V_{CC} range under Halt mode must be maintained at +5V ± 10%, as in normal operation.

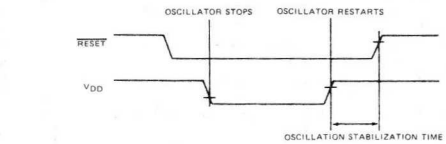
Stop Mode

The Stop mode provides an additional power consumption savings over the Halt mode of operation. The Stop mode is initiated by forcing V_{DD} to the low state during a $\overline{RESET}$ low. While in the Stop mode, oscillator operation is discontinued and only the contents of RAM are maintained.

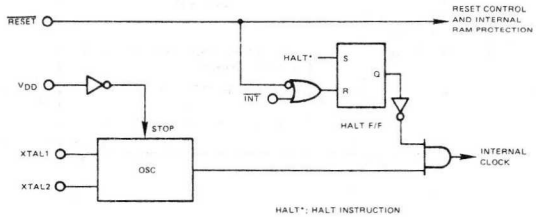
The μPD80C48 is released from the Stop mode when V_{DD} is forced high during a RESET low. Clock generation is then restarted. When oscillator stabilization is achieved, $\overline{RESET}$ is pulled high and the program is restarted from location 0.

Note: To insure reliable Stop mode operation, when releasing the Stop mode V_{DD} must be brought back up to +5V ± 10%. The V_{DD} pin must be protected against noise conditions since it controls oscillator operation. As under normal operation V_{CC} should be maintained at +5V ± 10%. RESET must be held low after oscillation stoppage until it is desired that the oscillator be restarted.

STOP MODE TIMING DIAGRAM



POWER STANDBY CONTROL BLOCK DIAGRAM



MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
ACCUMULATOR																
ADD A, # data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, # data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, # data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 1	**Logical OR Indirect the contents of data memory location with Accumulator.**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**r**	**1**	1				
RL A	(AN + 1) ← (AN) $(A_0) \leftarrow (A_7)$ for N = 0 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 6 $(A_0) \leftarrow$ (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0 6 $(A_7) \leftarrow (A_0)$	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 6 $(A_7) \leftarrow$ (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	$(A_{4-7}) \leftrightarrow (A_0$ 3)	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
BRANCH																
DJNZ Rr, addr	(Rr) ← (Rr) 1; r = 0 7 If (Rr) ≠ 0: (PC 0 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 7) ← addr if C = 1 (PC) ← (PC) + 2 if C 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC 0 7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC 0 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 10) ← addr 8 10 (PC 0 7) ← addr 0 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 7) ← addr if C = 0 (PC) ← (PC) + 2 if C 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 7) ← addr if I 0 (PC) ← (PC) + 2 if I 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
BRANCH (CONT.)																
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
CONTROL																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENTO CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 – 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 – 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 – 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
HALT		Initiate Halt State	0	0	0	0	0	0	0	1	1	1				
DATA MOVES																
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, # data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, # data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0 – 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ↔ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ↔ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ↔ ((Rr)) 0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
FLAGS																
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1
INPUT/OUTPUT																
ANL BUS, = data	(BUS) ← (BUS) AND data	Logical and Immediate-specified data with contents of BUS.	1	0	0	1	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANL Pp, = data	(Pp) ← (Pp) AND data p = 1 2	Logical and Immediate specified data with designated port (1 or 2)	1	0	0	1	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 3) p = 4 7	Logical and contents of Accumulator with designated port (4 7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1 2	Input data from designated port (1 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 7 (A 4 7) ← 0	Move contents of designated port (4 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0 3; p = 4 7	Move contents of Accumulator to designated port (4 7).	0	0	1	1	1	1	p	p	1	1				
ORL BUS, = data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS.	1	0	0	0	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 3) p = 4 7	Logical or contents of Accumulator with designated port (4 7).	1	0	0	0	1	1	p	p	1	1				
ORL Pp, = data	(Pp) ← (Pp) OR data p = 1 2	Logical or Immediate specified data with designated port (1 2)	1	0	0	0	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto BUS.	0	0	0	0	0	0	1	0	1	1				
OUTL Pp, A	(Pp) ← (A); p = 1 2	Output contents of Accumulator to designated port (1 2).	0	0	1	1	1	0	p	p	1	1				
REGISTERS																
DEC Rr (Rr)	(Rr) ← (Rr) 1; r = 0 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) +1; r = 0 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Ri	((Ri)) ← ((Ri)) + 1; r = 0 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
SUBROUTINE																
CALL addr	((SP)) ← (PC), (PSW 4 7)	Call designated Subroutine.	a_{10}	a_9	a_8	1	0	1	0	0	2	2				
	(SP) ← (SP) + 1 (PC 8 10) ← addr 8 10 (PC 0 7) ← addr 0 7 (PC 11) ← DBF		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
RET	(SP) ← (SP) 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) 1 (PC) ← ((SP)) (PSW 4 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
TIMER/COUNTER																
EN TCNTI		Enable Internal Interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal Interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1				
MISCELLANEOUS																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.

② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.

③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.

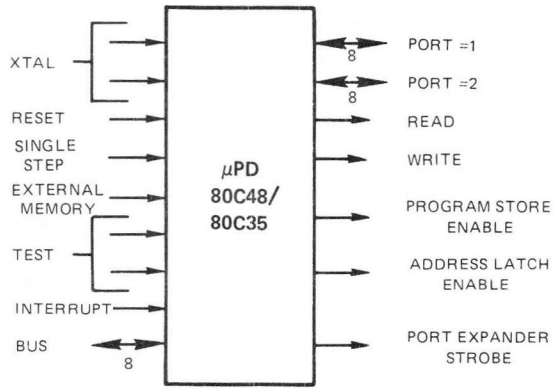
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions:

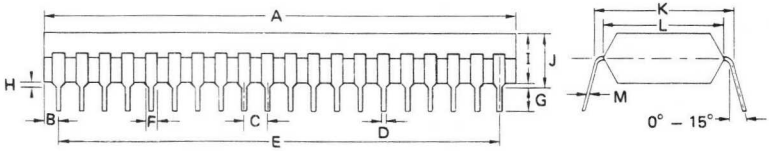
SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By

LOGIC SYMBOL



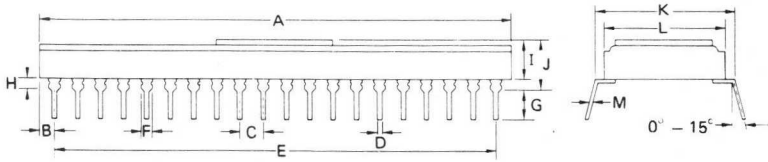
PACKAGE OUTLINES
μPD80C48C
μPD80C35C



(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{0.05}$	$0.010^{+0.004}_{0.002}$

μPD80C48D
μPD80C35D



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

7

HIGH PERFORMANCE SINGLE CHIP 8-BIT MICROCOMPUTERS

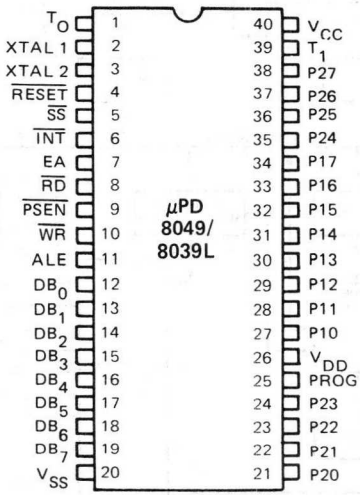
DESCRIPTION

The NEC μPD8049 and μPD8039L are single chip 8-bit microcomputers. The processors differ only in their internal program memory options: the μPD8049 has 2K x 8 bytes of mask ROM and the μPD8039L has external program memory. Both of these devices feature new, high performance 11 MHz operation.

FEATURES

- High Performance 11 MHz Operation
- Fully Compatible with Industry Standard 8049/8039
- Pin Compatible with the μPD8048/8748/8035
- NMOS Silicon Gate Technology Requiring a Single +5V ±10% Supply
- 1.36 μs Cycle Time. All Instructions 1 or 2 Bytes
- Programmable Interval Timer/Event Counter
- 2K x 8 Bytes of ROM, 128 x 8 Bytes of RAM
- Single Level Interrupt
- 96 Instructions: 70 Percent Single Byte
- 27 I/O Lines
- Internal Clock Generator
- Expandable with 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40-Pin Packages

PIN CONFIGURATION



7

μPD8049/8039L

FUNCTIONAL DESCRIPTION

The NEC μPD8049 and μPD8039L are high performance, single component, 8-bit parallel microcomputers using N-channel silicon gate MOS technology. The μPD8049 and μPD8039L function efficiently in control as well as arithmetic applications. The powerful instruction set eases bit handling applications and provides facilities for binary and BCD arithmetic. Standard logic functions implementation is facilitated by the large variety of branch and table look-up instructions.

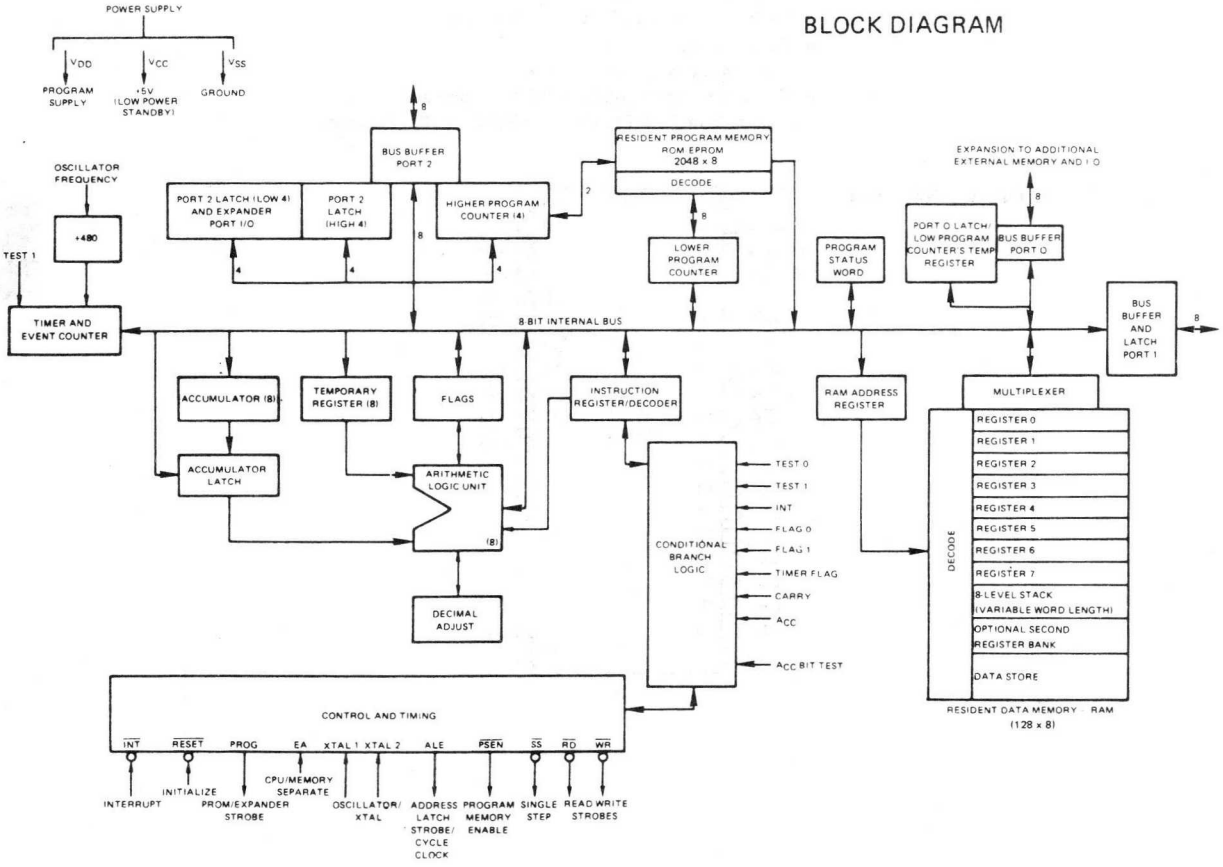
The μPD8049 and μPD8039L instruction set is comprised of 1 and 2 byte instructions with over 70 percent single-byte. The instruction set requires only 1 or 2 cycles per instruction with over 50 percent single-cycle.

The μPD8049 and μPD8039L microprocessors will function as stand-alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8049 contains the following functions usually found in external peripheral devices: 2048 x 8 bits of mask ROM program memory; 128 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; and oscillator and clock circuitry.

The μPD8039L is intended for applications using external program memory only. It contains all the features of the μPD8049 except the 2048 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENT0 CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal, LC, or external frequency source. (Non-TTL compatible V_{IH}.)
3	XTAL 2	The other side of the crystal or LC frequency source. For external sources, XTAL 2 must be driven with the logical complement of the XTAL 1 input.
4	$\overline{RESET}$	Active low input from processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non-TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe outputs (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active-high). Occurring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12-19	D_0-D_7 BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the D_0-D_7 BUS can be latched in a static mode. During an external memory fetch, the D_0-D_7 BUS holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the D_0-D_7 BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21-24, 35-38	P_{20}-P_{27}: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in P_{20}-P_{23}. Bits P_{20}-P_{23} are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	PROG is used as an output strobe for μPD8243's during I/O expansion. When the μPD8049 is used in a stand-alone mode the PROG pan can be allowed to float.
26	V_{DD}	V_{DD} is used to provide +5V to the 128 x 8 bit RAM section. During normal operation V_{CC} must also be +5V to provide power to the other functions in the device. During stand-by operation V_{DD} must remain at +5V while V_{CC} is at ground potential.
27-34	P_{10}-P_{17}: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power supply. V_{CC} is +5V during normal operation.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +125°C
Voltage on Any Pin	− 0.5 to +7 Volts ①
Power Dissipation	1.5 W

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

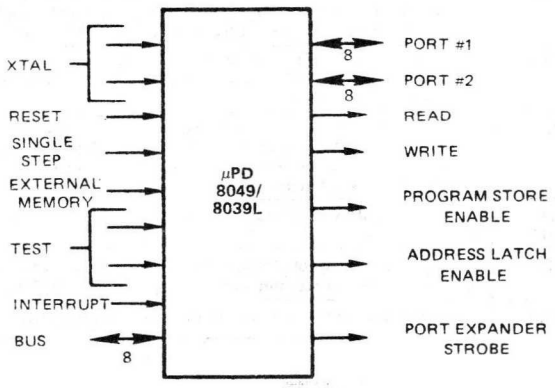
*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = V_{DD} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	-0.5		0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage ($\overline{RESET}$, XTAL 1, XTAL 2)	V_{IH1}	3.8		V_{CC}	V	
Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (All Other Outputs Except PROG)	V_{OL1}			0.45	V	I_{OL} = 1.6 mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	I_{OL} = 1.0 mA
Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH}	2.4			V	I_{OH} = −100 μA
Output High Voltage (All Other Outputs)	V_{OH1}	2.4			V	I_{OH} = −50 μA
Input Leakage Current (T_1, EA, INT)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Output Leakage Current (BUS, T_0 — High Impedance State)	I_{OL}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V
Power Down Supply Current	I_{DD}		25	50	mA	T_a = 25°C
Total Supply Current	$I_{DD} + I_{CC}$		100	170	mA	T_a = 25°C

LOGIC SYMBOL



AC CHARACTERISTICS

READ, WRITE AND INSTRUCTION FETCH – EXTERNAL DATA AND PROGRAM MEMORY

T_a = 0°C to +70°C; V_{CC} = V_{DD} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
ALE Pulse Width	t_{LL}	150			ns	
Address Setup before ALE	t_{AL}	70			ns	
Address Hold from ALE	t_{LA}	50			ns	
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}	300			ns	
Data Setup before $\overline{WR}$	t_{DW}	250			ns	
Data Hold after $\overline{WR}$	t_{WD}	40			ns	C_L = 20 pF ③
Cycle Time	t_{CY}	1.36		15.0	μs	
Data Hold	t_{DR}	0		100	ns	
$\overline{PSEN}$, $\overline{RD}$ to Data In	t_{RD}			200	ns	
Address Setup before $\overline{WR}$	t_{AW}	200			ns	
Address Setup before Data In	t_{AD}			400	ns	
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	-40			ns	

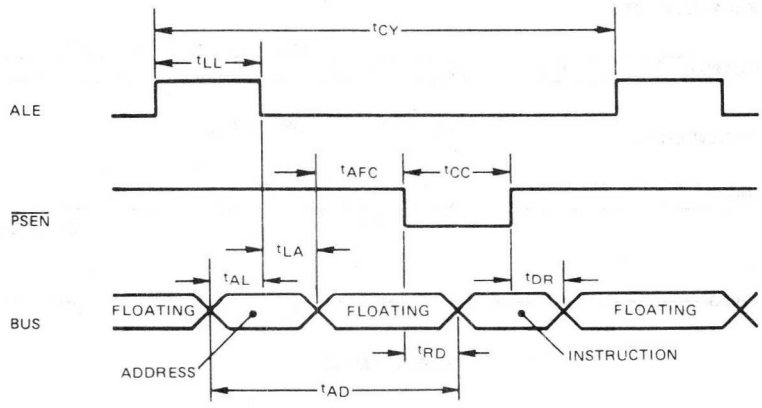
Notes: ① For Control Outputs: C_L = 80 pF
② For Bus Outputs: C_L = 150 pF
③ t_{CY} = 1.36 μs

PORT 2 TIMING

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

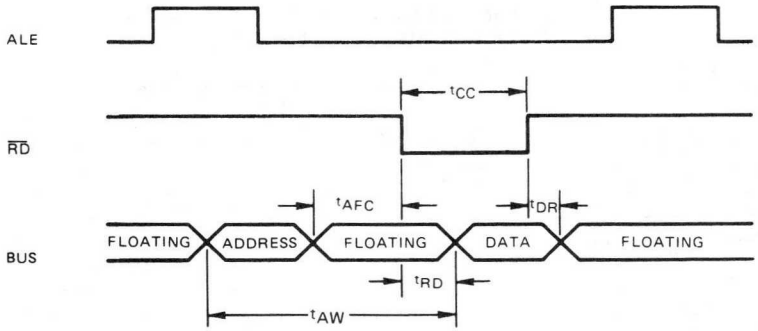
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Port Control Setup before Falling Edge of PROG	t_{CP}	100			ns	
Port Control Hold after Falling Edge of PROG	t_{PC}	60			ns	
PROG to Time P2 Input must be Valid	t_{PR}			650	ns	
Output Data Setup Time	t_{DP}	200			ns	
Output Data Hold Time	t_{PD}	20			ns	
Input Data Hold Time	t_{PF}	0		150	ns	
PROG Pulse Width	t_{PP}	700			ns	
Port 2 I/O Data Setup	t_{PL}	150			ns	
Port 2 I/O Data Hold	t_{LP}	20			ns	

TIMING WAVEFORMS

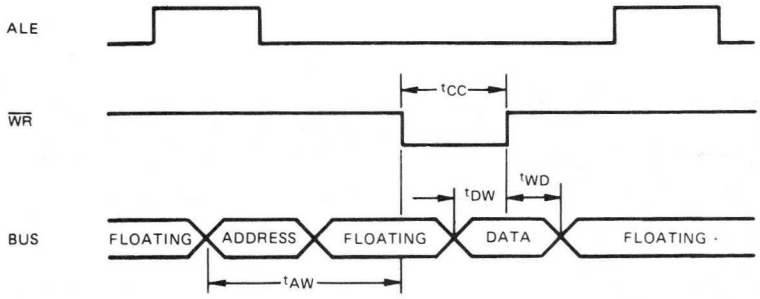


INSTRUCTION FETCH FROM EXTERNAL MEMORY

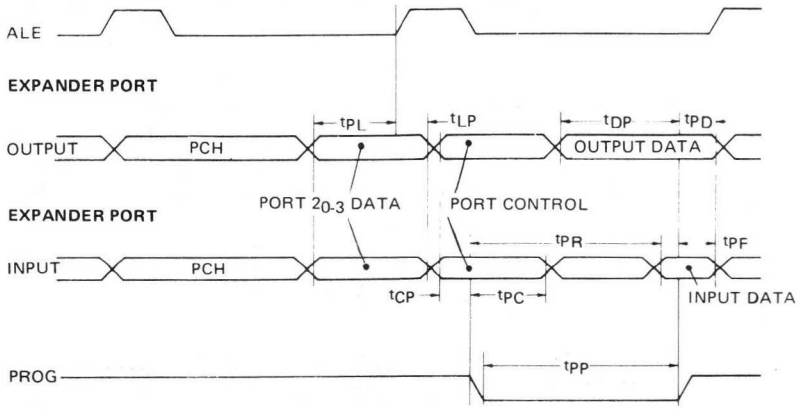
TIMING WAVEFORMS (CONT.)



READ FROM EXTERNAL DATA MEMORY



WRITE TO EXTERNAL MEMORY



PORT 2 TIMING

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
ACCUMULATOR																
ADD A, #data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0	0	0	0	0	0	1	1	2	2	•			
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, #data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0	0	0	1	0	0	1	1	2	2	•			
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, #data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0	1	0	1	0	0	1	1	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, #data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0	1	0	0	0	0	1	1	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) $(A_0) \leftarrow (A_7)$ for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 6 $(A_0) \leftarrow$ (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0 6 $(A_7) \leftarrow (A_0)$	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 6 $(A_7) \leftarrow$ (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	$(A_{4-7}) \leftrightarrow (A_0$ 3)	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, #data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1	1	0	1	0	0	1	1	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
BRANCH																
DJNZ Rr, addr	(Rr) ← (Rr) 1; r = 0 7 If (Rr) ≠ 0: (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1	1	1	0	1	r	r	r	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JBb addr	(PC 0 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2	b_1	b_0	1	0	0	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1	1	1	1	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JF0 addr	(PC 0 7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1	0	1	1	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JF1 addr	(PC 0 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0	1	1	1	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JMP addr	(PC 8 10) ← addr 8 10 (PC 0 7) ← addr 0 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10}	a_9	a_8	0	0	1	0	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JMPP @ A	(PC 0 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1	1	1	0	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JNI addr	(PC 0 7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1	0	0	0	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						

INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
BRANCH (CONT.)																
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
CONTROL																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 – 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 – 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 – 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
DATA MOVES																
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, # data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, # data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0 – 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ⇄ ((Rr)) 0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
FLAGS																
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1
INPUT/OUTPUT																
ANL BUS, = data	(BUS) ← (BUS) AND data	Logical and Immediate specified data with contents of BUS.	1	0	0	1	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANL Pp, = data	(Pp) ← (Pp) AND data p = 1 2	Logical and Immediate specified data with designated port (1 or 2)	1	0	0	1	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 3) p = 4 7	Logical and contents of Accumulator with designated port (4 7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp), p = 1 2	Input data from designated port (1 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0 3) ← (Pp); p = 4 7 (A 4 7) ← 0	Move contents of designated port (4 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0 3; p = 4 7	Move contents of Accumulator to designated port (4 7).	0	0	1	1	1	1	p	p	1	1				
ORL BUS, = data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS.	1	0	0	0	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 3) p = 4 7	Logical or contents of Accumulator with designated port (4 7).	1	0	0	0	1	1	p	p	1	1				
ORL Pp, = data	(Pp) ← (Pp) OR data p = 1 2	Logical or Immediate specified data with designated port (1 2)	1	0	0	0	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto BUS.	0	0	0	0	0	0	1	0	1	1				
OUTL Pp, A	(Pp) ← (A); p = 1 2	Output contents of Accumulator to designated port (1 2).	0	0	1	1	1	0	p	p	1	1				
REGISTERS																
DEC Rr (Rr)	(Rr) ← (Rr) 1; r = 0 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) +1; r = 0 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
SUBROUTINE																
CALL addr	((SP)) ← (PC), (PSW 4 7)	Call designated Subroutine.	a_{10}	a_9	a_8	1	0	1	0	0	2	2				
	(SP) ← (SP) + 1 (PC 8 10) ← addr 8 10 (PC 0 7) ← addr 0 7 (PC 11) ← DBF		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
RET	(SP) ← (SP) 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) 1 (PC) ← ((SP)) (PSW 4 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
TIMER/COUNTER																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1				
MISCELLANEOUS																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

Notes ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.

② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.

③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.

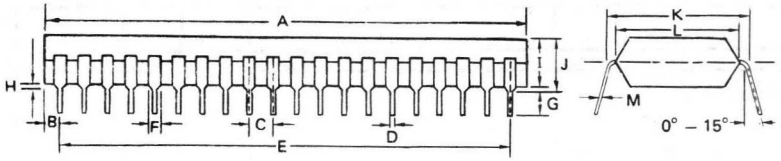
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By

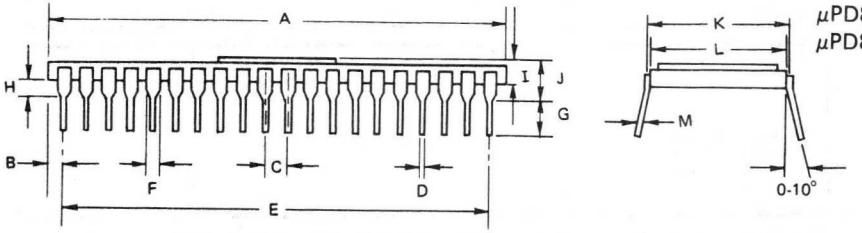
7



PACKAGE OUTLINES
μPD8049C
μPD8039LC

(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.028 MAX.
B	1.62 MAX.	0.064 MAX.
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.2 MIN.	0.047 MIN.
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.019 MIN.
I	5.22 MAX.	0.206 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24 TYP.	0.600 TYP.
L	13.2 TYP.	0.520 TYP.
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



μPD8049D
μPD8039LD

(CERAMIC)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.03 MAX.
B	1.62 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.0019

8-BIT N-CHANNEL MICROPROCESSOR COMPLETELY Z80™ COMPATIBLE

DESCRIPTION

The μPD780 and μPD780-1 processors are single-chip microprocessors developed from third-generation technology. Their increased computational power produces higher system through-put and more efficient memory utilization, surpassing that of any second-generation microprocessor. The single voltage requirement of the μPD780 and μPD780-1 processors makes it easy to implement them into a system. All output signals are fully decoded and timed to either standard memory or peripheral circuits. An N-channel, ion-implanted, silicon gate MOS process is utilized in implementing the circuit.

The block diagram shows the functions of the processor and details the internal register structure. The structure contains 26 bytes of Read/Write (R/W) memory available to the programmer. Included in the registers are two sets of six general purpose registers, which may be used individually as 8-bit registers, or as 6-bit register pairs. Also included are two sets of accumulator and flag registers.

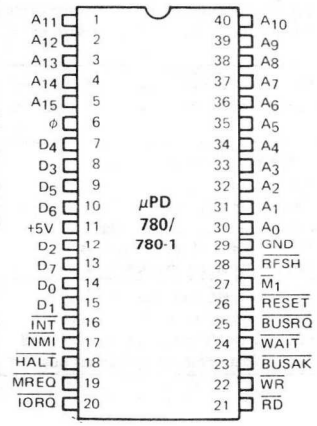
Through a group of exchange instructions the programmer has access to either set of main or alternate registers. The alternate register permits foreground/background mode of operation, or may be used for fast interrupt response. A 16-bit stack pointer is also included in each processor, simplifying implementation of multiple level interrupts, permitting unlimited subroutine nesting, and simplifying many types of data handling.

The two 16-bit index registers simplify implementation of relocatable code and manipulation of tabular data. The refresh register automatically refreshes external dynamic memories. A powerful interrupt response mode uses the I register to form the upper 8 bits of a pointer to an interrupt service address table, while the interrupting apparatus supplies the lower 8 bits of the pointer. An indirect call will then be made to service this address.

FEATURES

- Single Chip, N-Channel Silicon Gate Processor
- 158 Instructions – Including all 78 of the 8080A Instructions, Permitting Total Software Compatibility
- New 4-, 8-, and 16-Bit Operations Featuring Useful Addressing Modes such as Indexed, Bit and Relative
- 17 Internal Registers
- Three Modes of Rapid Interrupt Response, and One Non-Maskable Interrupt
- Directly Connects Standard Speed Dynamic or Static Memories, with Minimum Support Circuitry
- Single-Phase +5 Volt Clock and 5 VDC Supply
- TTL Compatibility
- Automatic Dynamic RAM Refresh Circuitry
- Available in Plastic Package

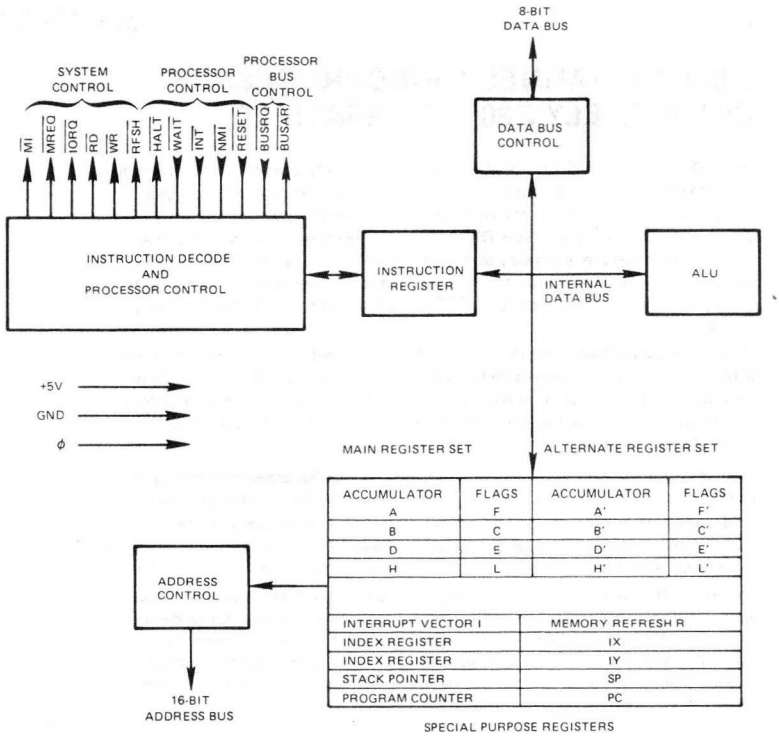
PIN CONFIGURATION



8

TM: Z80 is a registered trademark of Zilog, Inc.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1-5, 30-40	A_0-A_{15}	Address Bus	3-State Output, active high. Pins A_0-A_{15} constitute a 16-bit address bus, which provides the address for memory and I/O device data exchanges. Memory capacity 65,536 bytes. A_0-A_7 is also needed as refresh cycle.
7-10, 12-15	D_0-D_7	Data Bus	3-State input/output, active high. Pins D_0-D_7 compose an 8-bit, bidirectional data bus, used for data exchanges with memory and I/O devices.
27	$\overline{M}_1$	Machine Cycle One	Output, active low. $\overline{M}_1$ indicates that the machine cycle in operation is the op code fetch cycle of an instruction execution.
19	$\overline{MREQ}$	Memory Request	3-State output, active low. $\overline{MREQ}$ indicates that a valid address for a memory read or write operation is held in the address.
20	$\overline{IORQ}$	Input/Output Request	3-State output, active low. The I/O request signal indicates that the lower half of the address bus holds a valid address for an I/O read or write operation. The $\overline{IORQ}$ signal is also used to acknowledge an interrupt command, indicating that an interrupt response vector can be placed on the data bus.
21	$\overline{RD}$	Memory Read	3-State output, active low. $\overline{RD}$ indicates that the processor is requesting data from memory or an I/O device. The memory or I/O device being addressed should use this signal to gate data onto the data bus.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
22	$\overline{WR}$	Memory Write	3-State output, active low. The memory write signal indicates that the processor data bus is holding valid data to be stored in the addressed, memory or I/O device.
28	$\overline{RFSH}$	Refresh	Output, active low. $\overline{RFSH}$ indicates that a refresh address for dynamic memories is being held in the lower 7-bits of the address bus. The $\overline{MREQ}$ signal should be used to implement a refresh read to all dynamic memories.
18	$\overline{HALT}$	Halt State	Output, active low. $\overline{HALT}$ indicates that the processor has executed a HALT software instruction, and will not resume operation until either a non-maskable or a maskable (with mask enabled) interrupt has been implemented. The processor will execute NOP's while halted, to maintain memory refresh activity.
24	$\overline{WAIT}$	Wait	Input, active low. $\overline{WAIT}$ indicates to the processor that the memory or I/O devices being addressed are not ready for a data transfer. As long as this signal is active, the processor will reenter wait states.
16	$\overline{INT}$	Interrupt Request	Input, active low. The $\overline{INT}$ signal is produced by I/O devices. The request will be honored upon completion of the current instruction, if the interrupt enable flip-flop (IFF) is enabled by the internal software. There are three modes of interrupt response. Mode 0 is identical to 8080 interrupt response mode. The Mode 1 response is a restart location at 0038_H. Mode 2 is for simple vectoring to an interrupt service routine anywhere in memory.
17	$\overline{NMI}$	Non-Maskable Interrupt	Input, active low. The non-maskable interrupt has a higher priority than $\overline{INT}$. It is always acknowledged at the end of the current instruction, regardless of the status of the interrupt enable flip-flop. When the $\overline{NMI}$ signal is given, the μPD780 processor automatically restarts to location 0066_H.
26	$\overline{RESET}$	Reset	Input, active low. The $\overline{RESET}$ signal causes the processor to reset the interrupt enable flip-flop (IFF), clear PC and I and R registers, and set interrupt to 8080A mode. During the reset time, the address bus and data bus go to a state of high impedance, and all control output signals become inactive, after which processing continues at 0000H.
25	$\overline{BUSRQ}$	Bus Request	Input, active low. $\overline{BUSRQ}$ has a higher priority than $\overline{NMI}$, and is always honored at the end of the current machine cycle. It is used to allow other devices to take control over the processor address bus, data bus signals; by requesting that they go to a state of high impedance.
23	$\overline{BUSAK}$	Bus Acknowledge	Output, active low. $\overline{BUSAK}$ is used to inform the requesting device that the processor address bus, data bus and 3-state control bus signals have entered a state of high impedance, and the external device can now take control of these signals.

8

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin	−0.3 to +7 Volts (1)
Power Dissipation	1.5W

Note: (1) With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage		V_{ILC}	−0.3		0.45	V	
Clock Input High Voltage		V_{IHC}	V_{CC}−0.6		V_{CC}+0.3	V	
Input Low Voltage		V_{IL}	−0.3		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{CC}	V	
Output Low Voltage		V_{OL}			0.4	V	I_{OL} = 1.8 mA
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −250 μA
Power Supply Current	μPD780	I_{CC}			150	mA	t_c = 400 ns
	μPD780-1	I_{CC}		90	200	mA	t_c = 250 ns
Input Leakage Current		I_{LI}			10	μA	V_{IN} = 0 to V_{CC}
Tri-State Output Leakage Current in Float		I_{LOH}			10	μA	V_{OUT} = 2.4 to V_{CC}
Tri-State Output Leakage Current in Float		I_{LOL}			−10	μA	V_{OUT} = 0.4 V
Data Bus Leakage Current in Input Mode		I_{LD}			±10	μA	$0 \leq V_{IN} \leq V_{CC}$

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ			35	pF	f_c = 1 MHz
Input Capacitance	C_{IN}			5	pF	Unmeasured Pins
Output Capacitance	C_{OUT}			10	pF	Returned to Ground

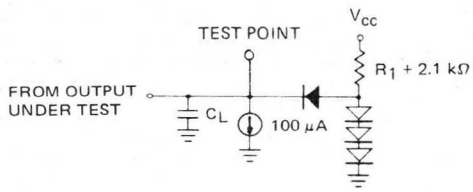
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS μPD780 MIN	LIMITS μPD780 MAX	LIMITS μPD780-1 MIN	LIMITS μPD780-1 MAX	UNIT	TEST CONDITIONS
Clock Period	t_c	0.4	⑫	0.25	⑫	μs	
Clock Pulse Width, Clock High	$t_{w(\Phi H)}$	180		110		ns	
Clock Pulse Width, Clock Low	$t_{w(\Phi L)}$	180	2000	110	2000	ns	
Clock Rise and Fall Time	t_r, t_f		30		30	ns	
Address Output Delay	$t_{D(AD)}$		145		110	ns	
Delay to Float	$t_{F(AD)}$		110		90	ns	
Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	t_{acm}	①		①		ns	C_L = 50 pF
Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	t_{aci}	②		②		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$	t_{ca}	③		③		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$ During Float	t_{caf}	④		④		ns	
Data Output Delay	$t_{D(D)}$		230		150	ns	
Delay to Float During Write Cycle	$t_{F(D)}$		90		90	ns	
Data Setup Time to Rising Edge of Clock During M1 Cycle	$t_{S\Phi(D)}$	50		35		ns	
Data Setup Time to Falling Edge of Clock During M2 to M5 Cycles	$t_{S\bar{\Phi}(D)}$	60		50		ns	C_L = 200 pF
Data Stable Prior to $\overline{WR}$ (Memory Cycle)	t_{dcm}	⑤		⑤		ns	
Data Stable Prior to $\overline{WR}$ (I/O Cycle)	t_{dci}	⑥		⑥		ns	
Data Stable from $\overline{WR}$	t_{cdf}	⑦		⑦		ns	
Any Hold Time for Setup Time	t_H	0			0	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ Low	$t_{DL\Phi(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Rising Edge of Clock to $\overline{MREQ}$ High	$t_{DH\Phi(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ High	$t_{DH\bar{\Phi}(MR)}$		100		85	ns	
Pulse Width, $\overline{MREQ}$ Low	$t_{w(MRL)}$	⑧		⑧		ns	
Pulse Width, $\overline{MREQ}$ High	$t_{w(MRH)}$	⑨		⑨		ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\Phi(IR)}$		90		75	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\bar{\Phi}(IR)}$		110		85	ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ High	$t_{DH\Phi(IR)}$		100		85	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ High	$t_{DH\bar{\Phi}(IR)}$		110		85	ns	C_L = 50 pF
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ Low	$t_{DL\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ Low	$t_{DL\bar{\Phi}(RD)}$		130		95	ns	
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ High	$t_{DH\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ High	$t_{DH\bar{\Phi}(RD)}$		110		85	ns	
$\overline{WR}$ Delay from Rising Edge of Clock to $\overline{WR}$ Low	$t_{DL\Phi(WR)}$		80		65	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ Low	$t_{DL\bar{\Phi}(WR)}$		90		80	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ High	$t_{DH\Phi(WR)}$		100		80	ns	
Pulse Width to $\overline{WR}$ Low	$t_{w(WRL)}$	⑩		⑩		ns	
$\overline{MI}$ Delay from Rising Edge of Clock to $\overline{MI}$ Low	$t_{DL(MI)}$		130		100	ns	C_L = 30 pF
$\overline{MI}$ Delay from Rising Edge of Clock to $\overline{MI}$ High	$t_{DH(MI)}$		130		100	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ Low	$t_{DL(RF)}$		180		130	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ High	$t_{DH(RF)}$		150		120	ns	
$\overline{WAIT}$ Setup Time to Falling Edge of Clock	$t_{S(WT)}$	70		70		ns	
$\overline{HALT}$ Delay Time from Falling Edge of Clock	$t_{D(HT)}$		300		300	ns	C_L = 50 pF
$\overline{INT}$ Setup Time to Rising Edge of Clock	$t_{S(IT)}$	80		80		ns	
Pulse Width, $\overline{NMI}$ Low	$t_{w(NML)}$	80		80		ns	
$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	$t_{S(BQ)}$	80		50		ns	
$\overline{BUSAK}$ Delay from Rising Edge of Clock to $\overline{BUSAK}$ Low	$t_{DL(BA)}$		120		100	ns	C_L = 50 pF
$\overline{BUSAK}$ Delay from Falling Edge of Clock to $\overline{BUSAK}$ High	$t_{DH(BA)}$		110		100	ns	
$\overline{RESET}$ Setup Time to Rising Edge of Clock	$t_{S(RS)}$	90		60		ns	
Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)	$t_{F(C)}$		100		80	ns	
$\overline{MI}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	t_{mr}	⑪		⑪		ns	

Notes:
① $t_{acm} = t_{w(\Phi H)} + t_f - 65$ (75)*
② $t_{aci} = t_c - 70$ (80)*
③ $t_{ca} = t_{w(\Phi L)} + t_r - 50$ (40)*
④ $t_{caf} = t_{w(\Phi L)} + t_r - 45$ (60)*
⑤ $t_{dcm} = t_c - 170$ (210)*
⑥ $t_{dci} = t_{w(\Phi L)} + t_r - 170$ (210)*
⑦ $t_{cdf} = t_{w(\Phi L)} + t_r - 70$ (80)*
⑧ $t_{w(\overline{MRL})} = t_c - 30$ (40)*
⑨ $t_{w(\overline{MRH})} = t_{w(\Phi H)} + t_f - 20$ (30)*
⑩ $t_{w(\overline{WR})} = t_c - 30$ (40)*
⑪ $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 65$ (80)*
⑫ $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

*These values apply to the μPD780.

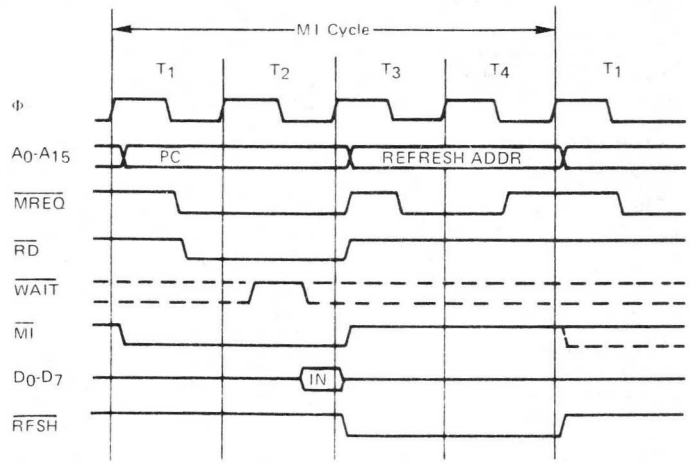


LOAD CIRCUIT FOR OUTPUT

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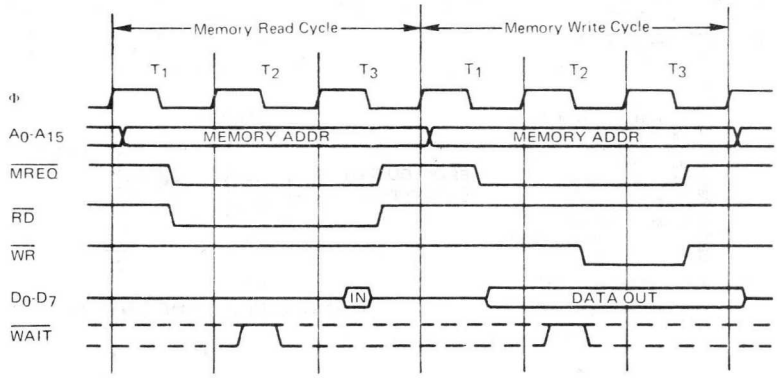
Instruction Op Code Fetch

The contents of the program counter (PC) are placed on the address bus at the start of the cycle. $\overline{MREQ}$ goes active one-half clock cycle later, and the falling edge of this signal can be used directly as a chip enable to dynamic memories. The memory data should be enabled onto the processor data bus when $\overline{RD}$ goes active. The processor takes data with the rising edge of the clock state T_3. The processor internally decodes and executes the instruction, while clock states T_3 and T_4 of the fetch cycle are used to refresh dynamic memories. The refresh control signal $\overline{RFSH}$ indicates that a refresh read should be done to all dynamic memories.



Memory Read or Write Cycles

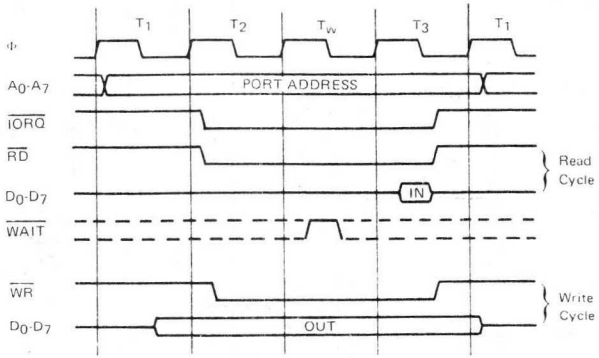
This diagram illustrates the timing of memory read or write cycles other than an op code fetch (M_1 cycle). The function of the $\overline{MREQ}$ and $\overline{RD}$ signals is exactly the same as in the op code fetch cycle. When a memory write cycle is implemented, the $\overline{MREQ}$ becomes active and is used directly as a chip enable for dynamic memories, when the address bus is stable. The $\overline{WR}$ line is used directly as a R/W pulse to any type of semiconductor memory, and is active when data on the data bus is stable.



TIMING WAVEFORMS (CONT.)

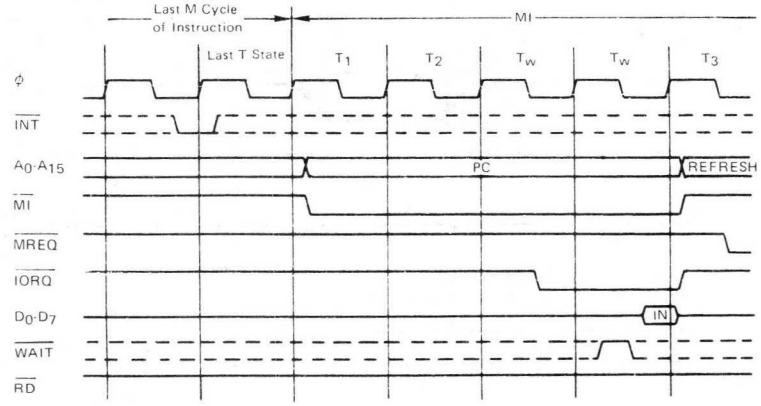
Input or Output Cycles

This illustrates the timing for an I/O read or I/O write operation. A single wait-state (T_W) is automatically inserted in I/O operations to allow sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line, if necessary.



Interrupt Request/Acknowledge Cycle

The processor samples the interrupt signal with the rising edge of the last clock at the end of any instruction. A special M_1 cycle is started when an interrupt is accepted. During the M_1 cycle, the $\overline{IORQ}$ (instead of $\overline{MREQ}$) signal becomes active, indicating that the interrupting device can put an 8-bit vector on the data bus. Two wait states (T_W) are automatically added to this cycle. This makes it easy to implement a ripple priority interrupt scheme.



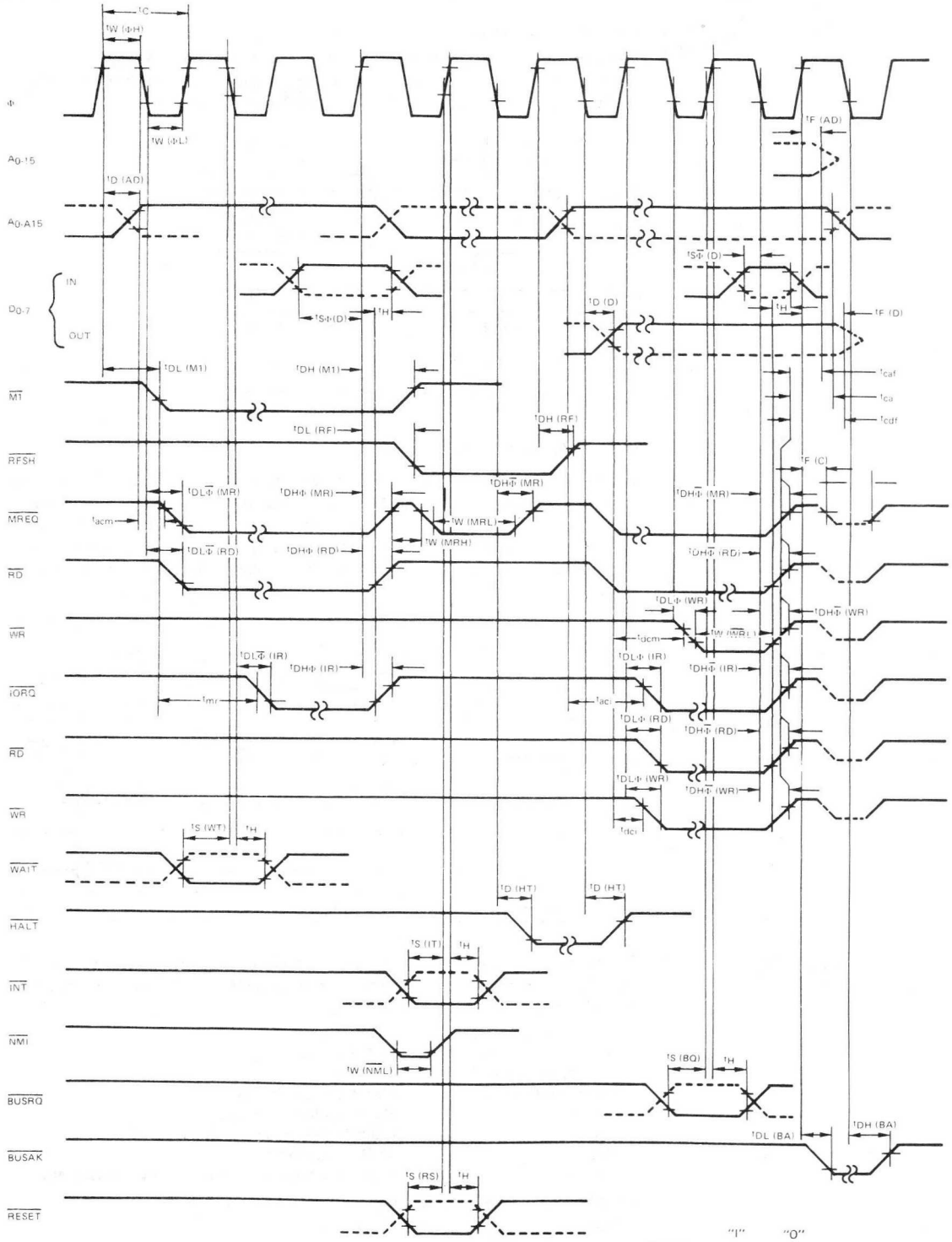
INSTRUCTION SET

The following summary shows the assembly language mnemonic and the symbolic operation performed by the instructions of the μPD780 and μPD780-1 processors. The instructions are divided into 16 categories:

Miscellaneous Group	8-Bit Loads
Rotates and Shifts	16-Bit Loads
Bit Set, Reset and Test	Exchanges
Input and Output	Memory Block Moves
Jumps	Memory Block Searches
Calls	8-Bit Arithmetic and Logic
Restarts	16-Bit Arithmetic
Returns	General Purpose Accumulator and Flag Operations

The addressing Modes include combinations of the following:

Indexed	Immediate
Register	Immediate Extended
Implied	Modified Page Zero
Register Indirect	Relative
Bit	Extended



	"I"	"O"
CLOCK	4.2V	0.8V
OUTPUT	2.0V	0.8V
INPUT	2.0V	0.8V
FLOAT	ΔV	±0.5V

Note: ① Timing measurements are made at the following voltages unless otherwise specified:

INSTRUCTION SET TABLE

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
ADC HL, ss	HL ← HL + ss + CY	Add with carry reg. pair ss to HL	1	11	↕	↕	V	↕	0	X	11 101 101 Ⓐ 01 ss1 010
ADC A, r	A ← A + r + CY	Add with carry Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 001 r r r Ⓑ
ADC A,n	A ← A + n + CY	Add with carry value n to ACC		7	↕	↕	V	↕	0	↕	11 001 110 n n n n n n n
ADC A, (HL)	A ← A + (HL) + CY	Add with carry loc. (HL) to ACC		7	↕	↕	V	↕	0	↕	10 001 110
ADC A, (IX + d)	A ← A + (IX + d) + CY	Add with carry loc. (IX + d) to ACC		19	↕	↕	V	↕	0	↕	11 011 101 10 001 110 d d d d d d d
ADC A, (IY + d)	A ← A + (IY + d) + CY	Add with carry loc. (IY + d) to ACC		19	↕	↕	V	↕	0	↕	11 111 101 10 001 110 d d d d d d d
ADD A, n	A ← A + n	Add value n to ACC	2	7	↕	↕	V	↕	0	↕	11 000 110 n n n n n n n
ADD A, r	A ← A + r	Add Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 000 r r r Ⓑ
ADD A, (HL)	A ← A + (HL)	Add location (HL) to ACC	1	7	↕	↕	V	↕	0	↕	10 000 110
ADD A, (IX + d)	A ← A + (IX + d)	Add location (IX + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 011 101 10 000 110 d d d d d d d
ADD A, (IY + d)	A ← A + (IY + d)	Add location (IY + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 111 101 10 000 110 d d d d d d d
ADD HL, ss	HL ← HL + ss	Add Reg. pair ss to HL	1	11	↕	•	•	•	0	X	00 ss 1 001 Ⓐ
ADD IX, pp	IX ← IX + pp	Add Reg. pair pp to IX	2	15	↕	•	•	•	0	X	11 011 101 Ⓒ 00 pp1 001
ADD IY, rr	IY ← IY + rr	Add Reg. pair rr to IY	2	15	↕	•	•	•	0	X	11 111 101 Ⓓ 00 rr1 001
AND r	A ← A∧r	Logical 'AND' of Reg. r ∧ ACC		4	0	↕	P	↕	0	↕	10 100 r r r Ⓑ
AND n	A ← A∧n	Logical 'AND' of value n ∧ ACC		7	0	↕	P	↕	0	↕	11 100 110 n n n n n n n
AND (HL)	A ← A∧(HL)	Logical 'AND' of loc. (HL) ∧ ACC		7	0	↕	P	↕	0	↕	10 100 110
AND (IX + d)	A ← A∧(IX + d)	Logical 'AND' of loc. (IX + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 011 101 10 100 110 d d d d d d d
AND (IY + d)	A ← A∧(IY + d)	Logical 'AND' of loc. (IY + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 111 101 10 100 110 d d d d d d d
BIT b, (HL)	Z ← $\overline{(HL)}_b$	Test BIT b of location (HL)	2	12	•	↕	X	X	0	1	11 001 011 Ⓔ 01 b b b 110
BIT b, (IX + d)	Z ← $\overline{(IX + d)}_b$	Test BIT b at location (IX + d)	4	20	•	↕	X	X	0	1	11 011 101 Ⓔ 11 001 011 d d d d d d d 01 b b b 110
BIT b, (IY + d)	Z ← $\overline{(IY + d)}_b$	Test BIT b at location (IY + d)	4	20	•	↕	X	X	0	1	11 111 101 Ⓔ 11 001 011 d d d d d d d 01 b b b 110
BIT b, r	Z ← $\overline{r}_b$	Test BIT of Reg. r	2	8	•	↕	X	X	0	1	11 001 011 01 b b b r r r Ⓑ Ⓔ
CALL cc, nn	If condition cc false continue, else same as CALL nn	Call subroutine at location nn if condition cc is true	3	10	•	•	↕	•	•	•	11 ←cc→ 100 Ⓗ n n n n n n n n n n n n n n
CALL nn	(SP − 1) ← PC_H (SP − 2) ← PC_L PC ← nn	Unconditional call subroutine at location nn	3	17	•	•	•	•	•	•	11 001 101 n n n n n n n n n n n n n n
CCF	CY ← $\overline{CY}$	Complement carry flag	1	4	↕	•	•	•	0	X	00 111 111
CP r	A − r	Compare Reg. r with ACC		4	↕	↕	V	↕	1	↕	10 111 r r r Ⓑ
CP n	A − n	Compare value n with ACC		7	↕	↕	V	↕	1	↕	11 111 110 n n n n n n n
CP (HL)	A − (HL)	Compare loc. (HL) with ACC		7	↕	↕	V	↕	1	↕	10 111 110
CP (IX + d)	A − (IX + d)	Compare loc. (IX + d) with ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 111 110 d d d d d d d
CP (IY + d)		Compare loc. (IY + d) with ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 111 110 d d d d d d d
CPD	A − (HL) HL ← HL − 1 BC ← BC − 1	Compare location (HL) and ACC, decrement HL and BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 101 001
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, decrement HL and BC, repeat until BC = 0	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 111 001

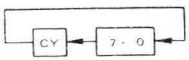
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MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
CPI	A – (HL) HL ← HL + 1 BC ← BC – 1	Compare location (HL) and ACC, increment HL and decrement BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 100 001
CPIR	A – (HL) HL ← HL + 1 BC ← BC – 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, increment HL, decrement BC Repeat until BC = C	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 110 001
CPL	A ← A	Complement ACC (1's comp.)	1	4	•	•	•	•	1	1	00 101 111
DAA		Decimal adjust ACC	1	4	↕	↕	P	↕	•	↕	00 100 111
DEC r	r ← r – 1	Decrement Reg. r		4	•	↕	V	↕	1	↕	00 rrr 101Ⓑ
DEC (HL)	(HL) ← (HL) – 1	Decrement loc. (HL)		11	•	↕	V	↕	1	↕	00 110 101
DEC (IX + d)	(IX + d) ← (IX + d) – 1	Decrement loc. (IX + d)		23	•	↕	V	↕	1	↕	11 011 101 00 110 101 dd ddd ddd
DEC (IY + d)	(IY + d) ← (IY + d) – 1	Decrement loc. (IY + d)		23	•	↕	V	↕	1	↕	11 111 101 00 110 101 dd ddd ddd
DEC IX	IX ← IX – 1	Decrement IX	2	10	•	•	•	•	•	•	11 011 101 00 101 011
DEC IY	IY ← IY – 1	Decrement IY	2	10	•	•	•	•	•	•	11 111 101 00 101 011
DEC ss	ss ← ss – 1	Decrement Reg. pair ss	1	6	•	•	•	•	•	•	00 ss1 011Ⓐ
DI	IFF ← 0	Disable interrupts	1	4	•	•	•	•	•	•	11 110 011
DJNZ, e	B ← B – 1 if B = 0 continue if B ≠ 0 PC ← PC + e	Decrement B and jump relative if B = 0	2	8	•	•	•	•	•	•	00 010 000 ◄—e-2—►
EI	IFF ← 1	Enable interrupts	1	4	•	•	•	•	•	•	11 111 011
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	Exchange the location (SP) and HL	1	19	•	•	•	•	•	•	11 100 011
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	Exchange the location (SP) and IX	2	23	•	•	•	•	•	•	11 011 101 11 100 011
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	Exchange the location (SP) and IY	2	23	•	•	•	•	•	•	11 111 101 11 100 011
EX AF, AF'	AF ↔ AF'	Exchange the contents of AF, AF'	1	4	•	•	•	•	•	•	00 001 000
EX DE, HL	DE ↔ HL	Exchange the contents of DE and HL	1	4	•	•	•	•	•	•	11 101 011
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	Exchange the contents of BC, DE, HL with contents of BC', DE', HL', respectively	1	4	•	•	•	•	•	•	11 011 001
HALT	Processor Halted	HALT (wait for interrupt or reset)	1	4	•	•	•	•	•	•	01 110 110
IM 0		Set Interrupt mode 0	2	8	•	•	•	•	•	•	11 101 101 01 000 110
IM 1		Set Interrupt mode 1	2	8	•	•	•	•	•	•	11 101 101 01 010 110
IM 2		Set Interrupt mode 2	2	8	•	•	•	•	•	•	11 101 101 01 011 110
IN A, (n)	A ← (n)	Load ACC with input from device n	2	11	•	•	•	•	•	•	11 011 011 nn nnn nnn
IN r, (C)	r ← (C)	Load Reg. r with input from device (C)	2	12	•	↕	P	↕	0	↕	11 101 101Ⓘ 01 rrr 000
INC (HL)	(HL) ← (HL) + 1	Increment location (HL)	1	11	•	↕	V	↕	0	↕	00 110 100
INC IX	IX ← IX + 1	Increment IX	2	10	•	•	•	•	•	•	11 011 101 00 100 011
INC (IX + d)	(IX + d) ← (IX + d) + 1	Increment location (IX + d)	3	23	•	↕	V	↕	0	↕	11 011 101 00 110 100 dd ddd ddd
INC IY	IY ← IY + 1	Increment IY	2	10	•	•	•	•	•	•	11 111 101 00 100 011
INC (IY + d)	(IY + d) ← (IY + d) + 1	Increment location (IY + d)	3	23	•	↕	V	↕	0	↕	11 111 101 00 110 100 dd ddd ddd
INC r	r ← r + 1	Increment Reg. r	1	4	•	↕	V	↕	0	↕	00 rrr 100Ⓑ
INC ss	ss ← ss + 1	Increment Reg. pair ss	1	6	•	•	•	•	•	•	00 ss0 011Ⓐ
IND	(HL) ← (C) B ← B' – 1 HL ← HL – 1	Load location (HL) with input from port (C), decrement HL and B	2	16	•	↕③	X	X	1	X	11 101 101 10 101 010

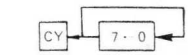
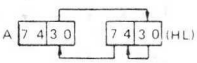
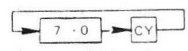
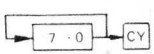
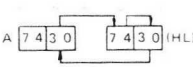
MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
INDR	(HL) ← (C) B ← B − 1 HL ← HL − 1 until B = 0	Load location (HL) with input from port (C), decrement HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 111 010
INI	(HL) ← (C) B ← B − 1 HL ← HL + 1	Load location (HL) with input from port (C); and increment HL and decrement B	2	16	•	↕③	X	X	1	X	11 101 101 10 100 010
INIR	(HL) ← (C) B ← B − 1 HL ← HL + 1 until B = 0	Load location (HL) with input from port (C), increment HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 110 010
JP (HL)	PC ← HL	Unconditional jump to (HL)	1	4	•	•	•	•	•	•	11 101 001
JP (IX)	PC ← IX	Unconditional jump to (IX)	2	8	•	•	•	•	•	•	11 011 101 11 101 001
JP (IY)	PC ← IY	Unconditional jump to (IY)	2	8	•	•	•	•	•	•	11 111 101 11 101 001
JP cc, nn	If cc true PC ← nn else continue	Jump to location nn if condition cc is true	3	10	•	•	•	•	•	•	11 ←cc→ 010Ⓗ nn nnn nnn nn nnn nnn
JP nn	PC ← nn	Unconditional jump to location nn	3	10	•	•	•	•	•	•	11 000 011 nn nnn nnn nn nnn nnn
JR C, e	If C = 0 continue If C = 1 PC ← PC + e	Jump relative to PC + e, if carry = 1	2	7 if condition met, 12, if not	•	•	•	•	•	•	00 111 000 ←e-2→
JR e	PC ← PC + e	Unconditional jump relative to PC + e	2	12	•	•	•	•	•	•	00 011 000 ←e-2→
JR NC, e	If C = 1 continue If C = 0 PC ← PC + e	Jump relative to PC + e if carry = 0	2	7	•	•	•	•	•	•	00 110 000 ←e-2→
JR NZ, e	If Z = 1 continue	Jump relative to PC + e if non-zero (Z = 0)	2	7	•	•	•	•	•	•	00 100 000 ←e-2→
JR Z, e	If Z = 0 continue	Jump relative to PC + e if zero (Z = 1)	2	7	•	•	•	•	•	•	00 101 000 ←e-2→
LD A, (BC)	A ← (BC)	Load ACC with location (BC)	1	7	•	•	•	•	•	•	00 001 010
LD A, (DE)	A ← (DE)	Load ACC with location (DE)	1	7	•	•	•	•	•	•	00 011 010
LD A, I	A ← I	Load ACC with I	2	9	•	↕	IFF	↕	0	0	11 101 101 01 010 111
LD A, (nn)	A ← (nn)	Load ACC with location nn	3	13	•	•	•	•	•	•	00 111 010 nn nnn nnn nn nnn nnn
LD A, R	A ← R	Load ACC with Reg. R	2	9	•	↕	IFF	↕	0	0	11 101 101 01 011 111
LD (BC), A	(BC) ← A	Load location (BC) with ACC	1	7	•	•	•	•	•	•	00 000 010
LD (DE), A	(DE) ← A	Load location (DE) with ACC	1	7	•	•	•	•	•	•	00 010 010
LD (HL), n	(HL) ← n	Load location (HL) with value n	2	10	•	•	•	•	•	•	00 110 110 nn nnn nnn
LD ss, nn	ss ← nn	Load Reg. pair ss with value nn	4	20	•	•	•	•	•	•	00 ss0 001Ⓐ nn nnn nnn nn nnn nnn
LD HL, (nn)	H ← (nn + 1) L ← (nn)	Load HL with location (nn)	3	16	•	•	•	•	•	•	00 101 010 nn nnn nnn nn nnn nnn
LD (HL), r	(HL) ← r	Load location (HL) with Reg. r	1	7	•	•	•	•	•	•	01 110 rrrⒷ
LD I, A	I ← A	Load I with ACC	2	9	•	•	•	•	•	•	11 101 101 01 000 111
LD IX, nn	IX ← nn	Load IX with value nn	4	19	•	•	•	•	•	•	11 011 101 00 100 001 nn nnn nnn nn nnn nnn
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	Load IX with location (nn)	4	20	•	•	•	•	•	•	11 011 101 00 101 010 nn nnn nnn nn nnn nnn
LD (IX + d), n	(IX + d) ← n	Load location (IX + d) with value n	4	19	•	•	•	•	•	•	11 011 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IX + d), r	(IX + d) ← r	Load location (IX + d) with Reg. r	3	19	•	•	•	•	•	•	11 011 101Ⓑ 01 110 rrr dd ddd ddd

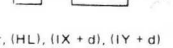
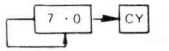
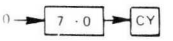
8

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
LD IY, nn	IY ← nn	Load IY with value nn	4	14	•	•	•	•	•	•	11 111 101 00 100 001 nn nnn nnn nn nnn nnn
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	Load IY with location (nn)	4	20	•	•	•	•	•	•	11 111 101 00 101 010 nn nnn nnn nn nnn nnn
LD ss, (nn)	ss_H ← (nn + 1) ss_L ← (nn)	Load Reg. pair dd with location (nn)	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss1 011 nn nnn nnn nn nnn nnn
LD (IY + d), n	(IY + d) ← n	Load (IY + d) with value n	4	19	•	•	•	•	•	•	11 111 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IY + d), r	(IY + d) ← r	Load location (IY + d) with Reg. r	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 110 rrr dd ddd ddd
LD (nn), A	(nn) ← A	Load location (nn) with ACC	3	13	•	•	•	•	•	•	00 110 010 nn nnn nnn nn nnn nnn
LD (nn), ss	(nn + 1) ← ss_H (nn) ← ss_L	Load location (nn) with Reg. pair dd	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss0 011 nn nnn nnn nn nnn nnn
LD (nn), HL	(nn + 1) ← H (nn) ← L	Load location (nn) with HL	3	16	•	•	•	•	•	•	00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	Load location (nn) with IX	4	20	•	•	•	•	•	•	11 011 101 00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	Load location (nn) with IY	4	20	•	•	•	•	•	•	11 111 101 00 100 010 nn nnn nnn nn nnn nnn
LD R, A	R ← A	Load R with ACC	2	9	•	•	•	•	•	•	11 101 101 01 001 111
LD r, (HL)	r ← (HL)	Load Reg. r with location (HL)	1	7	•	•	•	•	•	•	01 rrr 110 Ⓑ
LD r, (IX + d)	r ← (IX + d)	Load Reg. r with location (IX + d)	3	19	•	•	•	•	•	•	11 011 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, (IY + d)	r ← (IY + d)	Load Reg. r with location (IY + d)	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, n	r ← n	Load Reg. r with value n	2	7	•	•	•	•	•	•	00 rrr 110 Ⓑ nn nnn nnn
LD, r, r'	r ← r'	Load Reg. r with Reg. r	1	4	•	•	•	•	•	•	01 rrr rrr Ⓕ
LD SP, HL	SP ← HL	Load SP with HL	1	6	•	•	•	•	•	•	11 111 001
LD SP, IX	SP ← IX	Load SP with IX	2	10	•	•	•	•	•	•	11 011 101 11 111 001
LD SP, IY	SP ← IY	Load SP with IY	2	10	•	•	•	•	•	•	11 111 101 11 111 001
LDD	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1	Load location (DE) with location (HL), decrement DE, HL and BC	2	16	•	•	↕	•	0	0	11 101 101 10 101 000
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 until BC = 0	Load location (DE) with location (HL)	2	21	•	•	①	•	0	0	11 101 101 10 111 000
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1	Load location (DE) with location (HL), increment DE, HL; decrement BC	2	16	•	•	↕ ①	•	0	0	11 101 101 10 100 000
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1 until BC = 0	Load location (DE) with location (HL), increment DE, HL; decrement BC and repeat until BC = 0	2	21 if BC ≠ 0 16 if BC = 0	•	•	0	•	0	0	11 101 101 10 110 000
NEG	A ← 0 − A	Negate ACC (2's complement)	2	8	↕	↕	V	↕	1	↕	11 101 101 01 000 100

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
NOP		No operation	1	4	•	•	•	•	•	•	00 000 000
OR r	A ← A ∨ r	Logical 'OR' of Reg. r and ACC		4	0	↕	P	↕	0	↕	10 110 rrr (B)
OR n	A ← A ∨ n	Logical 'OR' of value n and ACC		7	•	↕	P	↕	0	↕	11 110 110 nn nnn nnn
OR (HL)	A ← A ∨ (HL)	Logical 'OR' of loc. (HL) and ACC		7	•	↕	P	↕	0	↕	10 110 110
OR (IX + d)	A ← (IX + d) ∨ A	Logical 'OR' of loc. (IX + d) ∨ ACC		19	•	↕	P	↕	0	↕	11 011 101 10 110 110 dd ddd ddd
OR (IY + d)	A ← A ∨ (IY + d)	Logical 'OR' of loc. (IY + d) ∨ ACC		19	•	↕	P	↕	0	↕	11 111 101 10 110 110 dd ddd ddd
OTDR	(C) ← (HL) B ← B − 1 HL ← HL − 1 until B = 0	Load output port (C) with contents of location (HL), decrement HL and B, repeat until B = 0	2	21 if B ≠ 0 16 if B = C	•	1	X	X	1	X	11 101 101 10 111 011
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 until B = 0	Load output port (C) with location (HL), increment HL, decrement B, repeat until B = 0	2	21 if B ≠ 0 16 if B = C	•	1	X	X	1	X	11 101 101 10 110 011
OUT (C), r	(C) ← r	Load output port (C) with Reg. r	2	12	•	•	•	•	•	•	11 101 101 (B) 01 rrr 001
OUT (n), A	(n) ← A	Load output port (n) with ACC	2	11	•	•	•	•	•	•	11 010 011 nn nnn nnn
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕ (3)	X	X	1	X	11 101 101 10 101 011
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕ (3)	X	X	1	X	11 101 101 10 100 011
POP IX	IX_H ← (SP + 1) IX_L ← (SP)	Load IX with top of stack	2	14	•	•	•	•	•	•	11 011 101 11 100 001
POP IY	IY_H ← (SP + 1) IY_L ← (SP)	Load IY with top of stack	2	14	•	•	•	•	•	•	11 111 101 11 100 001
POP qq	qq_H ← (SP + 1) qq_L ← (SP)	Load Reg. pair qq with top of stack	1	10	•	•	•	•	•	•	11 qq0 001 (G)
PUSH IX	(SP − 2) ← IX_L (SP − 1) ← IX_H	Load IX onto stack	2	15	•	•	•	•	•	•	11 011 101 11 100 101
PUSH IY	(SP − 2) ← IY_L (SP − 1) ← IY_H	Load IY onto stack	2	15	•	•	•	•	•	•	11 111 101 11 100 101
PUSH qq	(SP − 2) ← qq_L (SP − 1) ← qq_H	Load Reg. pair qq onto stack	1	11	•	•	•	•	•	•	11 qq0 101 (G)
RES b, r	S_b ← 0	Reset Bit b of Reg. r		8	•	•	•	•	•	•	11 001 011 (B) 10 bbb rrr (E)
RES b, (HL)	S_b ← 0, (HL)	Reset Bit b of loc. (HL)		15	•	•	•	•	•	•	11 001 011 10 bbb 110
RES b, (IX + d)	S_b ← 0, (IX + d)	Reset Bit b of loc. (IX + d)		23	•	•	•	•	•	•	11 011 101 11 001 011 dd ddd ddd 10 bbb 110
RES b, (IY + d)	S_b ← 0, (IY + d)	Reset Bit b of loc. (IY + d)		23	•	•	•	•	•	•	11 111 101 11 001 011 dd ddd ddd 10 bbb 110
RET	PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine	1	10	•	•	•	•	•	•	11 001 001
RET cc	If condition cc is false cont. else (PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine if condition cc is true	1	5 if CC false 11 if CC true	•	•	•	•	•	•	11 cc 000 (H)
RETI		Return from interrupt	2	14	•	•	•	•	•	•	11 101 101 01 001 101
RETN		Return from non-maskable interrupt	2	14	•	•	•	•	•	•	11 101 101 01 000 101
RL r		Rotate left through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 010 rrr
RL (HL)		Rotate left through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 010 110
RL (IX + d)		Rotate left through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 010 110
RL (IY + d)	m r, (HL), (IX + d), (IY + d), A	Rotate left through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 010 110
RLA		Rotate left ACC through carry	1	4	↕	•	•	•	0	0	00 010 111

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MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
RLC (HL)		Rotate location (HL) left circular	2	15	:	:	P	:	0	0	11 001 011 00 000 110
RLC (IX + d)		Rotate location (IX + d) left circular	4	23	:	:	P	:	0	0	11 011 101 11 001 011 dd ddd ddd 00 000 110
RLC (IY + d)	 m = r, (HL), (IX + d), (IY + d), A	Rotate location (IY + d) left circular	4	23	:	:	P	:	0	0	11 111 101 11 001 011 dd ddd ddd 00 000 110
RLC r		Rotate Reg. r left circular	2	8	:	:	P	:	0	0	11 001 011 (B) 00 000 rrr
RLCA		Rotate left circular ACC	1	4	:	•	•	•	0	0	00 000 111
RLD		Rotate digit left and right between ACC and location (HL)	2	18	•	:	P	:	0	0	11 101 101 01 101 111
RR r		Rotate right through carry Reg. r		2	:	:	P	:	0	0	11 001 011 (B) 00 011 rrr
RR (HL)		Rotate right through carry loc. (HL)		4	:	:	P	:	0	0	11 001 011 00 011 110
RR (IX + d)		Rotate right through carry loc. (IX + d)		6	:	:	P	:	0	0	11 011 101 11 001 011 dd ddd ddd 00 011 110
RR (IY + d)	 m = r, (HL), (IX + d), (IY + d), A	Rotate right through carry loc. (IY + d)		6	:	:	P	:	0	0	11 111 101 11 001 011 dd ddd ddd 00 011 110
RRA		Rotate right ACC through carry	1	4	:	•	•	•	0	0	00 011 111
RRC r		Rotate Reg. r right circular		2	:	:	P	:	0	0	11 001 011 (B) 00 001 rrr
RRC (HL)		Rotate loc. (HL) right circular		4	:	:	P	:	0	0	11 001 011 00 001 110
RRC (IX + d)		Rotate loc. (IX + d) right circular		6	:	:	P	:	0	0	11 011 101 11 001 011 dd ddd ddd 00 001 110
RRC (IY + d)	m = r, (HL), (IX + d), (IY + d), A	Rotate loc. (IY + d) right circular		6	:	:	P	:	0	0	11 111 101 11 001 011 dd ddd ddd 00 001 110
RRCA		Rotate right circular ACC	1	4	:	•	•	•	0	0	00 001 111
RRD		Rotate digit right and left between ACC and location (HL)	2	18	•	:	P	:	0	0	11 101 101 01 100 111
RST_t	(SP − 1) ← PC_H (SP − 2) ← PC_L PC_H ← 0, PC_L ← T	Restart to location T	1	11	•	•	•	•	•	•	11 ttt 111
SBC A, r	A ← A − r − CY	Subtract Reg. r from ACC w/carry	1	4	:	:	V	:	1	:	10 011 rrr (B)
SBC A, n	A ← A − n − CY	Subtract value n from ACC with carry		7	:	:	V	:	1	:	11 011 110 nn nnn nnn
SBC A, (HL)	A ← A − (HL) − CY	Sub. loc. (HL) from ACC w/carry		7	:	:	V	:	1	:	10 011 110
SBC A, (IX + d)	A ← A − (IX + d) − CY	Subtract loc. (IX + d) from ACC with carry		19	:	:	V	:	1	:	11 011 101 10 011 110 dd ddd ddd
SBC A, (IY + d)	A ← A − (IY + d) − CY	Subtract loc. (IY + d) from ACC with carry		19	:	:	V	:	1	:	11 111 101 10 011 110 dd ddd ddd
SBC HL, ss	HL ← HL − ss − CY	Subtract Reg. pair ss from HL with carry	2	15	:	:	V	:	1	X	11 101 101 (A) 01 ss0 010
SCF	CY ← 1	Set carry flag (C ← 1)	1	4	1	•	•	•	0	0	00 110 111
SET b, (HL)	$(HL)_b$ ← 1	Set Bit b of location (HL)	2	15	•	•	•	•	•	•	11 001 011 (E) 11 bbb 110
SET b, (IX + d)	$(IX + d)_b$ ← 1	Set Bit b of location (IX + d)	4	23	•	•	•	•	•	•	11 011 101 (E) 11 001 011 dd ddd ddd 11 bbb 110

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
SET b, (IY + d)	$(IY + d)_b \leftarrow 1$	Set Bit b of location (IY + d)	4	23	•	•	•	•	•	•	11 111 101 Ⓔ 11 001 011 dd ddd ddd 11 bbb 110
SET b, r	$r_b \leftarrow 1$	Set Bit b of Reg. r	2	8	•	•	•	•	•	•	11 001 011 Ⓑ 11 bbb rrr
SLA r		Shift Reg. r left arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 100 rrr
SLA (HL)		Shift loc. (HL) left arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 100 110
SLA (IX + d)		Shift loc. (IX + d) left arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 100 110
SLA (IY + d)	m = r, (HL), (IX + d), (IY + d)	Shift loc. (IY + d) left arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 100 110
SRA r		Shift Reg. r right arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 101 rrr
SRA (HL)		Shift loc. (HL) right arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 101 110
SRA (IX + d)		Shift loc. (IX + d) right arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 101 110
SRA (IY + d)	m = r, (HL), (IX + d), (IY + d)	Shift loc. (IY + d) right arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 101 110
SRL r		Shift Reg. r right logical		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 111 rrr
SRL (HL)		Shift loc. (HL) right logical		15	↕	↕	P	↕	0	0	11 001 011 00 111 110
SRL (IX + d)		Shift loc. (IX + d) right logical		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 111 110
SRL (IY + d)	m = r, (HL), (IX + d), (IY + d)	Shift loc. (IY + d) right logical		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 111 110
SUB r	A ← A − r	Subtract Reg. r from ACC		4	↕	↕	V	↕	1	↕	10 010 rrr Ⓑ
SUB n	A ← A − n	Subtract value n from ACC		7	↕	↕	V	↕	1	↕	11 010 110 nn nnn nnn
SUB (HL)	A ← A − (HL)	Subtract loc. (HL) from ACC		7	↕	↕	V	↕	1	↕	10 010 110
SUB (IX + d)	A ← A − (IX + d)	Subtract loc. (IX + d) from ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 010 110 dd ddd ddd
SUB (IY + d)	A ← A − (IY + d)	Subtract loc. (IY + d) from ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 010 110 dd ddd ddd
XOR r	A ← A∀r	Exclusive 'OR' Reg. r and ACC		4	↕	↕	P	↕	1	↕	10 101 rrr Ⓑ
XOR n	A ← A∀n	Exclusive 'OR' value n and ACC		7	↕	↕	P	↕	1	↕	11 101 110 nn nnn nnn
XOR (HL)	A ← A∀ (HL)	Exclusive 'OR' loc. (HL) and ACC		7	↕	↕	P	↕	1	↕	10 101 110
XOR (IX + d)	A ← A∀ (IX + d)	Exclusive 'OR' loc. (IX + d) and ACC		19	↕	↕	P	↕	1	↕	11 011 101 10 101 110 dd ddd ddd
XOR (IY + d)	A ← A∀ (IY + d)	Exclusive 'OR' loc. (IY + d) and ACC		19	↕	↕	P	↕	1	↕	11 111 101 10 101 110 dd ddd ddd

FLAG NOTES:

① P/V flag is 0 if B-1=0, else P/V=1

② Z=1 if A=(HL), else Z=0

③ If B-1=0, Z flag set, else reset

FLAG DEFINITIONS:

• = Flag not affected
0 = Flag reset
1 = Flag set
X = Flag unknown
↕ = Flag affected according to result of operation
V = Overflow set
P = Parity set
IFF = Interrupt flip-flop set

Ⓐ

Reg	ss
BC	00
DE	01
HL	10
SP	11

Ⓑ

Reg	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓒ

Reg	pp
BC	00
DE	01
IX	10
SP	11

Ⓓ

Reg	rr
BC	00
DE	01
IY	10
SP	11

Ⓔ

Bit	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Ⓕ

Reg	r,r'
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓖ

Reg	qq
BC	00
DE	01
HL	10
AF	11

Ⓗ

CC	Condition	Relevant Flag
000	NZ Non Zero	Z
001	Z Zero	Z
010	NC Non Carry	C
011	C Carry	C
100	PO Parity Odd	P/V
101	PE Parity Even	P/V
110	P Sign Positive	S
111	M Sign Negative	S

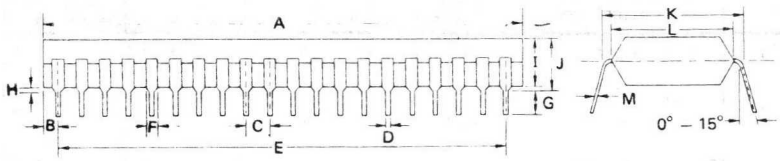
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Reg	r
B	000
C	001
D	010
E	011
H	100
L	101
F	110
A	111

FLAG DESCRIPTION:

C = Carry/Link
Z = Zero
P/V = Parity/Overflow
S = Sign
N = Add/Subtract
H = Half Carry

8



PACKAGE OUTLINE
μ PD780C
μ PD780-1C

(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

780/780-1DS-12-80-CAT

μPD8080AF 8-BIT N-CHANNEL MICROPROCESSOR FAMILY

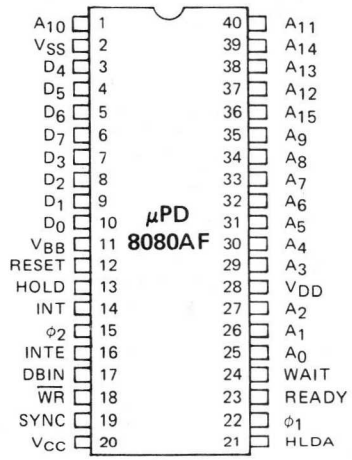
DESCRIPTION

The μPD8080AF is a complete 8-bit parallel processor for use in general purpose digital computer systems. It is fabricated on a single LSI chip using N-channel silicon gate MOS process, which offers much higher performance than conventional microprocessors (1.28 μs minimum instruction cycle). A complete microcomputer system is formed when the μPD8080AF is interfaced with I/O ports (up to 256 input and 256 output ports) and any type or speed of semiconductor memory. It is available in a 40 pin ceramic or plastic package.

FEATURES

- 78 Powerful Instructions
- Three Devices – Three Clock Frequencies
  μPD8080AF – 2.0 MHz
  μPD8080AF-2 – 2.5 MHz
  μPD8080AF-1 – 3.0 MHz
- Direct Access to 64K Bytes of Memory with 16-Bit Program Counter
- 256 8-Bit Input Ports and 256 8-Bit Output Ports
- Double Length Operations Including Addition
- Automatic Stack Memory Operation with 16-Bit Stack Pointer
- TTL Compatible (Except Clocks)
- Multi-byte Interrupt Capability
- **Fully** Compatible with Industry Standard 8080A
- Available in either Plastic or Ceramic Package

PIN CONFIGURATION



8

μPD8080AF

FUNCTIONAL DESCRIPTION

The μPD8080AF contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8080AF also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8080AF utilizes a 16-bit address bus to directly address 64K bytes of memory, is TTL compatible (1.9 mA), and utilizes the following addressing modes: Direct; Register; Register Indirect; and Immediate.

The μPD8080AF has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8080AF also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

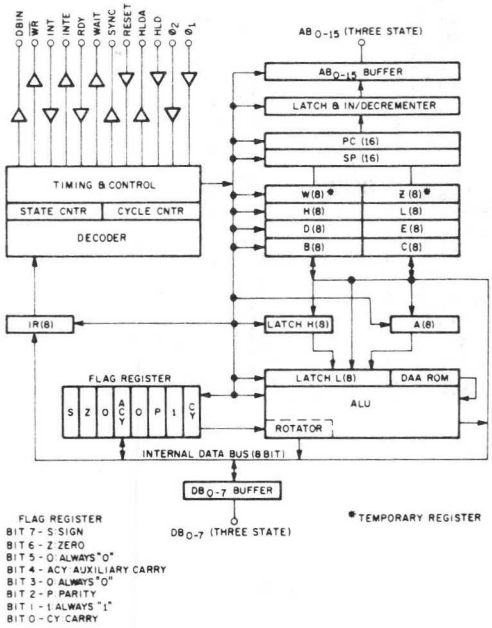
This processor is designed to greatly simplify system design. Separate 16-line address and 8-line bidirectional data buses are employed to allow direct interface to memories and I/O ports. Control signals, requiring no decoding, are provided directly by the processor. All buses, including the control bus, are TTL compatible.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the Hold Acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address and data lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data buses.

The μPD8080AF has the capability to accept a multiple byte instruction upon an interrupt. This means that a CALL instruction can be inserted so that any address in the memory can be the starting location for an interrupt program. This allows the assignment of a separate location for each interrupt operation, and as a result no polling is required to determine which operation is to be performed.

NEC offers three versions of the μPD8080AF. These processors have all the features of the μPD8080AF except the clock frequency ranges from 2.0 MHz to 3.0 MHz. These units meet the performance requirements of a variety of systems while maintaining software and hardware compatibility with other 8080A devices.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 25-27, 29-40	$A_{15} - A_0$	Address Bus (output three-state)	The address bus is used to address memory (up to 64K 8-bit words) or specify the I/O device number (up to 256 input and 256 output devices). A_0 is the least significant bit.
2	V_{SS}	Ground (input)	Ground
3-10	$D_7 - D_0$	Data Bus (input/output three-state)	The bidirectional data bus communicates between the processor, memory, and I/O devices for instructions and data transfers. During each sync time, the data bus contains a status word that describes the current machine cycle. D_0 is the least significant bit.
11	V_{BB}	V_{BB} Supply Voltage (input)	−5V ± 5%
12	RESET	Reset (input)	If the RESET signal is activated, the program counter is cleared. After RESET, the program starts at location 0 in memory. The INTE and HLDA flip-flops are also reset. The flags, accumulator, stack pointer, and registers are not cleared. (Note: External synchronization is not required for the RESET input signal which must be active for a minimum of 3 clock periods.)
13	HOLD	Hold (input)	HOLD requests the processor to enter the HOLD state. The HOLD state allows an external device to gain control of the μPD8080AF address and data buses as soon as the μPD8080AF has completed its use of these buses for the current machine cycle. It is recognized under the following conditions: • The processor is in the HALT state. • The processor is in the T_2 or T_W stage and the READY signal is active. As a result of entering the HOLD state, the ADDRESS BUS ($A_{15} - A_0$) and DATA BUS ($D_7 - D_0$) are in their high impedance state. The processor indicates its state on the HOLD ACKNOWLEDGE (HLDA) pin.
14	INT	Interrupt Request (input)	The μPD8080AF recognizes an interrupt request on this line at the end of the current instruction or while halted. If the μPD8080AF is in the HOLD state, or if the Interrupt Enable flip-flop is reset, it will not honor the request.
15	ϕ_2	Phase Two (input)	Phase two of processor clock.
16	INTE ①	Interrupt Enable (output)	INTE indicates the content of the internal interrupt enable flip-flop. This flip-flop is set by the Enable (EI) or reset by the Disable (DI) interrupt instructions and inhibits interrupts from being accepted by the processor when it is reset. INTE is automatically reset (disabling further interrupts) during T_1 of the instruction fetch cycle (M_1) when an interrupt is accepted and is also reset by the RESET signal.
17	DBIN	Data Bus In (output)	DBIN indicates that the data bus is in the input mode. This signal is used to enable the gating of data onto the μPD8080AF data bus from memory or input ports.
18	$\overline{WR}$	Write (output)	$\overline{WR}$ is used for memory WRITE or I/O output control. The data on the data bus is valid while the $\overline{WR}$ signal is active ($\overline{WR}$ = 0).
19	SYNC	Synchronizing Signal (output)	The SYNC signal indicates the beginning of each machine cycle.
20	V_{CC}	V_{CC} Supply Voltage (input)	+5V ± 5%
21	HLDA	Hold Acknowledge (output)	HLDA is in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at: • T_3 for READ memory or input operations. • The clock period following T_3 for WRITE memory or OUTPUT operations. In either case, the HLDA appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.
22	ϕ_1	Phase One (input)	Phase one of processor clock.
23	READY	Ready (input)	The READY signal indicates to the μPD8080AF that valid memory or input data is available on the μPD8080AF data bus. READY is used to synchronize the processor with slower memory or I/O devices. If after sending an address out, the μPD8080AF does not receive a high on the READY pin, the μPD8080AF enters a WAIT state for as long as the READY pin is low. (READY can also be used to single step the processor.)
24	WAIT	Wait (output)	The WAIT signal indicates that the processor is in a WAIT state.
28	V_{DD}	V_{DD} Supply Voltage (input)	+12V ± 5%

Note: ① After the EI instruction, the μPD8080AF accepts interrupts on the second instruction following the EI. This allows proper execution of the RET instruction if an interrupt operation is pending after the service routine.

μPD8080AF

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	-65°C to +150°C
Storage Temperature (Plastic Package)	-40°C to +125°C
All Output Voltages ①	-0.3 to +20 Volts
All Input Voltages ①	-0.3 to +20 Volts
Supply Voltages V_{CC}, V_{DD} and V_{SS} ①	-0.3 to +20 Volts
Power Dissipation	1.5W

Note: ① Relative to V_{BB}.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

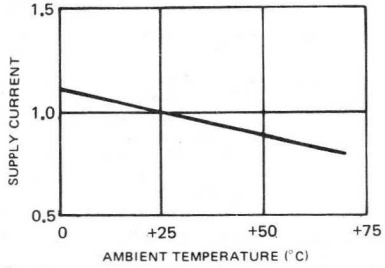
*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage	V_{ILC}	V_{SS} - 1		V_{SS} + 0.8	V	
Clock Input High Voltage	V_{IHC}	9.0		V_{DD} + 1	V	
Input Low Voltage	V_{IL}	V_{SS} - 1		V_{SS} + 0.8	V	
Input High Voltage	V_{IH}	3.3		V_{CC} + 1	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.9 mA on all outputs
Output High Voltage	V_{OH}	3.7			V	I_{OH} = − 150 μA ②
Avg. Power Supply Current (V_{DD})	$I_{DD(AV)}$		40	70	mA	t_{CY} min
Avg. Power Supply Current (V_{CC})	$I_{CC(AV)}$		60	80	mA	t_{CY} min
Avg. Power Supply Current (V_{BB})	$I_{BB(AV)}$		0.01	1	mA	t_{CY} min
Input Leakage	I_{IL}			±10 ②	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Clock Leakage	I_{CL}			±10 ②	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
Data Bus Leakage in Input Mode	I_{DL} ①			- 100 ②	μA	$V_{SS} \leq V_{IN} \leq V_{SS}$ + 0.8V
				-2 ②	mA	V_{SS} + 0.8V $\leq V_{IN} \leq V_{CC}$
Address and Data Bus Leakage During HOLD	I_{FL}			+10 ②	μA	$V_{ADDR/DATA} = V_{CC}$
				- 100 ②	μA	$V_{ADDR/DATA} = V_{SS}$ + 0.45V

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED ③



Notes: ① When DBIN is high and $V_{IN} > V_{IH}$ internal active pull-up resistors will be switched onto the data bus.
② Minus (−) designates current flow out of the device.
③ ΔI supply/ΔT_a = −0.45%/°C.

CAPACITANCE

T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V, V_{BB} = −5V.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ		17	25	pF	f_c = 1 MHz
Input Capacitance	C_{IN}		6	10	pF	Unmeasured Pins
Output Capacitance	C_{OUT}		10	20	pF	Returned to V_{SS}

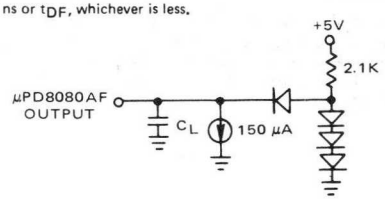
AC CHARACTERISTICS μPD8080AF

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.48		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
φ1 Pulse Width	$t_{\phi1}$	60			nsec	
φ2 Pulse Width	$t_{\phi2}$	220			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	70			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	80			nsec	
Address Output Delay From φ2	t_{DA} ②			200	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			220	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	30			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	150			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	120			nsec	
HOLD Setup Time to φ2	t_{HS}	140			nsec	
INT Setup Time During φ2 (During φ1 in Halt Mode)	t_{IS}	120			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

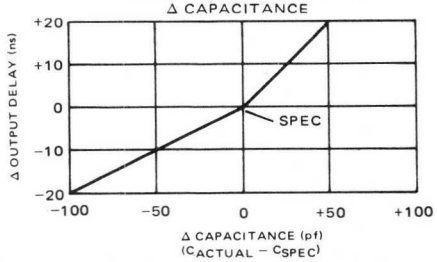
Notes: ① Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.

② Load Circuit.



③ Actual $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} > t_{CY}$ Min.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



8

AC CHARACTERISTICS
μPD8080AF-1

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.32		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		25	nsec	
φ1 Pulse Width	$t_{\phi1}$	50			nsec	
φ2 Pulse Width	$t_{\phi2}$	145			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	60			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	60			nsec	
Address Output Delay From φ2	t_{DA} ②			150	nsec	C_L = 50 pF
Data Output Delay From φ2	t_{DD} ②			180	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			110	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		130	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	10			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	120			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 50 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued:

④ The following are relevant when interfacing the μPD8080AF to devices having V_{IH} = 3.3V.

a. Maximum output rise time from 0.8V to 3.3V = 100 ns at C_L = SPEC.

b. Output delay when measured to 3.0V = SPEC +60 ns at C_L = SPEC.

c. If $C_L \neq$ SPEC, add 0.6 ns/pF if $C_L > C_{SPEC}$, subtract 0.3 ns/pF (from modified delay) if $C_L < C_{SPEC}$.

AC CHARACTERISTICS
μPD8080AF-2

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.38		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
φ1 Pulse Width	$t_{\phi1}$	60			nsec	
φ2 Pulse Width	$t_{\phi2}$	175			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	70			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	70			nsec	
Address Output Delay From φ2	t_{DA} ②			175	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			200	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	20			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	130			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued: ⑤

Device	t_{AW}
μPD8080AF	$2t_{CY} - t_{D3} - t_{r\phi2} - 140$
μPD8080AF-2	$2t_{CY} - t_{D3} - t_{r\phi2} - 130$
μPD8080AF-1	$2t_{CY} - t_{D3} - t_{r\phi2} - 110$

⑥

Device	t_{DW}
μPD8080AF	$t_{CY} - t_{D3} - t_{r\phi2} - 170$
μPD8080AF-2	$t_{CY} - t_{D3} - t_{r\phi2} - 170$
μPD8080AF-1	$t_{CY} - t_{D3} - t_{r\phi2} - 150$

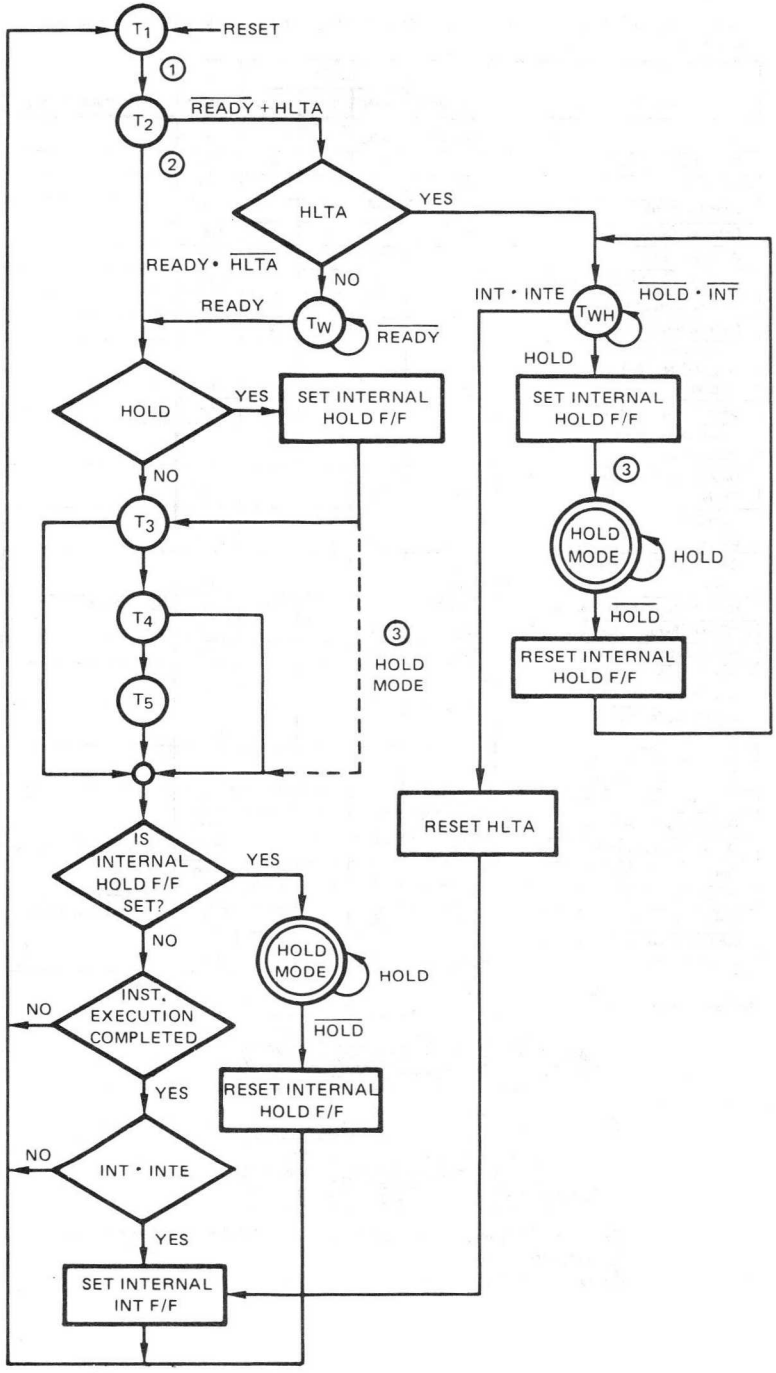
⑦ If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.

⑧ $t_{HF} = t_{D3} + t_{r\phi2} - 50$ ns.

⑨ $t_{WF} = t_{D3} + t_{r\phi2} - 10$ ns.

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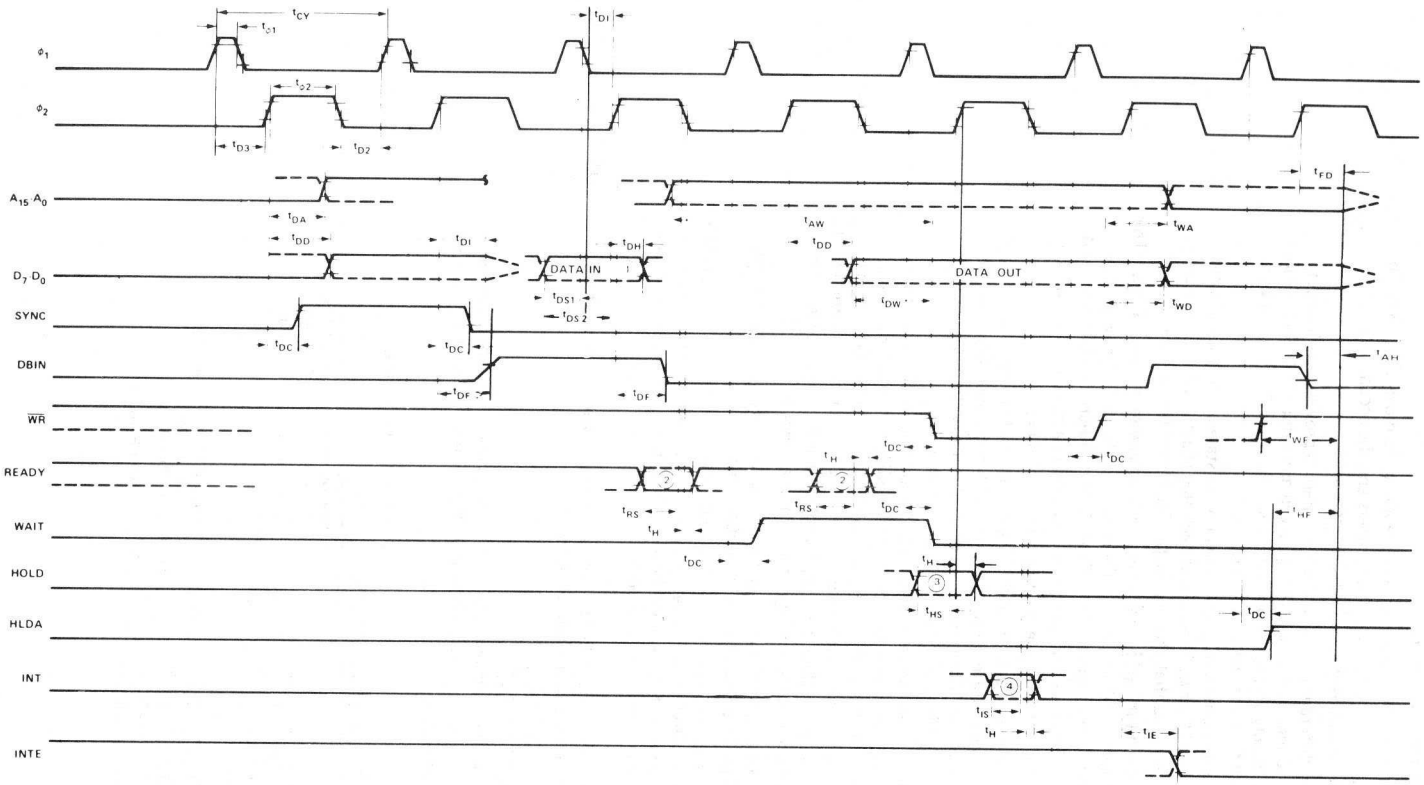
PROCESSOR STATE
TRANSITION DIAGRAM



Notes:
1. INTE F/F IS RESET IF INTERNAL INT F/F IS SET.
2. INTERNAL INT F/F IS RESET IF INTE F/F IS RESET.
3. IF REQUIRED, T_4 AND T_5 ARE COMPLETED SIMULTANEOUSLY WITH ENTERING HOLD STATE.

TIMING WAVEFORMS (5)

(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



Notes: (1) Data in must be stable for this period during DBIN • T_3. Both t_{DS1} and t_{DS2} must be satisfied.

(2) Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)

(3) Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)

(4) Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized in the following instruction. (External synchronization is not required.)

(5) This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

(6) Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.3V; "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.

INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (Sign, Zero, Parity and Carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table.)

The Sign flag is set (High) if bit 7 of the result is a "1"; otherwise it is reset (Low). The Zero flag is set if the result is "0"; otherwise it is reset. The Parity flag is set if the modulo 2 sum of the bits of the result is "0" (Even Parity); otherwise (Odd Parity) it is reset. The Carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the μPD8080AF has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the μPD8080AF. The ability to increment and decrement memory, the six general registers and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the μPD8080AF instruction set.

The special instruction group completes the μPD8080AF instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

DATA AND INSTRUCTION FORMATS

Data in the μPD8080AF is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB DATA WORD LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.

One Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2

TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable, or disable interrupt instructions

Immediate mode or I/O instructions

Jump, call or direct load and store instructions

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
MOVE														
MOV d,s	Move register to register	0	1	d	d	d	s	s	s	5				
MOV M,s	Move register to memory	0	1	1	1	0	s	s	s	7				
MOV d,M	Move memory to register	0	1	d	d	d	1	1	0	7				
MVI d,D8	Move immediate to register	0	0	d	d	d	1	1	0	7				
MVI M,D8	Move immediate to memory	0	0	1	1	0	1	1	0	10				
INCREMENT/DECREMENT														
INR d	Increment register	0	0	d	d	d	1	0	0	5	•	•	•	
DCR d	Decrement register	0	0	d	d	d	1	0	1	5	•	•	•	
INR M	Increment memory	0	0	1	1	0	1	0	0	10	•	•	•	
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	•	•	•	
ALU – REGISTER TO ACCUMULATOR														
ADD s	Add register to A	1	0	0	0	0	s	s	s	4	•	•	•	•
ADC s	Add register to A with carry	1	0	0	0	1	s	s	s	4	•	•	•	•
SUB s	Subtract register from A	1	0	0	1	0	s	s	s	4	•	•	•	•
SBB s	Subtract register from A with borrow	1	0	0	1	1	s	s	s	4	•	•	•	•
ANA s	AND register with A	1	0	1	0	0	s	s	s	4	•	•	•	0
XRA s	Exclusive OR Register with A	1	0	1	0	1	s	s	s	4	•	•	•	0
ORA s	OR register with A	1	0	1	1	0	s	s	s	4	•	•	•	0
CMP s	Compare register with A	1	0	1	1	1	s	s	s	4	•	•	•	•
ALU – MEMORY TO ACCUMULATOR														
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	•	•	•	•
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	•	•	•	•
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	•	•	•	•
ANA M	AND memory with A	1	0	1	0	0	1	1	0	7	•	•	•	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	7	•	•	•	0
ORA M	OR memory with A	1	0	1	1	0	1	1	0	7	•	•	•	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	•	•	•	•
ALU – IMMEDIATE TO ACCUMULATOR														
ADI D8	Add immediate to A	1	1	0	0	0	1	1	0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	•	•	•	•
SUI D8	Subtract immediate from A	1	1	0	1	0	1	1	0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	•	•	•	•
ANI D8	AND immediate with A	1	1	1	0	0	1	1	0	7	•	•	•	0
XRI D8	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	7	•	•	•	0
ORI D8	OR immediate with A	1	1	1	1	0	1	1	0	7	•	•	•	0
CPI D8	Compare immediate with A	1	1	1	1	1	1	1	0	7	•	•	•	•
ALU – ROTATE														
RLC	Rotate A left, MSB to carry (8-bit)	0	0	0	0	0	1	1	1	4				•
RRC	Rotate A right, LSB to carry (8-bit)	0	0	0	0	1	1	1	1	4				•
RAL	Rotate A left through carry (9-bit)	0	0	0	1	0	1	1	1	4				•
RAR	Rotate A right through carry (9-bit)	0	0	0	1	1	1	1	1	4				•
JUMP														
JMP ADDR	Jump unconditional	1	1	0	0	0	0	1	1	10				
JNZ ADDR	Jump on not zero	1	1	0	0	0	0	1	0	10				
JZ ADDR	Jump on zero	1	1	0	0	1	0	1	0	10				
JNC ADDR	Jump on no carry	1	1	0	1	0	0	1	0	10				
JC ADDR	Jump on carry	1	1	0	1	1	0	1	0	10				
JPO ADDR	Jump on parity odd	1	1	1	0	0	0	1	0	10				
JPE ADDR	Jump on parity even	1	1	1	0	1	0	1	0	10				
JP ADDR	Jump on positive	1	1	1	1	0	0	1	0	10				
JM ADDR	Jump on minus	1	1	1	1	1	0	1	0	10				
CALL														
CALL ADDR	Call unconditional	1	1	0	0	1	1	0	1	17				
CNZ ADDR	Call on not zero	1	1	0	0	0	1	0	0	11/17				
CZ ADDR	Call on zero	1	1	0	0	1	1	0	0	11/17				
CNC ADDR	Call on no carry	1	1	0	1	0	1	0	0	11/17				
CC ADDR	Call on carry	1	1	0	1	1	1	0	0	11/17				
CPO ADDR	Call on parity odd	1	1	1	0	0	1	0	0	11/17				
CPE ADDR	Call on parity even	1	1	1	0	1	1	0	0	11/17				
CP ADDR	Call on positive	1	1	1	1	0	1	0	0	11/17				
CM ADDR	Call on minus	1	1	1	1	1	1	0	0	11/17				
RETURN														
RET	Return	1	1	0	0	1	0	0	1	10				
RNZ	Return on not zero	1	1	0	0	0	0	0	0	5/11				
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11				
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11				
RC	Return on carry	1	1	0	1	1	0	0	0	5/11				
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11				
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11				
RP	Return on positive	1	1	1	1	0	0	0	0	5/11				
RM	Return on minus	1	1	1	1	1	0	0	0	5/11				

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR														
LXI B,D16	Load immediate register pair BC	0	0	0	0	0	0	0	1	10				
LXI D,D16	Load immediate register pair DE	0	0	0	1	0	0	0	1	10				
LXI H,D16	Load immediate register pair HL	0	0	1	0	0	0	0	1	10				
LXI SP,D16	Load immediate Stack Pointer	0	0	1	1	0	0	0	1	10				
PUSH														
PUSH B	Push register pair BC on stack	1	1	0	0	0	1	0	1	11				
PUSH D	Push register pair DE on stack	1	1	0	1	0	1	0	1	11				
PUSH H	Push register pair HL on stack	1	1	1	0	0	1	0	1	11				
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	11				
POP														
POP B	Pop register pair BC off stack	1	1	0	0	0	0	0	1	10				
POP D	Pop register pair DE off stack	1	1	0	1	0	0	0	1	10				
POP H	Pop register pair HL off stack	1	1	1	0	0	0	0	1	10				
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	•	•	•	•
DOUBLE ADD														
DAD B	Add BC to HL	0	0	0	0	1	0	0	1	10				•
DAD D	Add DE to HL	0	0	0	1	1	0	0	1	10				•
DAD H	Add HL to HL	0	0	1	0	1	0	0	1	10				•
DAD SP	Add Stack Pointer to HL	0	0	1	1	1	0	0	1	10				•
INCREMENT REGISTER PAIR														
INX B	Increment BC	0	0	0	0	0	0	1	1	5				
INX D	Increment DE	0	0	0	1	0	0	1	1	5				
INX H	Increment HL	0	0	1	0	0	0	1	1	5				
INX SP	Increment Stack Pointer	0	0	1	1	0	0	1	1	5				
DECREMENT REGISTER PAIR														
DCX B	Decrement BC	0	0	0	0	1	0	1	1	5				
DCX D	Decrement DE	0	0	0	1	1	0	1	1	5				
DCX H	Decrement HL	0	0	1	0	1	0	1	1	5				
DCX SP	Decrement Stack Pointer	0	0	1	1	1	0	1	1	5				
REGISTER INDIRECT														
STAX B	Store A at ADDR in BC	0	0	0	0	0	0	1	0	7				
STAX D	Store A at ADDR in DE	0	0	0	1	0	0	1	0	7				
LDAX B	Load A at ADDR in BC	0	0	0	0	1	0	1	0	7				
LDAX D	Load A at ADDR in DE	0	0	0	1	1	0	1	0	7				
DIRECT														
STA ADDR	Store A direct	0	0	1	1	0	0	1	0	13				
LDA ADDR	Load A direct	0	0	1	1	1	0	1	0	13				
SHLD ADDR	Store HL direct	0	0	1	0	0	0	1	0	16				
LHLD ADDR	Load HL direct	0	0	1	0	1	0	1	0	16				
MOVE REGISTER PAIR														
XCHG	Exchange DE and HL register pairs	1	1	1	0	1	0	1	1	4				
XTHL	Exchange top of stack and HL	1	1	1	0	0	0	1	1	18				
SPHL	HL to Stack Pointer	1	1	1	1	1	0	0	1	5				
PCHL	HL to Program Counter	1	1	1	0	1	0	0	1	5				
INPUT/OUTPUT														
IN A	Input	1	1	0	1	1	0	1	1	10				
OUT A	Output	1	1	0	1	0	0	1	1	10				
EI	Enable interrupts	1	1	1	1	1	0	1	1	4				
DI	Disable interrupts	1	1	1	1	0	0	1	1	4				
RST A	Restart	1	1	A	A	A	1	1	1	11				
MISCELLANEOUS														
CMA	Complement A	0	0	1	0	1	1	1	1	4				
STC	Set carry	0	0	1	1	0	1	1	1	4				1
CMC	Complement carry	0	0	1	1	1	1	1	1	4				$\overline{CY}$
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4	•	•	•	•
NOP	No operation	0	0	0	0	0	0	0	0	4				
HLT	Halt	0	1	1	1	0	1	1	0	7				

Notes:

[1] Operand Symbols used
A = 8-bit address or expression
s = source register
d = destination register
PSW = Processor Status Word
SP = Stack Pointer
D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
ADDR = 16-bit Memory address expression

[2] ddd or sss – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.

[3] Two possible cycle times (5/11) indicate instruction cycles dependent on condition flags.

[4] • = flag affected
– = flag not affected
0 = flag reset
1 = flag set

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INSTRUCTION CYCLE TIMES

One to five machine cycles (M_1 -- M_5) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$). During $\phi_1 \cdot$ SYNC of each machine cycle, a status word that identifies the type of machine cycle is available on the data bus.

Execution times and machine cycles used for each type of instruction are shown below.

INSTRUCTION	MACHINE CYCLES EXECUTED	CLOCK TIMES (MIN/MAX)
RST X and PUSH RP	PCR5 ① SPW3 ⑤ SPW3 ⑤	11
All CALL Instructions	PCR5 ① PCR3 ② PCR3 ② SPW3 ⑤ SPW3 ⑤	11/17
Conditional TURN Instructions	PCR5 ① SPR3 ④ SPR3 ④	5/11
RET Instruction	PCR4 ① SPR3 ④ SPR3 ④	10
XTHL	PCR4 ① SPR3 ④ SPR3 ④ SPW3 ⑤ SPW5 ⑤	18
DAD RP	PCR4 ① PCX3 ⓧ PCX3 ⓧ	10
INR R; INX RP, DCR R; DCX RP; PCHL; MOV R, R; SPHL	PCR5 ①	5
All JUMP Instructions and LXI RP	PCR4 ① PCR3 ② PCR3 ②	10
POP RP	PCR4 ① SPR3 ④ SPR3 ④	10
LDA	PCR4 ① PCR3 ② PCR3 ② BBR3 ②	13
STA	PCR4 ① PCR3 ② PCR3 ② BBW3 ③	13
LHLD	PCR4 ① PCR3 ② PCR3 ② BBR3 ② BBR3 ②	16
SHLD	PCR4 ① PCR3 ② PCR3 ② BBW3 ③ BBW3 ③	16
STAX B	PCR4 ① BCW3 ③	7
STAX D	PCR4 ① DEW3 ③	7
LDAX B	PCR4 ① BCR3 ②	7
LDAX D	PCR4 ① DER3 ②	7
MOV R, M; ADD M; ADC M; SUB M; SB B M; ANA M; XRA M; ORA M; CMP M	PCR4 ① HLR3 ②	7
INR M and DCR M	PCR4 ① HLR3 ② HLW3 ③	10
MVI M	PCR4 ① PCR3 ② HLW3 ③	10
MVI R; ADI; ACI; SUI; SBI; ANI; XRI; ORI; CPI	PCR4 ① PCR3 ②	7
MOV M, R	PCR4 ① HLW3 ③	7
EI; DI ADD R; ADC R; SUB R; SBB R; ANA R; XRA R; ORA R; CMP R; RLC; RRC; RAL; RAR; DAA; CMA; STC; CMC; NOP; XCHG	PCR4 ①	4
OUT	PCR4 ① PCR3 ② ABW3 ⑦	10
IN	PCR4 ① PCR3 ② ABR3 ⑥	10
HLT	PCR4 ① PCX3 ⑨	7

Machine Cycle Symbol Definition

XX Y Z (N)
- XX: Status word defining type of machine cycle (See Status Word Chart)
- Y: Number of clocks for this machine cycle
- Z: R = Read cycle – data into processor; W = Write cycle – data out of processor; X = No data transfer; PC = Program Counter used as address
- (N)

XX:
- HL = Registers H and L used as address
- BC = Registers B and C used as address
- DE = Registers D and E used as address
- SP = Stack Pointer used as address
- BB = Byte 2 and 3 used as address
- AB = Byte 2 used as address

Underlined (XXYZ(N)) indicates machine cycle is executed if condition is True.

STATUS INFORMATION DEFINITION

SYMBOLS	DATA BUS BIT	DEFINITION
INTA ①	D_0	Acknowledge signal for INTERRUPT request. Signal should be used to gate a restart or CALL instruction onto the data bus when DBIN is active.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function ($\overline{WO}$ = 0). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for HALT instruction.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{WR}$ is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instruction.
INP ①	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR ①	D_7	Designates that the data bus will be used for memory read data.

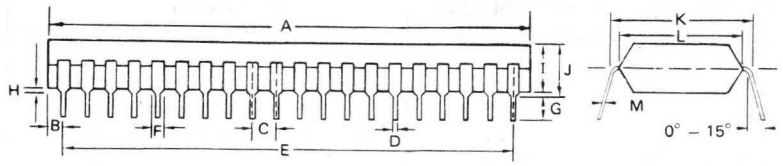
Note: ① These three status bits can be used to control the flow of data onto the μPD8080AF data bus.

STATUS WORD CHART

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	① INSTRUCTION FETCH	② MEMORY READ	③ MEMORY WRITE	④ STACK READ	⑤ STACK WRITE	⑥ INPUT READ	⑦ OUTPUT WRITE	⑧ INTERRUPT ACKNOWLEDGE	⑨ HALT ACKNOWLEDGE	⑩ INT. ACK. WHILE HALT
											← Ⓝ STATUS WORD
D_0	INTA	0	0	0	0	0	0	1	0	1	
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

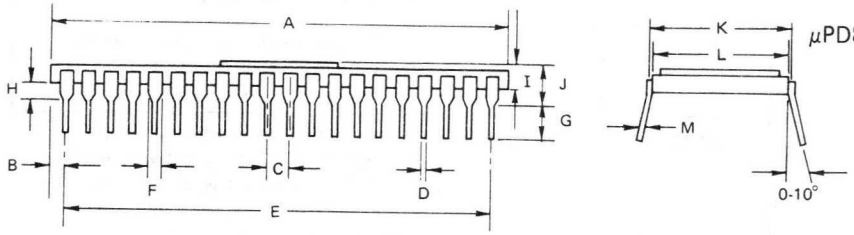
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PACKAGE OUTLINE
μPD8080AFC

(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.028 MAX.
B	1.62 MAX.	0.064 MAX.
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.2 MIN.	0.047 MIN.
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.019 MIN.
I	5.22 MAX.	0.206 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24 TYP.	0.600 TYP.
L	13.2 TYP.	0.520 TYP.
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



μPD8080AFD

(CERAMIC)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.03 MAX.
B	1.62 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.0019

μPD8085A SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

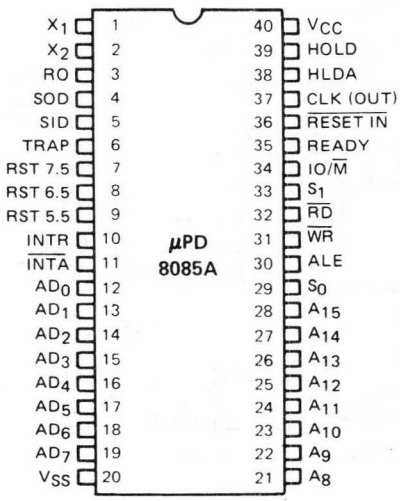
DESCRIPTION

The μPD8085A is a single chip 8-bit microprocessor which is 100 percent software compatible with the industry standard 8080A. It has the ability of increasing system performance of the industry standard 8080A by operating at a higher speed. Using the μPD8085A in conjunction with its family of ICs allows the designer complete flexibility with minimum chip count.

FEATURES

- Single Power Supply: +5 Volt, ±10%
- Internal Clock Generation and System Control
- Internal Serial In/Out Port.
- Fully TTL Compatible
- Internal 4-Level Interrupt Structure
- Multiplexed Address/Data Bus for Increased System Performance
- Complete Family of Components for Design Flexibility
- Software Compatible with Industry Standard 8080A
- Higher Throughput: μPD8085A – 3 MHz
  μPD8085A-2 – 5 MHz
- Available in Either Plastic or Ceramic Package

PIN CONFIGURATION



8

FUNCTIONAL DESCRIPTION

The μPD8085A contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8085A also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8085A has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8085A also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

The μPD8085A was designed with speed and simplicity of the overall system in mind. The multiplexed address/data bus increases available pins for advanced functions in the processor and peripheral chips while providing increased system speed and less critical timing functions. All signals to and from the μPD8085A are fully TTL compatible.

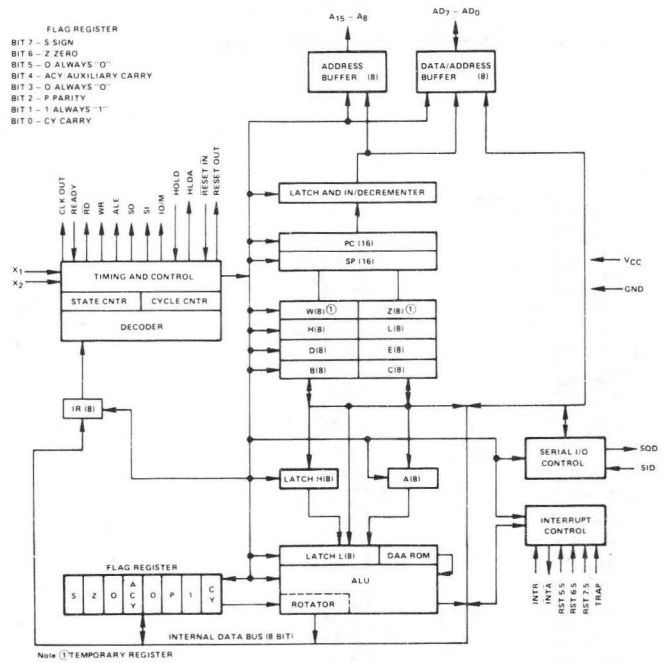
The internal interrupt structure of the μPD8085A features 4 levels of prioritized interrupt with three levels internally maskable.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the Hold Acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address, data and control lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data busses.

The μPD8085A features internal clock generation with status outputs available for advanced read/write timing and memory/IO instruction indications. The clock may be crystal controlled, RC controlled, or driven by an external signal.

On chip serial in/out port is available and controlled by the newly added RIM and SIM instructions.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 2	X_1, X_2	Crystal In	Crystal, RC, or external clock input
3	RO	Reset Out	Acknowledge that the processor is being reset to be used as a system reset
4	SOD	Serial Out Data	1-bit data out by the SIM instruction
5	SID	Serial In Data	1-bit data into ACC bit 7 by the RIM instruction
6	Trap	Trap Interrupt Input	Highest priority nonmaskable restart interrupt
7 8 9	RST 7.5 RST 6.5 RST 5.5	Restart Interrupts	Priority restart interrupt inputs, of which 7.5 is the highest and 5.5 the lowest priority
10	INTR	Interrupt Request In	A general interrupt input which stops the PC from incrementing, generates $\overline{INTA}$, and samples the data bus for a restart or call instruction
11	$\overline{INTA}$	Interrupt Acknowledge	An output which indicates that the processor has responded to INTR
12-19	$AD_0 - AD_7$	Low Address/Data Bus	Multiplexed low address and data bus
20	V_{SS}	Ground	Ground Reference
21-28	$A_8 - A_{15}$	High Address Bus	Nonmultiplexed high 8-bits of the address bus
29, 33	S_0, S_1	Status Outputs	Outputs which indicate data bus status: Halt, Write, Read, Fetch
30	ALE	Address Latch Enable Out	A signal which indicates that the lower 8-bits of address are valid on the AD lines
31, 32	$\overline{WR}$, $\overline{RD}$	Write/Read Strobes Out	Signals out which are used as write and read strobes for memory and I/O devices
34	IO/$\overline{M}$	I/O or Memory Indicator	A signal out which indicates whether $\overline{RD}$ or $\overline{WR}$ strobes are for I/O or memory devices
35	Ready	Ready Input	An input which is used to increase the data and address bus access times (can be used for slow memory)
36	$\overline{Reset\ In}$	Reset Input	An input which is used to start the processor activity at address 0, resetting IE and HLDA flip-flops
37	CLK	Clock Out	System Clock Output
38, 39	HLDA, HOLD	Hold Acknowledge Out and Hold Input Request	Used to request and indicate that the processor should relinquish the bus for DMA activity. When hold is acknowledged, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, Address and Data busses are all 3-stated.
40	V_{CC}	5V Supply	Power Supply Input

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
(Plastic Package)	−40°C to +125°C
All Output Voltages	−0.3 to +7 Volts
All Input Voltages	−0.3 to +7 Volts
Supply Voltage V_{CC}	−0.3 to +7 Volts
Power Dissipation	1.5W

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ± 10%, V_{SS} = GND, unless otherwise specified

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	V_{SS} − 0.5		V_{SS} + 0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA on all outputs
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μs ①
Power Supply Current (V_{CC})	I_{CC} (AV)			170	mA	t_{CY} min
Input Leakage	I_{IL}			±10 ①	μA	V_{IN} = V_{CC}
Output Leakage	I_{LO}			±10 ①	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
Input Low Level, Reset	V_{ILR}	−0.5		+0.8	V	
Input High Level, Reset	V_{IHR}	2.4		V_{CC} + 0.5	V	
Hysteresis, Reset	V_{HY}	0.25			V	

Note: ① Minus (−) designates current flow out of the device.

AC CHARACTERISTICS

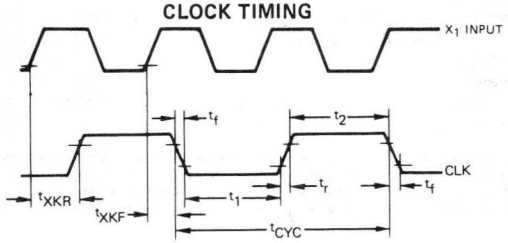
T_a = 0°C to + 70°C; V_{CC} = 5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS μPD8085A MIN	LIMITS μPD8085A MAX	LIMITS μPD8085A-2 MIN	LIMITS μPD8085A-2 MAX	UNIT	TEST CONDITIONS
CLK Cycle Period	T_{CYC}	320	2000	200	2000	ns	
CLK Low Time	t_1	80		40		ns	
CLK High Time	t_2	120		70		ns	
CLK Rise and Fall Time	t_r, t_f		30		30	ns	T_{CYC} = 320 ns
Address Valid Before Trailing Edge of ALE	t_{AL}	110		50		ns	C_L = 150 pF
Address Hold Time After ALE	t_{LA}	100		50		ns	
ALE Width	t_{LL}	140		80		ns	
ALE Low During CLK High	t_{LCK}	100		50		ns	Output Voltages
Training Edge of ALE to Leading Edge of Control	t_{LC}	130		60		ns	V_L = 0.8 Volts V_H = 2.0 Volts
Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)	t_{AFR}		0		0	ns	
Valid Address to Valid Data In	t_{AD}		575		350	ns	Input Voltages
$\overline{READ}$ (or $\overline{INTA}$) to Valid Data	t_{RD}		300		150	ns	V_L = 0.8 Volts
Data Hold Time After $\overline{READ}$ ($\overline{INTA}$)	t_{RDH}	0		0		ns	V_H = 1.5 Volts at
Training Edge of READ to Re-Enabling of Address	t_{RAE}	150		90		ns	20 ns rise and fall times
Address (A_8-A_{15}) Valid After Control ①	t_{CA}	120		60		ns	For outputs where
Data Valid to Training Edge of $\overline{WRITE}$	t_{DW}	420		230		ns	C_L = 150 pf, correct
Data Valid After Training Edge of $\overline{WRITE}$	t_{WD}	100		60		ns	as follows:
Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	t_{CC}	400		230		ns	25 pf ⩽ CL < 150 pf −0.10 ns/pf
Training Edge of Control to Leading Edge of ALE	t_{CL}	50		25		ns	
READY Valid from Address Valid	t_{ARY}		220		100	ns	150 pf < CL ⩽
READY Setup Time to Leading Edge of CLK	t_{RYS}	110		100		ns	300 pf + 0.30 ns/pf
READY Hold Time	t_{RYH}	0		0		ns	
HLDA Valid to Training Edge of CLK	t_{HACK}	110		40		ns	Outputs measured
Bus Float After HLDA	t_{HABF}		210		150	ns	with only
HLDA to Bus Enable	t_{HABE}		210		150	ns	capacitive load
ALE to Valid Data In	t_{LDR}		460		270	ns	
Control Training Edge to Leading Edge of Next Control	t_{RV}	400		220		ns	
Address Valid to Leading Edge of Control	t_{AC}	270		115		ns	
HOLD Setup Time to Training Edge of CLK	t_{HDS}	170		120		ns	
HOLD Hold Time	t_{HDH}	0		0		ns	
INTR Setup Time to Leading Edge of CLK (M1, T1 only). Also RST and TRAP	t_{INS}	160		150		ns	
INTR Hold Time	t_{INH}	0		0		ns	
X_1 Falling to CLK Rising	t_{XKR}	30	120	30	100	ns	
X_1 Falling to CLK Falling	t_{XKF}	30	150	30	110	ns	
Leading Edge of Write to Data Valid	t_{WDL}		40		20		

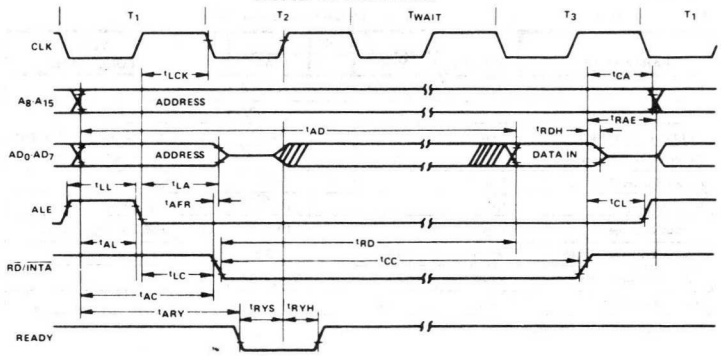
Note: ① IO/$\overline{M}$, SO, SI

TIMING WAVEFORMS

CLOCK TIMING

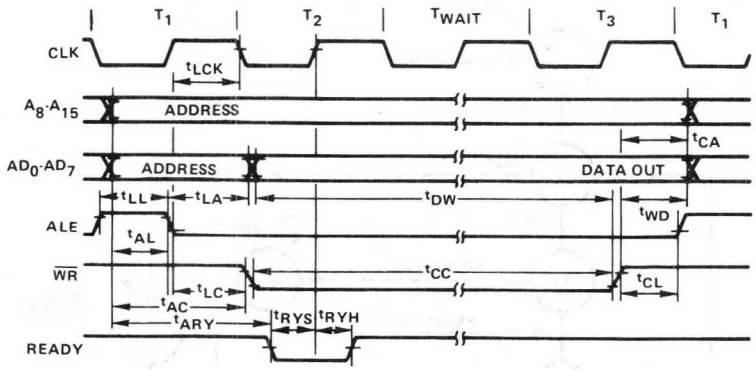


READ OPERATION

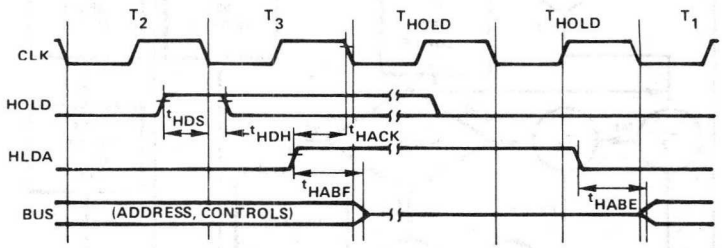


TIMING WAVEFORMS (CONT.)

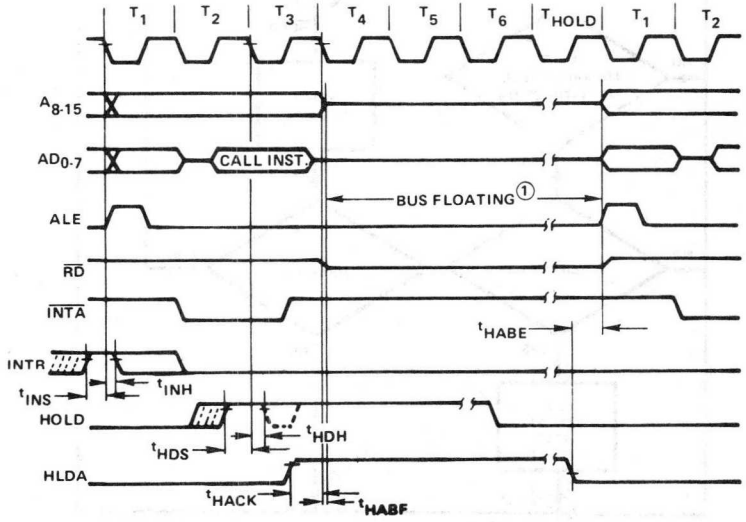
WRITE OPERATION



HOLD OPERATION

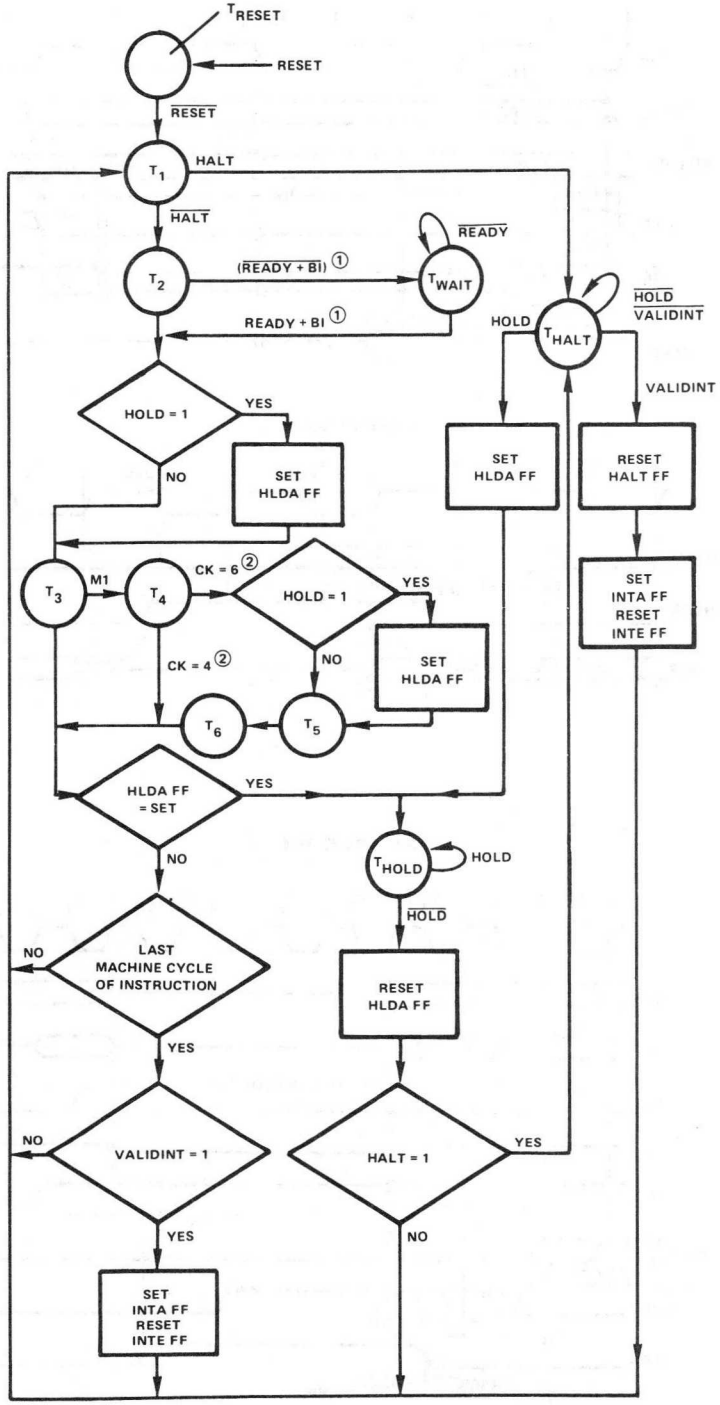


INTERRUPT TIMING



Note: ① IO/$\overline{M}$ is also floating during this time.

PROCESSOR STATE TRANSITION DIAGRAM



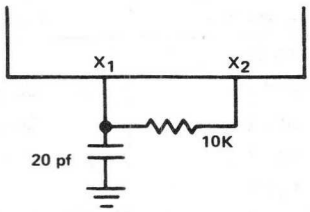
Notes: ① BI indicates that the bus is idle during this machine cycle.

② CK indicates the number of clock cycles in this machine cycle.

CLOCK INPUTS ①

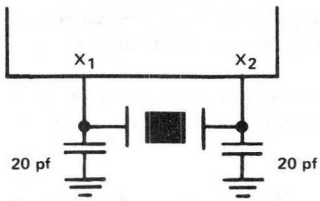
As stated, the timing for the μPD8085A may be generated in one of three ways; crystal, RC, or external clock. Recommendations for these methods are shown below.

RC



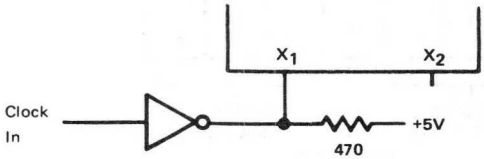
≈3 MHz Input Frequency
RC Resonance

CRYSTAL

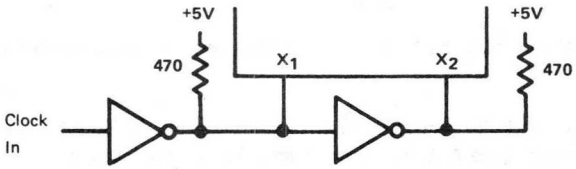


1-6 MHz Input Frequency
Parallel Resonant Crystal

EXTERNAL



1-6 MHz 25-50% DC
X_2 not used



1-6 MHz > 50% DC

Note: ① Input frequency must be twice the internal operating frequency.

STATUS OUTPUTS

The Status Outputs are valid during ALE time and have the following meaning:

	S1	S0
Halt	0	0
Write	0	1
Read	1	0
Fetch	1	1

These pins may be decoded to portray the processor's data bus status.

INTERRUPTS

The μPD8085A has five interrupt pins available to the user. INTR is operationally the same as the 8080 interrupt request, three (3) internally maskable restart interrupts: RESTART 5.5, 6.5 and 7.5, and TRAP, a nonmaskable restart.

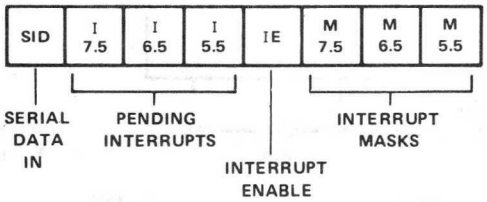
PRIORITY	INTERRUPT	RESTART ADDRESS
Highest	TRAP	24_{16}
|	RST 7.5	$3C_{16}$
|	RST 6.5	34_{16}
|	RST 5.5	$2C_{16}$
Lowest	INTR	

INTR, RST 5.5 and RST 6.5 are all level sensing inputs while RST 7.5 is set on a rising edge. TRAP, the highest priority interrupt, is nonmaskable and is set on the rising edge or positive level. It must make a low to high transition and remain high to be seen, but it will not be generated again until it makes another low to high transition.

SERIAL I/O

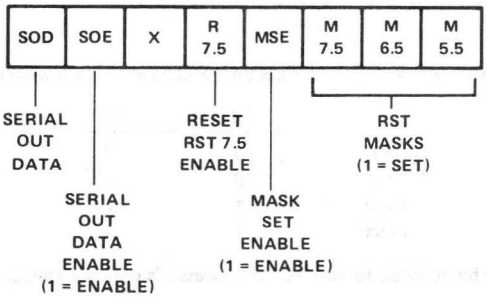
Serial input and output is accomplished with two new instructions not included in the 8080: RIM and SIM. These instructions serve several purposes: serial I/O, and reading or setting the interrupt mask.

The RIM (Read Interrupt Mask) instruction is used for reading the interrupt mask and for reading serial data. After execution of the RIM instruction the ACC content is as follows:



Note: After the TRAP interrupt, the RIM instruction must be executed to preserve the status of IE.

The SIM (Set Interrupt Mask) instruction is used to program the interrupt mask and to output serial data. Presetting the ACC for the SIM instruction has the following meaning:



INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also, the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (Sign, Zero, Parity and Carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table.)

The Sign flag is set (High) if bit 7 of the result is "1"; otherwise it is reset (Low). The Zero flag is set if the result is "0"; otherwise it is reset. The Parity flag is set if the modulo 2 sum of the bits of the result is "0" (Even Parity); otherwise (Odd Parity) it is reset. The Carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the μPD8085A has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the μPD8085A. The ability to increment and decrement memory, the six general registers and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

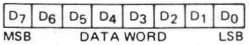
Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the μPD8085A instruction set.

Two instructions, RIM and SIM, are used for reading and setting the internal interrupt mask as well as input and output to the serial I/O port.

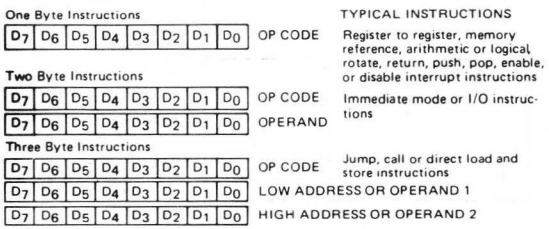
The special instruction group completes the μPD8085A instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

DATA AND INSTRUCTION FORMATS

Data in the μPD8085A is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:



Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.



INSTRUCTION SET TABLE

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
MOVE														
MOV d,s	Move register to register	0	1	d	d	d	s	s	s	4				
MOV M,s	Move register to memory	0	1	1	1	0	s	s	s	7				
MOV d,M	Move memory to register	0	1	d	d	d	1	1	0	7				
MVI d,D8	Move immediate to register	0	0	d	d	d	1	1	0	7				
MVI M,D8	Move immediate to memory	0	0	1	1	0	1	1	0	10				
INCREMENT/DECREMENT														
INR d	Increment register	0	0	d	d	d	1	0	0	4	•	•	•	
DCR d	Decrement register	0	0	d	d	d	1	0	1	4	•	•	•	
INR M	Increment memory	0	0	1	1	0	1	0	0	10	•	•	•	
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	•	•	•	
ALU – REGISTER TO ACCUMULATOR														
ADD s	Add register to A	1	0	0	0	0	s	s	s	4	•	•	•	•
ADC s	Add register to A with carry	1	0	0	0	1	s	s	s	4	•	•	•	•
SUB s	Subtract register from A	1	0	0	1	0	s	s	s	4	•	•	•	•
SBB s	Subtract register from A with borrow	1	0	0	1	1	s	s	s	4	•	•	•	•
ANA s	AND register with A	1	0	1	0	0	s	s	s	4	•	•	•	0
XRA s	Exclusive OR Register with A	1	0	1	0	1	s	s	s	4	•	•	•	0
ORA s	OR register with A	1	0	1	1	0	s	s	s	4	•	•	•	0
CMP s	Compare register with A	1	0	1	1	1	s	s	s	4	•	•	•	•
ALU – MEMORY TO ACCUMULATOR														
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	•	•	•	•
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	•	•	•	•
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	•	•	•	•
ANA M	AND memory with A	1	0	1	0	0	1	1	0	7	•	•	•	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	7	•	•	•	0
ORA M	OR memory with A	1	0	1	1	0	1	1	0	7	•	•	•	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	•	•	•	•
ALU – IMMEDIATE TO ACCUMULATOR														
ADI D8	Add immediate to A	1	1	0	0	0	1	1	0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	•	•	•	•
SUI D8	Subtract immediate from A	1	1	0	1	0	1	1	0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	•	•	•	•
ANI D8	AND immediate with A	1	1	1	0	0	1	1	0	7	•	•	•	0
XRI D8	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	7	•	•	•	0
ORI D8	OR immediate with A	1	1	1	1	0	1	1	0	7	•	•	•	0
CPI D8	Compare immediate with A	1	1	1	1	1	1	1	0	7	•	•	•	•
ALU – ROTATE														
RLC	Rotate A left, MSB to carry (8-bit)	0	0	0	0	0	1	1	1	4				•
RRC	Rotate A right, LSB to carry (8-bit)	0	0	0	0	1	1	1	1	4				•
RAL	Rotate A left through carry (9-bit)	0	0	0	1	0	1	1	1	4				•
RAR	Rotate A right through carry (9-bit)	0	0	0	1	1	1	1	1	4				•
JUMP														
JMP ADDR	Jump unconditional	1	1	0	0	0	0	1	1	10				
JNZ ADDR	Jump on not zero	1	1	0	0	0	0	1	0	7/10				
JZ ADDR	Jump on zero	1	1	0	0	1	0	1	0	7/10				
JNC ADDR	Jump on no carry	1	1	0	1	0	0	1	0	7/10				
JC ADDR	Jump on carry	1	1	0	1	1	0	1	0	7/10				
JPO ADDR	Jump on parity odd	1	1	1	0	0	0	1	0	7/10				
JPE ADDR	Jump on parity even	1	1	1	0	1	0	1	0	7/10				
JP ADDR	Jump on positive	1	1	1	1	0	0	1	0	7/10				
JM ADDR	Jump on minus	1	1	1	1	1	0	1	0	7/10				
CALL														
CALL ADDR	Call unconditional	1	1	0	0	1	1	0	1	18				
CNZ ADDR	Call on not zero	1	1	0	0	0	1	0	0	9/18				
CZ ADDR	Call on zero	1	1	0	0	1	1	0	0	9/18				
CNC ADDR	Call on no carry	1	1	0	1	0	1	0	0	9/18				
CC ADDR	Call on carry	1	1	0	1	1	1	0	0	9/18				
CPO ADDR	Call on parity odd	1	1	1	0	0	1	0	0	9/18				
CPE ADDR	Call on parity even	1	1	1	0	1	1	0	0	9/18				
CP ADDR	Call on positive	1	1	1	1	0	1	0	0	9/18				
CM ADDR	Call on minus	1	1	1	1	1	1	0	0	9/18				
RETURN														
RET	Return	1	1	0	0	1	0	0	1	10				
RNZ	Return on not zero	1	1	0	0	0	0	0	0	6/12				
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12				
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12				
RC	Return on carry	1	1	0	1	1	0	0	0	6/12				
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12				
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12				
RP	Return on positive	1	1	1	1	0	0	0	0	6/12				
RM	Return on minus	1	1	1	1	1	0	0	0	6/12				

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR														
LXI B,D16	Load immediate register pair BC	0	0	0	0	0	0	0	1	10				
LXI D,D16	Load immediate register pair DE	0	0	0	1	0	0	0	1	10				
LXI H,D16	Load immediate register pair HL	0	0	1	0	0	0	0	1	10				
LXI SP,D16	Load immediate Stack Pointer	0	0	1	1	0	0	0	1	10				
PUSH														
PUSH B	Push register pair BC on stack	1	1	0	0	0	1	0	1	12				
PUSH D	Push register pair DE on stack	1	1	0	1	0	1	0	1	12				
PUSH H	Push register pair HL on stack	1	1	1	0	0	1	0	1	12				
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	12				
POP														
POP B	Pop register pair BC off stack	1	1	0	0	0	0	0	1	10				
POP D	Pop register pair DE off stack	1	1	0	1	0	0	0	1	10				
POP H	Pop register pair HL off stack	1	1	1	0	0	0	0	1	10				
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	•	•	•	•
DOUBLE ADD														
DAD B	Add BC to HL	0	0	0	0	1	0	0	1	10				•
DAD D	Add DE to HL	0	0	0	1	1	0	0	1	10				•
DAD H	Add HL to HL	0	0	1	0	1	0	0	1	10				•
DAD SP	Add Stack Pointer to HL	0	0	1	1	1	0	0	1	10				•
INCREMENT REGISTER PAIR														
INX B	Increment BC	0	0	0	0	0	0	1	1	6				
INX D	Increment DE	0	0	0	1	0	0	1	1	6				
INX H	Increment HL	0	0	1	0	0	0	1	1	6				
INX SP	Increment Stack Pointer	0	0	1	1	0	0	1	1	6				
DECREMENT REGISTER PAIR														
DCX B	Decrement BC	0	0	0	0	1	0	1	1	6				
DCX D	Decrement DE	0	0	0	1	1	0	1	1	6				
DCX H	Decrement HL	0	0	1	0	1	0	1	1	6				
DCX SP	Decrement Stack Pointer	0	0	1	1	1	0	1	1	6				
REGISTER INDIRECT														
STAX B	Store A at ADDR in BC	0	0	0	0	0	0	1	0	7				
STAX D	Store A at ADDR in DE	0	0	0	1	0	0	1	0	7				
LDAX B	Load A at ADDR in BC	0	0	0	0	1	0	1	0	7				
LDAX D	Load A at ADDR in DE	0	0	0	1	1	0	1	0	7				
DIRECT														
STA ADDR	Store A direct	0	0	1	1	0	0	1	0	13				
LDA ADDR	Load A direct	0	0	1	1	1	0	1	0	13				
SHLD ADDR	Store HL direct	0	0	1	0	0	0	1	0	16				
LHLD ADDR	Load HL direct	0	0	1	0	1	0	1	0	16				
MOVE REGISTER PAIR														
XCHG	Exchange DE and HL register pairs	1	1	1	0	1	0	1	1	4				
XTHL	Exchange top of stack and HL	1	1	1	0	0	0	1	1	16				
SPHL	HL to Stack Pointer	1	1	1	1	1	0	0	1	6				
PCHL	HL to Program Counter	1	1	1	0	1	0	0	1	6				
INPUT/OUTPUT														
IN A	Input	1	1	0	1	1	0	1	1	10				
OUT A	Output	1	1	0	1	0	0	1	1	10				
EI	Enable interrupts	1	1	1	1	1	0	1	1	4				
DI	Disable interrupts	1	1	1	1	0	0	1	1	4				
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4				
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4				
RST A	Restart	1	1	A	A	A	1	1	1	12				
MISCELLANEOUS														
CMA	Complement A	0	0	1	0	1	1	1	1	4				
STC	Set carry	0	0	1	1	0	1	1	1	4				1 (Cy)
CMC	Complement carry	0	0	1	1	1	1	1	1	4				
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4	•	•	•	•
NOP	No operation	0	0	0	0	0	0	0	0	4				
HLT	Halt	0	1	1	1	0	1	1	0	5				

Notes:

[1] Operand Symbols used
- A = 8-bit address or expression
- s = source register
- d = destination register
- PSW = Processor Status Word
- SP = Stack Pointer
- D8 = 8-bit data quantity, expression, or constant, always 8_2 of instruction
- D16 = 16-bit data quantity, expression, or constant, always $8_3 8_2$ of instruction
- ADDR = 16-bit Memory address expression

[2] ddd or sss – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A

[3] Two possible cycle times (7/10) indicate instruction cycles dependent on condition flags.

[4] • = flag affected
- = flag not affected
0 = flag reset
1 = flag set

INSTRUCTION CYCLE TIMES

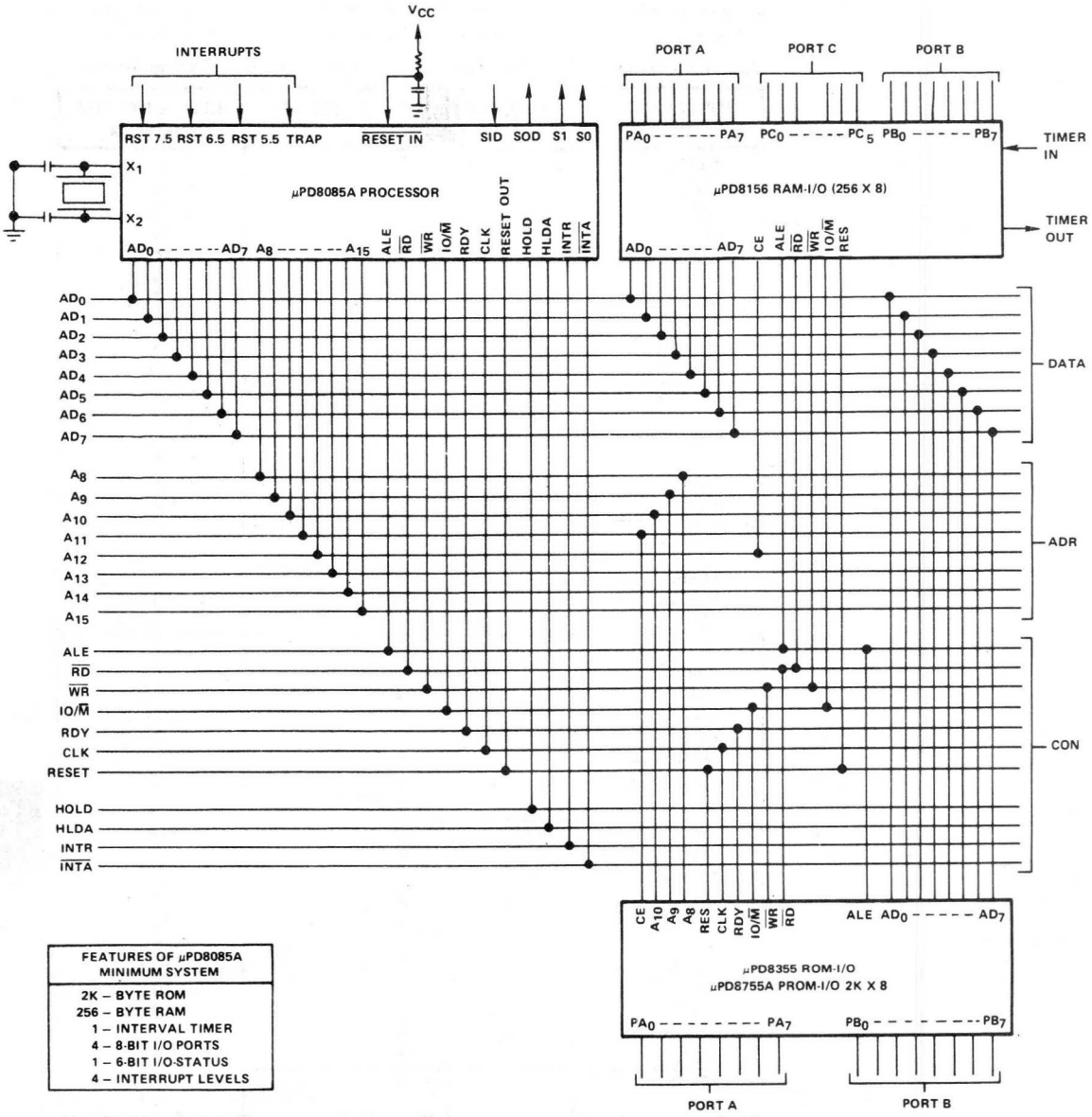
One to five machine cycles ($M_1 - M_5$) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$).

Machine cycles and clock states used for each type of instruction are shown below.

INSTRUCTION TYPE	MACHINE CYCLES EXECUTED MIN/MAX	CLOCK STATUS MIN/MAX
ALU R	1	4
CMC	1	4
CMA	1	4
DAA	1	4
DCR R	1	4
DI	1	4
EI	1	4
INR R	1	4
MOV R, R	1	4
NOP	1	4
ROTATE	1	4
RIM	1	4
SIM	1	4
STC	1	4
XCHG	1	4
HLT	1	5
DCX	1	6
INX	1	6
PCHL	1	6
RET COND.	1/3	6/12
SPHL	1	6
ALU I	2	7
ALU M	2	7
JNC	2/3	7/10
LDAX	2	7
MVI	2	7
MOV M, R	2	7
MOV R, M	2	7
STAX	2	7
CALL COND.	2/5	9/18
DAD	3	10
DCR M	3	10
IN	3	10
INR M	3	10
JMP	3	10
LOAD PAIR	3	10
MVI M	3	10
OUT	3	10
POP	3	10
RET	3	10
PUSH	3	12
RST	3	12
LDA	4	13
STA	4	13
LHLD	5	16
SHLD	5	16
XTHL	5	16
CALL	5	18

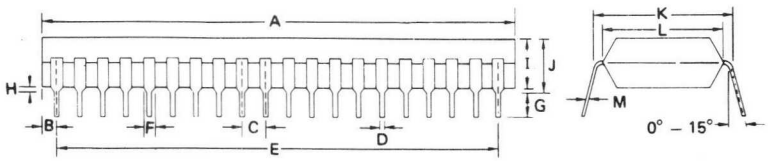
A minimum computer system consisting of a processor, ROM, RAM, and I/O can be built with only 3-40 pin packs. This system is shown below with its address, data, control busses and I/O ports.

μPD8085A FAMILY MINIMUM SYSTEM CONFIGURATION



FEATURES OF μPD8085A MINIMUM SYSTEM
2K – BYTE ROM
256 – BYTE RAM
1 – INTERVAL TIMER
4 – 8-BIT I/O PORTS
1 – 6-BIT I/O-STATUS
4 – INTERRUPT LEVELS

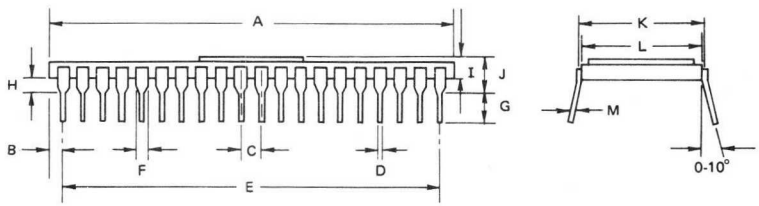
PACKAGE OUTLINE
μPD8085AC



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

μPD8085AD



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.03 MAX.
B	1.62 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.0019

8085ADS-REV2-10-80-CAT

NOTES

16 BIT MICROPROCESSOR

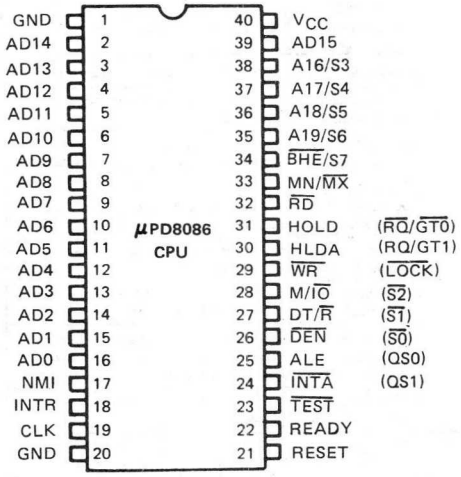
DESCRIPTION

The μPD8086 is a 16-bit microprocessor that has both 8-bit and 16-bit attributes. It has a 16-bit wide physical path to memory for high performance. Its architecture allows higher throughput than the 5 MHz μPD8085A-2.

FEATURES

- Can Directly Address 1 Megabyte of Memory
- Fourteen 16-Bit Registers with Symmetrical Operations
- Bit, Byte, Word, and Block Operations
- 8 and 16-Bit Signed and Unsigned Arithmetic Operations in Binary or Decimal
- Multiply and Divide Instructions
- 24 Operand Addressing Modes
- Assembly Language Compatible with the μPD8080/8085
- Complete Family of Components for Design Flexibility

PIN CONFIGURATION



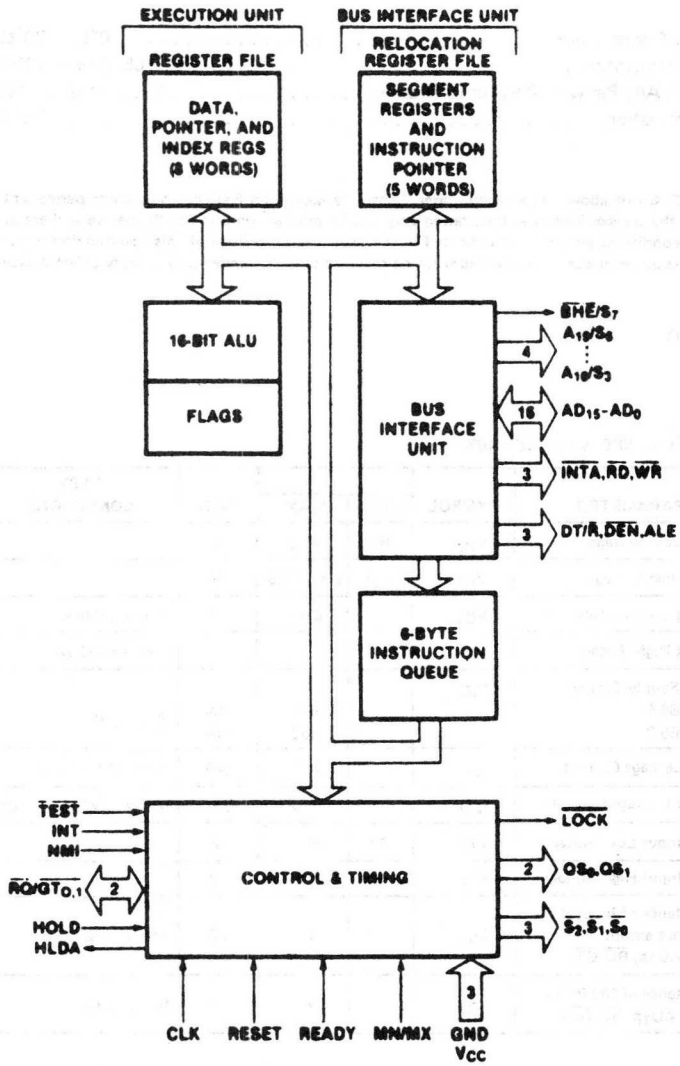
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*Preliminary

PIN IDENTIFICATION

NO.	SYMBOL	NAME	FUNCTION
2-16, 39	AD0-AD15	Address/Data Bus	Multiplexed address (T_1) and data (T_2, T_3, T_W, T_4) bus. 8-bit peripherals tied to the lower 8 bits, use A0 to condition chip select functions. These lines are tri-state during interrupt acknowledge and hold states.
17	NMI	Non-Maskable Interrupt	This is an edge triggered input causing a type Z interrupt. A look-up table is used by the processor for vectoring information.
18	INTR	Interrupt Request	A level triggered input sampled on the last clock cycle of each instruction. Vectoring is via an interrupt look-up table. INTR can mask in software by resetting the interrupt enable bit.
19	CLK	Clock	The clock input is a 1/3 duty cycle input basic timing for the processor and bus controller.
21	RESET	Reset	This active high signal must be high for 4 clock cycles. When it returns low, the processor restarts execution.
22	READY	Ready	An acknowledgement from memory or I/O that data will be transferred. Synchronization is done by the μPD8284 clock generator.
23	$\overline{TEST}$	Test	This input is examined by the "WAIT" instruction, and if low, execution continues. Otherwise the processor waits in an "Idle" state. Synchronized by the processor on the leading edge of CLK.
24	$\overline{INTA}$	Interrupt Acknowledge	This is a read strobe for reading vectoring information. During T_2, T_3, and T_W of each interrupt acknowledge cycle it is low.
25	$\overline{ALE}$	Address Latch Enable	This is used in conjunction with the μPD8282/8283 latches to latch the address, during T_1 of any bus cycle.
26	$\overline{DEN}$	Data Enable	This is the output enable for the μPD8282/8287 transceivers. It is active low during each memory and I/O access and INTA cycles.
27	DT/$\overline{R}$	Data Transmit/Receive	Used to control the direction of data flow through the transceivers.
28	M/$\overline{IO}$	Memory/IO Status	This is used to separate memory access from I/O access.
29	$\overline{WR}$	Write	Depending on the state of the M/$\overline{IO}$ line, the processor is either writing to I/O or memory.
30	HLDA	Hold Acknowledge	A response to the HOLD input, causing the processor to tri-state the local bus. The bus return active one cycle after HOLD goes back low.
31	HOLD	Hold	When another device requests the local bus, driving HOLD high, will cause the μPD8086 to issue a HLDA.
32	$\overline{RD}$	Read	Depending on the state of the M/$\overline{IO}$ line, the processor is reading from either memory or I/O.
33	MN/$\overline{MX}$	Minimum/Maximum	This input is to tell the processor which mode it is to be used in. This effects some of the pin descriptions.
34	$\overline{BHE}$/S_7	Bus/High Enable	This is used in conjunction with the most significant half of the data bus. Peripheral devices on this half of the bus use BHE to condition chip select functions.
35-38	A16-A19	Most Significant Address Bits	The four most significant address bits for memory operations. Low during I/O operations.
26, 27, 28 34-38	S_0-S_7	Status Outputs	These are the status outputs from the processor. They are used by the μPD8288 to generate bus control signals.
24, 25	QS_1, QS_0	Que Status	Used to track the internal μPD8086 instruction que.
29	$\overline{LOCK}$	Lock	This output is set by the "LOCK" instruction to prevent other system bus masters from gaining control.
30, 31	$\overline{RQ}$/GT_0 $\overline{RQ}$/GT_1	Request/Grant	Other local bus masters can force the processor to rebase the local bus at the end of the current bus cycle.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . -1.0 to +7V
Power Dissipation 2.5W

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5V ± 10%

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5	+0.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -400 μA
Power Supply Current μPD8086/ μPD8086-2	I_{CC}		 340 350	 mA mA	 T_a = 25°C
Input Leakage Current	I_{LI}		±10	μA	$0V < V_{IN} < V_{CC}$
Output Leakage Current	I_{LO}		±10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
Clock Input Low Voltage	V_{CL}	-0.5	+0.6	V	
Clock Input High Voltage	V_{CH}	3.9	V_{CC} + 1.0	V	
Capacitance of Input Buffer (All input except AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)	C_{IN}		15	pF	fc = 1 MHz
Capacitance of I/O Buffer (AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)	C_{IO}		15	pF	fc = 1 MHz

AC CHARACTERISTICS

μPD8086: $T_a = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$

MINIMUM COMPLEXITY SYSTEM

TIMING REQUIREMENTS

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
CLK Cycle Period – μPD8086	TCLCL	200	500	125	500	ns	
CLK Low Time	TCLCH	(2/3 TCLCL) –15		(2/3 TCLCL) –15		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2		(1/3 TCLCL) +2		ns	
CLK Rise Time	TCH1CH2		10		10	ns	From 1.0V to 3.5V
CLK Fall Time	TCL2CL1		10		10	ns	From 3.5V to 1.0V
Data In Setup Time	TDVCL	30		20		ns	
Data In Hold Time	TCLDX	10		10		ns	
RDY Setup Time into μPD8284 ① ②	TR1VCL	35		35		ns	
RDY Hold Time into μPD8284 ① ②	TCLR1X	0		0		ns	
READY Setup Time into μPD8086	TRYHCH	(2/3 TCLCL) –15		(2/3 TCLCL) –15		ns	
READY Hold Time into μPD8086	TCHRYX	30		20		ns	
READY Inactive to CLK ③	TRYLCL	–8		–8		ns	
HOLD Setup Time	THVCH	35		20		ns	
INTR, NMI, $\overline{TEST}$ Setup Time ②	TINVCH	30		15		ns	

TIMING RESPONSES

TIMING RESPONSES

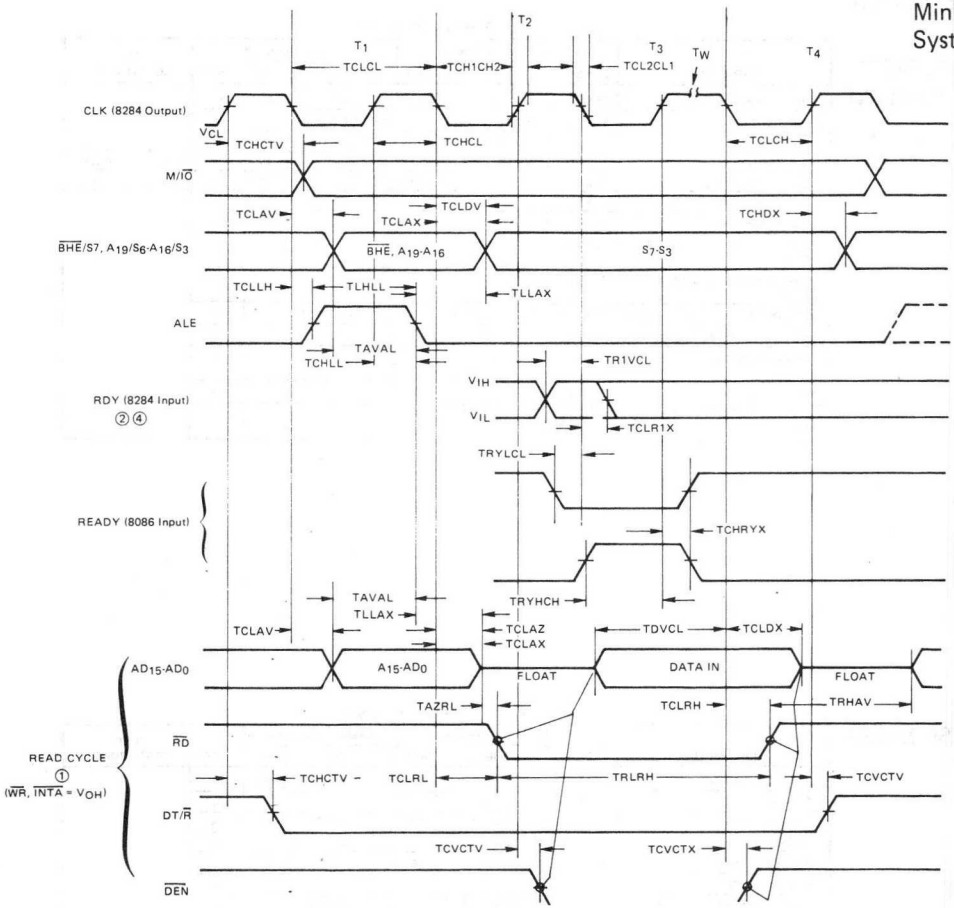
PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Address Valid Delay	TCLAV	10	110	10	60		C_L = 20-100 pF for all μPD8086 Outputs (In addition to μPD8086 self-load)
Address Hold Time	TCLAX	10		10		ns	
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns	
ALE Width	TLHLL	TCLCH–20		TCLCH–10		ns	
ALE Active Delay	TCLLH		80		50	ns	
ALE Inactive Delay	TCHLL		85		55	ns	
Address Hold Time to ALE Inactive	TLLAX	TCHCL–10		TCHCL–10		ns	
Data Valid Delay	TCLDV	10	110	10	60	ns	
Data Hold Time	TCHDX	10		10		ns	
Data Hold Time After WR	TWHDX	TCLCH–30		TCLCH–30		ns	
Control Active Delay 1	TCVCTV	10	110	10	70	ns	
Control Active Delay 2	TCHCTV	10	110	10	60	ns	
Control Active Delay	TCVCTX	10	110	10	70	ns	
Address Float to READ Active	TAZRL	0		0		ns	
$\overline{RD}$ Active Delay	TCLRL	10	165	10	100	ns	
$\overline{RD}$ Inactive Delay	TCLRH	10	150	10	80	ns	
$\overline{RD}$ Inactive to Next Address Active	TRHAV	TCLCL–45		TCLCL–40		ns	
HLDA Valid Delay	TCLHAV	10	160	10	100	ns	
$\overline{RD}$ Width	TRLRH	2TCLCL–75		2TCLCL–50		ns	
$\overline{WR}$ Width	TWLWH	2TCLCL–60		2TCLCL–40		ns	
Address Valid to ALE Low	TAVAL	TCLCH–60		TCLCH–40		ns	

NOTES: ① Signal at μPD8284 shown for reference only.
② Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
③ Applies only to T2 state. (8 ns into T3)

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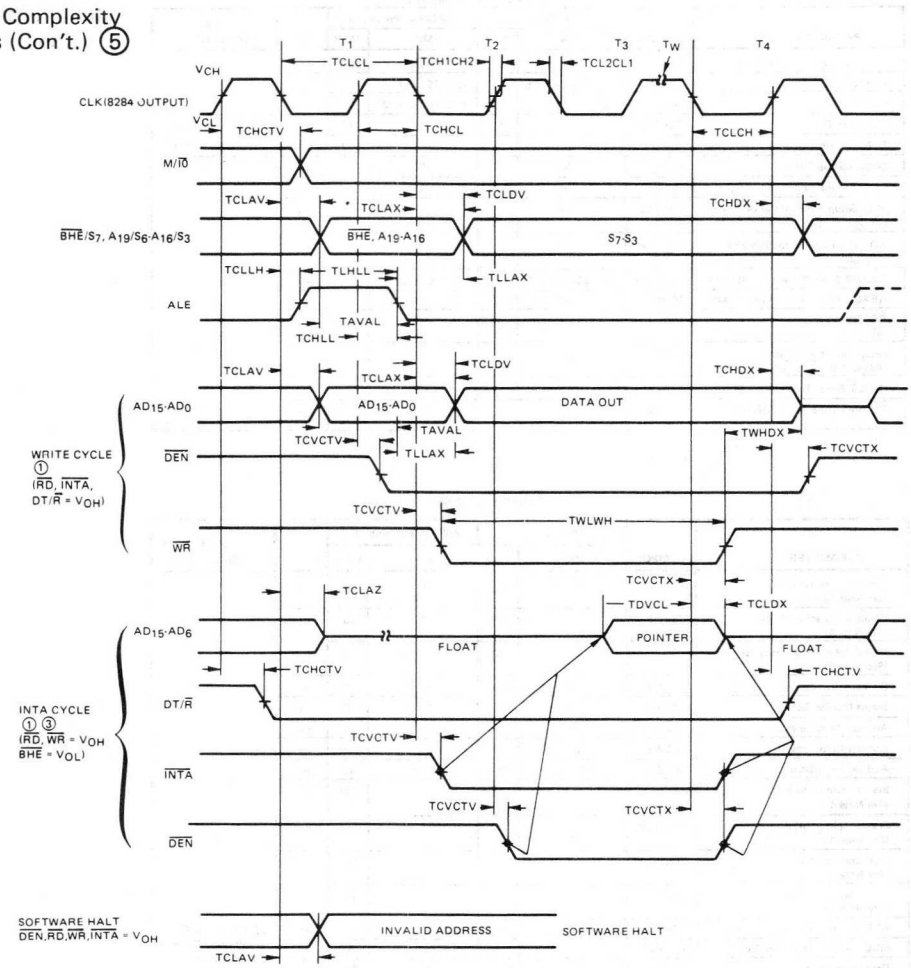
TIMING WAVEFORMS

Minimum Complexity Systems ⑤



TIMING WAVEFORMS

Minimum Complexity Systems (Con't.) ⑤



NOTES: ① All signals switch between V_{OH} and V_{OL} unless otherwise specified.

② RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.

③ Two INTA cycles run back-to-back. The μPD8086 local ADDR/Data Bus is floating during both INTA cycles. Control signals shown for second INTA cycle.

④ Signals at μPD8284 are shown for reference only.

⑤ All timing measurements are made at 1.5V unless otherwise noted.

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MAXIMUM MODE SYSTEM
With μPB8288 Bus Controller

TIMING WITH μPB8288 BUS CONTROLLER

TIMING REQUIREMENTS

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
CLK Cycle Period – μPD8086	TCLCL	200	500	125	500	ns	
CLK Low Time	TCLCH	(2/3 TCLCL) -15		(2/3 TCLCL) -15		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2		(1/3 TCLCL) +2		ns	
CLK Rise Time	TCH1CH2		10		10	ns	From 1.0V to 3.5V
CLN Fall Time	TCL2CL1		10		10	ns	From 3.5V to 1.0V
Data in Setup Time	TDVCL	30		20		ns	
Data in Hold Time	TCLDX	10		10		ns	
RDY Setup Time into μPD8284 ① ②	TR1VCL	35		35		ns	
RDY Hold Time into μPD8284 ①, ②	TCLR1X	0		0		ns	
READY Setup Time into μPD8086	TRYHCH	(2/3 TCLCL) -15		(2/3 TCLCL) -15		ns	
READY Hold Time into μPD8086	TCHRYX	30		20		ns	
READY inactive to CLK ④	TRYLCL	-8		-8		ns	
Setup Time for Recognition (INTR, NMI, TEST) ②	TINVCH	30		15		ns	
$\overline{RQ}/\overline{GT}$ Setup Time	TGVCH	30		15		ns	
$\overline{RQ}$ Hold Time into μPD8086	TCHGX	40		30		ns	

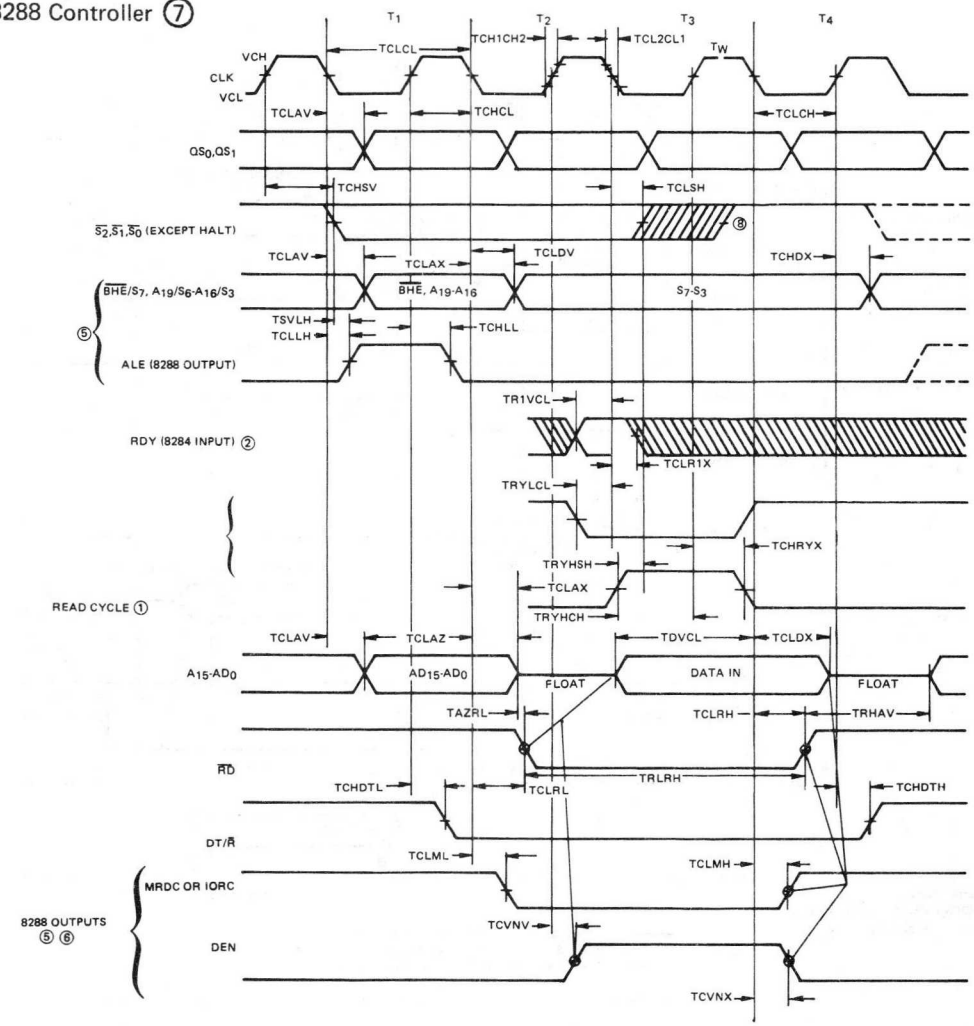
TIMING RESPONSES

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Command Active Delay (See Note 1)	TCLML	10	35	10	35	ns	
Command Inactive Delay (See Note 1)	TCLMH	10	35	10	35	ns	
READY Active to Status Passive (See Note 3)	TRYHSH		110		65	ns	
Status Active Delay	TCHSV	10	110	10	60	ns	
Status Inactive Delay	TCLSH	10	130	10	70	ns	
Address Valid Delay	TCLAV	10	110	10	60	ns	
Address Hold Time	TCLAX	10		10		ns	
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns	
Status Valid to ALE High (See Note 1)	TSVLH		15		15	ns	
Status Valid to MCE High (See Note 1)	TSVMCH		15		15	ns	
CLK Low to ALE Valid (See Note 1)	TCLLH		15		15	ns	
CLK Low to MCE High (See Note 1)	TCLMCH		15		15	ns	
ALE Inactive Delay (See Note 1)	TCHLL		15		15	ns	C_L = 20-100 pF for all μPD8086 Outputs (In addition to μPD8086 self-load)
MCE Inactive Delay (See Note 1)	TCLMCL		15		15	ns	
Data Valid Delay	TCLDV	10	110	10	60	ns	
Data Hold Time	TCHDX	10		10		ns	
Control Active Delay (See Note 1)	TCVNV	5	45	5	45	ns	
Control Inactive Delay (See Note 1)	TCVNX	10	45	10	45	ns	
Address Float to Read Active	TAZRL	0		0		ns	
RD Active Delay	TCLRL	10	165	10	100	ns	
RD Inactive Delay	TCLRH	10	150	10	80	ns	
RD Inactive to Next Address Active	TRHAV	TCLCL-45		TCLCL-40		ns	
Direction Control Active Delay (See Note 1)	TCHDTL		50		50	ns	
Direction Control Inactive Delay (See Note 1)	TCHDTH		30		30	ns	
$\overline{GT}$ Active Delay	TCLGL	0	85	0	50	ns	
$\overline{GT}$ Inactive Delay	TCLGH	0	85	0	50	ns	
$\overline{RD}$ Width	TRLRH	2TCLCL-50		2TCLCL-50		ns	

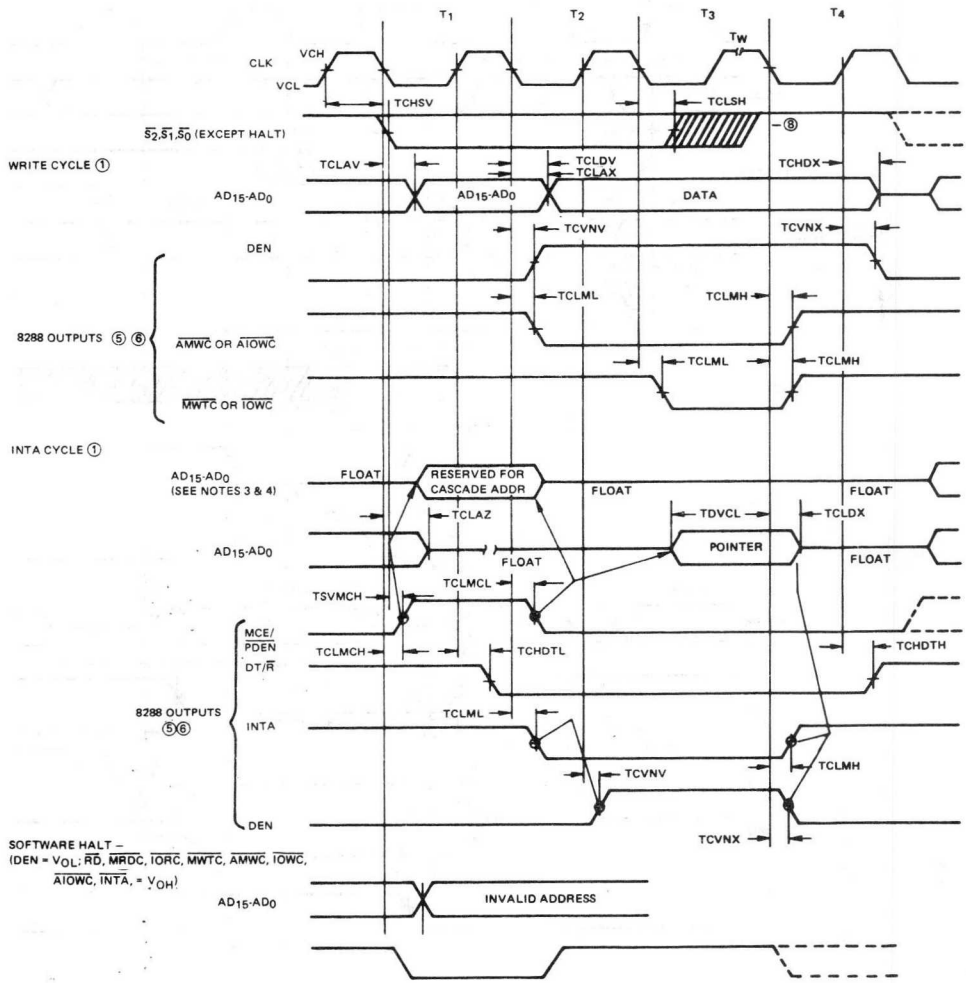
NOTES: ① Signal at μPB8284 or μPB8288 shown for reference only.
② Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
③ Applies only to T3 and wait states.
④ Applies only to T2 state (8 ns into T3).

TIMING WAVEFORMS

Maximum Mode System Using μPB8288 Controller (7)

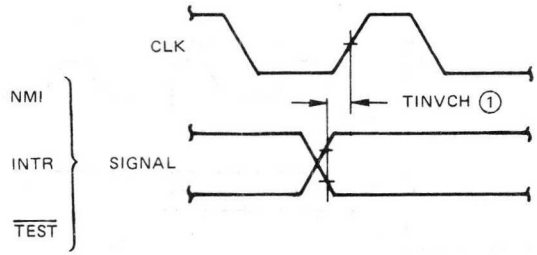


TIMING WAVEFORMS
Maximum Mode
System Using
μPB8288 Controller
(Con't.) ⑦



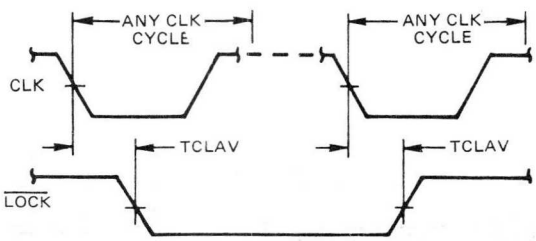
NOTES: ① All signals switch between V_{OH} and V_{OL} unless otherwise specified.
② RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
③ Cascade address is valid between first and second INTA cycle.
④ Two INTA cycles run back-to-back. The 8086 local ADDR/Data Bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
⑤ Signals at 8284 or 8288 are shown for reference only.
⑥ The issuance of the 8288 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high 8288 CEN.
⑦ All timing measurements are made at 1.5V unless otherwise noted.
⑧ Status inactive in state just prior to T_4.

ASYNCHRONOUS SIGNAL RECOGNITION

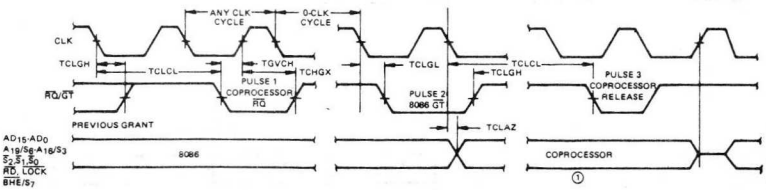


NOTE: (1) Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

BUS LOCK SIGNAL TIMING



REQUEST/GRANT SEQUENCE TIMING*

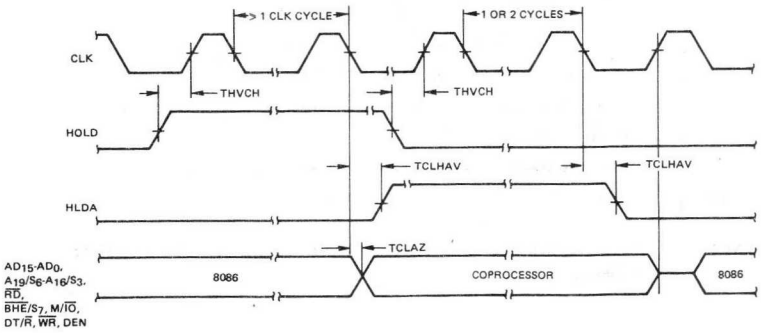


NOTE: (1) The coprocessor may not drive the buses outside the region shown without risking contention.

*for Maximum Mode only

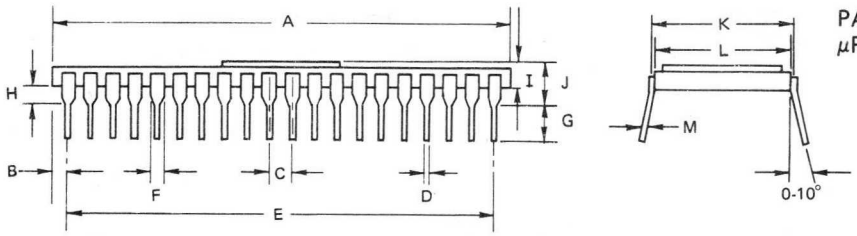
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HOLD/HOLD ACKNOWLEDGE TIMING*



*for Minimum Mode only

PACKAGE OUTLINE μPD8086D



Cerdip

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.03 MAX.
B	1.62 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.0019

SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

DESCRIPTION

The μPD765 is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The μPD765 provides control signals which simplify the design of an external phase locked loop, and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Interface.

Hand-shaking signals are provided in the μPD765 which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the μPD8257. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the μPD765 and DMA controller.

There are 15 separate commands which the μPD765 will execute. Each of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

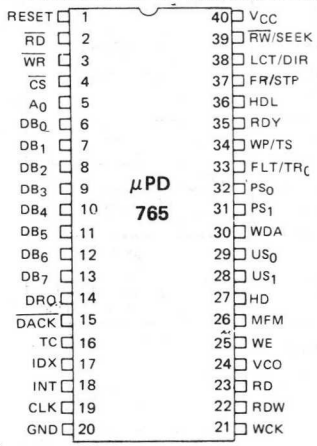
Read Data	Scan High or Equal	Write Deleted Data
Read ID	Scan Low or Equal	Seek
Read Deleted Data	Specify	Recalibrate (Restore to Track 0)
Read a Track	Write Data	Sense Interrupt Status
Scan Equal	Format a Track	Sense Drive Status

FEATURES

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The μPD765 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density modes.

- IBM Compatible in Both Single and Double Density Recording Formats
- Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- Multi-Sector and Multi-Track Transfer Capability
- Drive Up to 4 Floppy Disks
- Data Scan Capability — Will Scan a Single Sector or an Entire Cylinder's Worth of Data Fields, Comparing on a Byte by Byte Basis, Data in the Processor's Memory with Data Read from the Diskette
- Data Transfers in DMA or Non-DMA Mode
- Parallel Seek Operations on Up to Four Drives
- Compatible with Most Microprocessors Including 8080A, 8085A, μPD780 (Z80™)
- Single Phase 8 MHz Clock
- Single +5 Volt Power Supply
- Available in 40 Pin Plastic Dual-in-Line Package

PIN CONFIGURATION

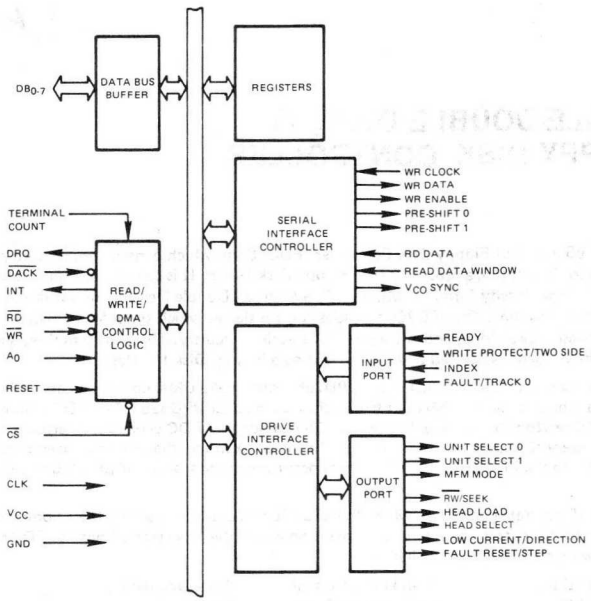


TM:Z80 is a registered trademark of Zilog, Inc.

Rev/2

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +70°C
Storage Temperature	-40°C to +125°C
All Output Voltages	-0.5 to +7 Volts
All Input Voltages	-0.5 to +7 Volts
Supply Voltage V_{CC}	-0.5 to +7 Volts
Power Dissipation	1 Watt

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = -10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = -200 μA
Input Low Voltage (CLK + WR Clock)	$V_{IL(\Phi)}$	-0.5		0.65	V	
Input High Voltage (CLK + WR Clock)	$V_{IH(\Phi)}$	2.4		V_{CC} + 0.5	V	
V_{CC} Supply Current	I_{CC}			150	mA	
Input Load Current (All Input Pins)	I_{LI}			10	μA	V_{IN} = V_{CC}
				-10	μA	V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			-10	μA	V_{OUT} = +0.45V

Note: ① Typical values for T_a = 25°C and nominal supply voltage.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	INPUT/ OUTPUT	CONNECTION TO	FUNCTION
1	RST	Reset	Input	Processor	Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not effect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1-25 ms later. To clear this interrupt use Sense Interrupt Status command.
2	$\overline{RD}$	Read	Input(1)	Processor	Control signal for transfer of data from FDC to Data Bus, when "0" (low).
3	$\overline{WR}$	Write	Input(1)	Processor	Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	$\overline{CS}$	Chip Select	Input	Processor	IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
5	A_0	Data/Status Reg Select	Input(1)	Processor	Selects Data Reg (A_0=1) or Status Reg (A_0=0) contents of the FDC to be sent to Data Bus.
6-13	DB_0-DB_7	Data Bus	Input/(1) Output	Processor	Bi-Directional 8-Bit Data Bus.
14	DRQ	Data DMA Request	Output	DMA	DMA Request is being made by FDC when DRQ="1".
15	$\overline{DACK}$	DMA Acknowledge	Input	DMA	DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
16	TC	Terminal Count	Input	DMA	Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or Interrupt mode.
17	IDX	Index	Input	FDD	Indicates the beginning of a disk track.
18	INT	Interrupt	Output	Processor	Interrupt Request Generated by FDC.
19	CLK	Clock	Input		Single Phase 8 MHz Squarewave Clock.
20	GND	Ground			D.C. Power Return.
21	WCK	Write Clock	Input		Write data rate to FDD. FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM.
22	RDW	Read Data Window	Input	Phase Lock Loop	Generated by PLL, and used to sample data from FDD.
23	RDD	Read Data	Input	FDD	Read data from FDD, containing clock and data bits.
24	VCO	VCO Sync	Output	Phase Lock Loop	Inhibits VCO in PLL when "0" (low), enables VCO when "1".
25	WE	Write Enable	Output	FDD	Enables write data into FDD.
26	MFM	MFM Mode	Output	Phase Lock Loop	MFM mode when "1", FM mode when "0".
27	HD	Head Select	Output	FDD	Head 1 selected when "1" (high), Head 0 selected when "0" (low).
28,29	US_1,US_0	Unit Select	Output	FDD	FDD Unit Selected.
30	WDA	Write Data	Output	FDD	Serial clock and data bits to FDD.
31,32	PS_1,PS_0	Precompensation (pre-shift)	Output	FDD	Write precompensation status during MFM mode. Determines early, late, and normal times.
33	FLT/TR_0	Fault/Track 0	Input	FDD	Senses FDD fault condition, in Read/ Write mode; and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two-Side	Input	FDD	Senses Write Protect status in Read/Write mode; and Two Side Media in Seek mode.
35	RDY	Ready	Input	FDD	Indicates FDD is ready to send or receive data.
36	HDL	Head Load	Output	FDD	Command which causes read/write head in FDD to contact diskette.
37	FR/STP	Flt Reset/Step	Output	FDD	Resets fault F.F. in FDD in Read/Write mode, contains step pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/ Direction	Output	FDD	Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.
39	$\overline{RW}$/SEEK	Read Write/SEEK	Output	FDD	When "1" (high) Seek mode selected and when "0" (low) Read/Write mode selected.
40	V_{CC}	+5V			D.C. Power.

Note: (1) Disabled when CS = 1.

CAPACITANCE

$T_a = 25°C$; $f_c = 1$ MHz; $V_{CC} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Capacitance	$C_{IN(\Phi)}$			20	pF	All Pins Except Pin Under Test Tied to AC Ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

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AC CHARACTERISTICS

T_a = -10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP①	MAX		
Clock Period	Φ_{CY}	120	125	500	ns	
Clock Active (High)	Φ_0	40			ns	
Clock Rise Time	Φ_r			20	ns	
Clock Fall Time	Φ_f			20	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}$ ↓	T_{AR}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}$ ↑	T_{RA}	0			ns	
$\overline{RD}$ Width	T_{RR}	250			ns	
Data Access Time from $\overline{RD}$ ↓	T_{RD}			200	ns	C_L = 100 pf
DB to Float Delay Time from $\overline{RD}$ ↑	T_{DF}	20		100	ns	C_L = 100 pF
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{WR}$ ↓	T_{AW}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time to $\overline{WR}$ ↑	T_{WA}	0			ns	
$\overline{WR}$ Width	T_{WW}	250			ns	
Data Set Up Time to $\overline{WR}$ ↑	T_{DW}	150			ns	
Data Hold Time from $\overline{WR}$ ↑	T_{WD}	5			ns	
INT Delay Time from $\overline{RD}$ ↑	T_{RI}			500	ns	
INT Delay Time from $\overline{WR}$ ↑	T_{WI}			500	ns	
DRQ Cycle Time	T_{MCY}	13			μs	
DRQ Delay Time from $\overline{DACK}$ ↓	T_{AM}			200	ns	
TC Width	T_{TC}	1			ΦCY	
Reset Width	T_{RST}	14			ΦCY	
WCK Cycle Time	T_{CY}		2 or 4② 1 or 2		μs	MFM = 0 MFM = 1
WCK Active Time (High)	T_0	80	250	350	ns	
WCK Rise Time	T_r			20	ns	
WCK Fall Time	T_f			20	ns	
Pre-Shift Delay Time from WCK ↑	T_{CP}	20		100	ns	
WDA Delay Time from WCK ↑	T_{CD}	20		100	ns	
RDD Active Time (High)	T_{RDD}	40			ns	
Window Cycle Time	T_{WCY}		2.0 1.0		μs	MFM = 0 MFM = 1
Window Hold Time to/from RDD	T_{RDW} T_{WRD}	15			ns	
$US_{0,1}$ Hold Time to $\overline{RW}$/SEEK ↑	T_{US}	12			μs	8 MHz Clock Period
SEEK/RW Hold Time to LOW CURRENT/DIRECTION ↑	T_{SD}	7			μs	
LOW CURRENT/DIRECTION Hold Time to FAULT RESET/STEP ↑	T_{DST}	1.0			μs	
$US_{0,1}$ Hold Time from FAULT RESET/STEP ↑	T_{STU}	5.0			μs	
STEP Active Time (High)	T_{STP}		5.0		μs	
STEP Cycle Time	T_{SC}	33	③	③	μs	
FAULT RESET Active Time (High)	T_{FR}	8.0		10	μs	
Write Data Width	T_{WDD}	T_0-50			ns	
$US_{0,1}$ Hold Time After SEEK	T_{SU}	15			μs	8 MHz Clock Period
Seek Hold Time from DIR	T_{DS}	30			μs	
DIR Hold Time after STEP	T_{STD}	24			μs	
Index Pulse Width	T_{IDX}	625			μs	
$\overline{RD}$ ↓ Delay from DRQ	T_{MR}	800			ns	8 MHz Clock Period
$\overline{WR}$ ↓ Delay from DRQ	T_{MW}	250			ns	
$\overline{WE}$ or $\overline{RD}$ Response Time from DRQ ↑	T_{MRW}			12	μs	

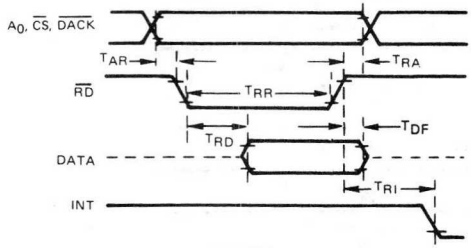
Notes: ① Typical values for T_a = 25°C and nominal supply voltage.

② The former value of 2 and 1 are applied to Standard Floppy, and the latter value of 4 and 2 are applied to Mini-floppy.

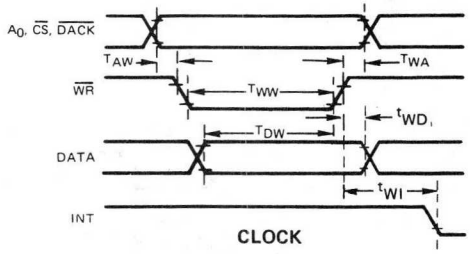
③ Under Software Control. The range is from 1 ms to 16 ms at 8 MHz Clock Period, and 2 to 32 ms at 4 MHz Clock Period.

TIMING WAVEFORMS

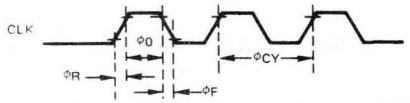
PROCESSOR READ OPERATION



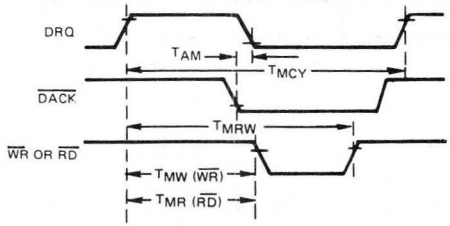
PROCESSOR WRITE OPERATION



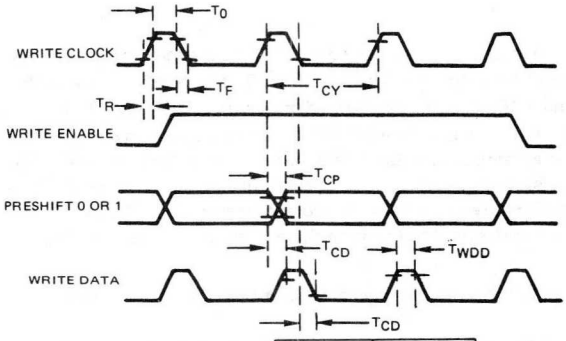
CLOCK



DMA OPERATION



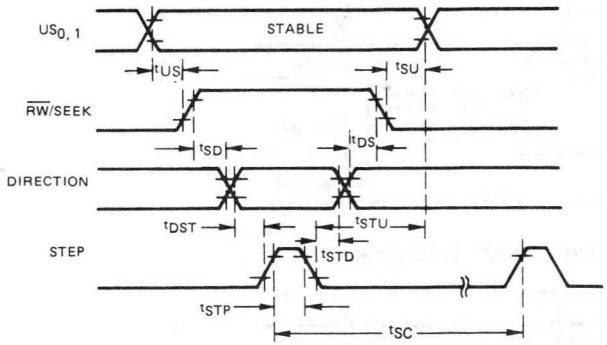
FDD WRITE OPERATION



	PRESHIFT 0	PRESHIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

TIMING WAVEFORMS (CONT.)

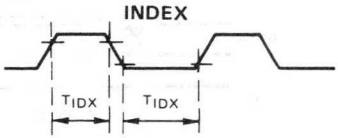
SEEK OPERATION



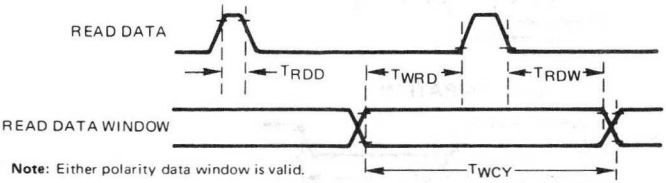
FLT RESET



INDEX

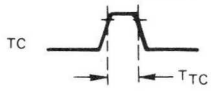


FDD READ OPERATION

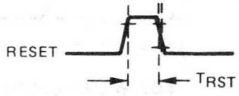


Note: Either polarity data window is valid.

TERMINAL COUNT



RESET



INTERNAL REGISTERS

The μPD765 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and μPD765.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown below.

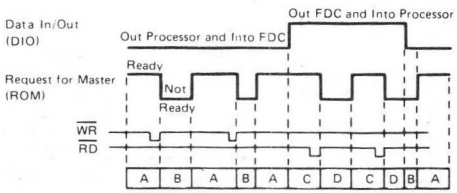
A_0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

INTERNAL REGISTERS (CONT.)

The bits in the Main Status Register are defined as follows:

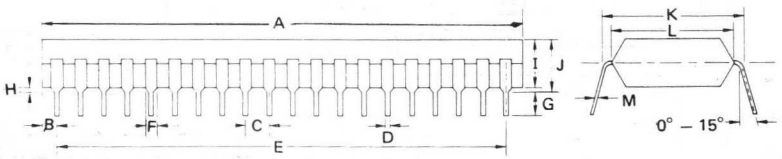
BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
DB_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended, and result phase was started. It operates only during NON-DMA mode of operation.
DB_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. The max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time Main Status Register is read the CPU should wait 12 μs. The max time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB_4 (FDC Busy) goes low is 12 μs.



Notes: [A] – Data register ready to be written into by processor
[B] – Data register not ready to be written into by processor
[C] – Data register ready for next data byte to be read by the processor
[D] – Data register not ready for next data byte to be read by processor

PACKAGE OUTLINE μPD765C



ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

COMMAND SEQUENCE

The μPD765 is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the μPD765 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase: The FDC receives all information required to perform a particular operation from the processor.

Execution Phase: The FDC performs the operation it was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping information are made available to the processor.

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ DATA										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ DELETED DATA										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DATA										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the main-system and FDD
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DELETED DATA										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ A TRACK										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system. FDC reads all data fields from index hole to EOT.
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ ID										
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information read during Execution Phase from Floppy Disk.
	R	H								
	R	R								
	R	N								
FORMAT A TRACK										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire track
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								
SCAN EQUAL										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

Note: ① Symbols used in this table are described at the end of this section.

② A_0 should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

PHASE	R/W	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
SCAN LOW OR EQUAL			
Command	W	MT MF SK 1 1 0 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution
	R	H	
	R	R	
	R	N	
SCAN HIGH OR EQUAL			
Command	W	MT MF SK 1 1 1 0 1	Command Codes
	W	X X X X X HD US1 US0	
	W	C	Sector ID information prior Command execution
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data-compared between the FDD and main-system
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution
	R	H	
	R	R	
	R	N	

PHASE	R/W	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
RECALIBRATE			
Command	W	0 0 0 0 0 1 1 1	Command Codes
	W	X X X X X 0 US1 US0	
Execution			Head retracted to Track 0
SENSE INTERRUPT STATUS			
Command	W	0 0 0 0 1 0 0 0	Command Codes
Result	R	STO	Status information at the end of seek-operation about the FDC
	R	PCN	
SPECIFY			
Command	W	0 0 0 0 0 0 1 1	Command Codes
	W	SRT HUT	
	W	HLT ND	
SENSE DRIVE STATUS			
Command	W	0 0 0 0 0 1 0 0	Command Codes
	W	X X X X X HD US1 US0	
Result	R	ST 3	Status information about FDD
SEEK			
Command	W	0 0 0 0 1 1 1 1	Command Codes
	W	X X X X X HD US1 US0	
	W	NCN	
Execution			Head is positioned over proper Cylinder on Diskette
INVALID			
Command	W	Invalid Codes	Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	ST 0	ST 0 = 80 (16)

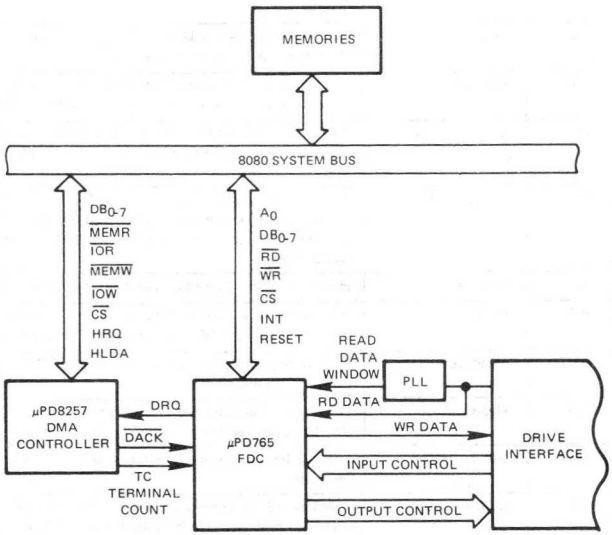
COMMAND SYMBOL DESCRIPTION

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1)
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop date transfer after a sector # equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1.

COMMAND SYMBOL DESCRIPTION (CONT.)

SYMBOL	NAME	DESCRIPTION
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.).
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0 = 0$). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

SYSTEM CONFIGURATION



PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data read or written to Data Register, CPU should wait for 12 μs before reading MSR. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the μPD765. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the μPD765 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the μPD765 is in the NON-DMA Mode, then the receipt of each data byte (if μPD765 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will reset the Interrupt as well as output the Data onto the Data Bus. If the processor cannot handle Interrupts fast enough (every 13 μs) for MFM and 27 μs for FM mode, then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the WR signal performs the reset to the Interrupt signal.

If the μPD765 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The μPD765 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) or EOT sector was read/written, then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The μPD765 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The μPD765 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the μPD765 to form the Command Phase, and are read out of the μPD765 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the μPD765, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the μPD765 is ready for a new command.

POLLING FEATURE OF THE μPD765

After the Specify command has been sent to the μPD765, the Unit Select line US0 and US1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the μPD765 polls all four FDD's looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the μPD765 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the μPD765 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands.

READ DATA

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the $\overline{\text{DACK}}$ for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.
The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 1. Transfer Capacity

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the Command.

FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

Notes: 1 NC (No Change): The same value as the one at the beginning of command execution.

2 LSB (Least Significant Bit): The least significant bit of H is complemented.

WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the Specify Command), and begins reading ID Fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs in the FM mode, and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

9

READ A TRACK

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status Register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

READ ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

FORMAT A TRACK

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the μPD765 for each sector on the track. If FDC is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes:

		8" STANDARD FLOPPY					5¼" MINI FLOPPY				
FORMAT	SECTOR SIZE	N	SC	GPL ①	GPL ②	REMARKS	SECTOR SIZE	N	SC	GPL ①	GPL ②
FM Mode	128 bytes/Sector	00	$1A_{(16)}$	$07_{(16)}$	$1B_{(16)}$	IBM Diskette 1	128 bytes/Sector	00	12	07	09
	256	01	$0F_{(16)}$	$0E_{(16)}$	$2A_{(16)}$	IBM Diskette 2	128	00	10	10	19
	512	02	08	$1B_{(16)}$	$3A_{(16)}$		256	01	08	18	30
FM Mode	1024 bytes/Sector	03	04	47	8A		512	02	04	46	87
	2048	04	02	C8	FF		1024	03	02	C8	FF
	4096	05	01	C8	FF		2048	04	01	C8	FF
MFM Mode	256	01	$1A_{(16)}$	$0E_{(16)}$	$36_{(16)}$	IBM Diskette 2D	256	01	12	0A	0C
	512	02	$0F_{(16)}$	$1B_{(16)}$	$54_{(16)}$		256	01	10	20	32
	1024	03	08	$35_{(16)}$	$74_{(16)}$	IBM Diskette 2D	512	02	08	2A	50
	2048	04	04	99	FF		1024	03	04	80	F0
	4096	05	02	C8	FF		2048	04	02	C8	FF
	8192	06	01	C8	FF		4096	05	01	C8	FF

Table 3

Note: ① Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.

② Suggested values of GPL in format command.

③ In MFM mode FDC can perform a read operation only with 128 bytes/sector. (N = 00)

SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexidicernial byte of FF either from memory or from FDD can be used as a mask byte because it always meet the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

Table 4

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

SEEK

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)

PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits D_0B-D_3B in Main Status Register are set during seek operation and are clear by Sense Interrupt Status command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once. No other command could be issue for as long as FDC is in process of sending Step Pulses to any drive.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between first two Step Pulses may be shorter then set in the Specify command by as much as 1 ms.

RECALIBRATE

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulse have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in NON-DMA Mode, DB5 in Main Status Register is high. Upon entering Result Phase this bit gets clear. Reason 1 and 4 does not require Sense Interrupt Status command. The interrupt is cleared by reading/writing data to FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

SEEK END BIT 5	INTERRUPT CODE		CAUSE
	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Table 5

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

Issuing Sense Interrupt Status Command without interrupt pending is treated as an invalid command.

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms . . . . OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms . . . 7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the μPD765 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the μPD765 is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0 it will find a 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

STATUS REGISTER IDENTIFICATION

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 0			
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit Number at Interrupt
D_0	Unit Select 0	US 0	
STATUS REGISTER 1			
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.

STATUS REGISTER IDENTIFICATION (CONT.)

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 1 (CONT.)			
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2			
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3			
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

It is suggested that you utilize the following applications notes:

① #8 – for an example of an actual interface, as well as a "theoretical" data separator.

② #10 – for a well documented example of a working phase lock loop.

NOTES

DOT MATRIX PRINTER CONTROLLER

DESCRIPTION

The μPD781 is an LSI Dot Matrix Printer Controller chip which contains all the circuitry and control functions for interfacing an 8-bit processor to the Epson model 512, 522, and 542 Dot Matrix Printers. These printers are capable of printing 40 columns per row with a 5 x 7 dot matrix. The μPD781 is ideally suited for low-cost Electronic Cash Registers (ECR) and Point of Sale (POS) systems because it frees the processor from direct control of the printer and simplifies I/O software.

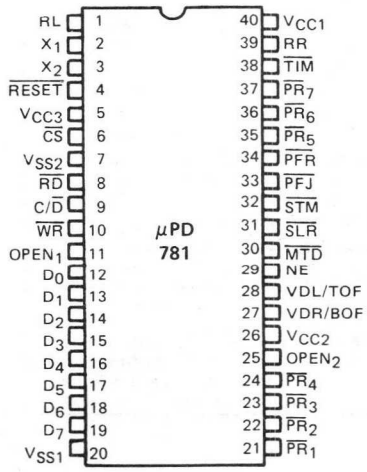
There are nine separate instructions which the μPD781 will execute. Each of these instructions requires only a single 8-bit byte from the processor to be executed. Upon receipt of the instruction the μPD781 assumes control of the printer, increments the print head, activates the print solenoids, performs line feed on either receipt or journal registers (or both), and performs these operations for an entire print line of 40 columns.

The μPD781 contains its own on-board character generator of 96 symbols. It contains a 40 column printer buffer and is capable of supplying status information to the host processor on both the controller itself as well as the printer. Characters to be printed are written into the μPD781 by the processor, and after the receipt of 40 characters the entire row is printed out with a single print command.

FEATURES

- Compatible with most Microprocessors including 8080A, 8085A, μPD780 (Z80™)
- Capable of Interfacing to Epson Model 512, 522, or 542 Printers
- Print Technique – Serial Dot Matrix
- Print Font – 5 x 7 Dot Matrix
- Column Print Capacity: 40 Columns for Model 512 and 522; 18 Columns for Receipt and 18 Columns for Journal-Model
- Buffer Capacity: 40 Columns – Model 512 and 522; 2 to 18 Columns – Model 542
- 96 Character Set (Alphanumerics Plus Symbols)
- Print Speed – Approximately 3 Lines/sec (Bidirectional Printing)
- Paper Feed: Independent or Simultaneous; Receipt and Journal Feed; Fast Feed
- Stamp Drive Output – Also Cutter Drive Output and Slip Release for Model 522.
- Sense Printer Status: Validation (Left/Right) Sensor – Model 512 and 522; TOF, BOF Sensor – Model 542; Low Paper Detector – Model 512 and 522
- On-Board 6 MHz Oscillator (External Crystal Required)
- Operates from a Single +5V Power Supply (NMOS Technology)
- Available in 40-Pin Plastic Package

PIN CONFIGURATION



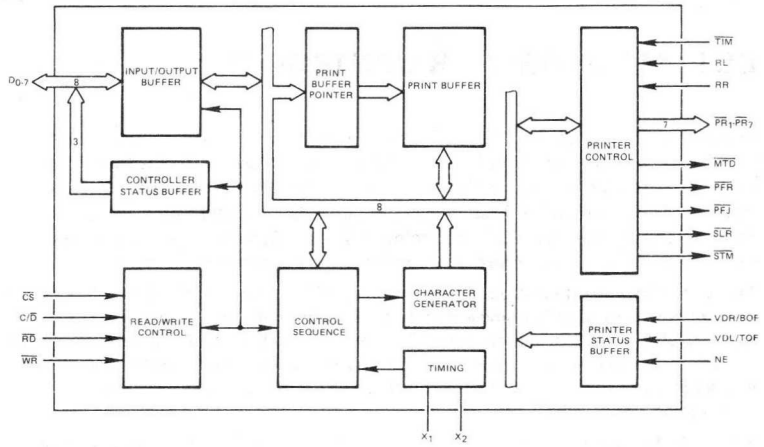
PIN NAMES

RL	Reset Signal (L)
RR	Reset Signal (R)
X_1, X_2	Crystal Inputs
$\overline{RESET}$	Reset
$\overline{CS}$	Chip Select
$\overline{RD}$	Read
C/$\overline{D}$	Command/Data
$\overline{WR}$	Write
$D_{0\text{-}7}$	Data Bus
$\overline{PR}_1$-$\overline{PR}_7$	Print Solenoids
VDR/BOF	Validation (R)/BOF Sensor
VDL/TOF	Validation (L)/TOP Sensor
NE	Low Paper Detector
$\overline{MTD}$	Motor Drive
$\overline{SLR}$	Slip Release
$\overline{STM}$	Stamp
$\overline{PFJ}$	Paper Feed Journal
$\overline{PFR}$	Paper Feed Receipt
$\overline{TIM}$	Timing Signal

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BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NUMBER	PIN SYMBOL	PIN NAME	I/O	FUNCTION
2, 3	X_1,X_2	External Crystal Input	I	This is a connection to external crystal (Frequency: 6 MHz). X_1 could also be used as input for external oscillator.
4	$\overline{RESET}$	Reset	I	The Reset signal initializes the μPD781. When $\overline{RESET}$ = 0, the buffer and register contents are: Bus Buffer – (IOM-1, IOB=PSR=0). Column Buffer – All characters in this buffer become $20_{(16)}$ (ASCII). Column Buffer Pointer – It indicates the left side of the buffer. Column Capacity – 40 columns. Print Head – Current Position.
6	$\overline{CS}$	Chip Select	I	If the Chip Select is 0 when the data bus becomes active, it enables the transfer of data between the processor and the μPD781 via the data bus. If it is 1, the data bus goes into High-Impedance state (inactive). However, the operation of the printer is not affected when $\overline{CS}$=1.
8	$\overline{RD}$	Read	I	The Read Control Signal is used to read controller status or printer status to the host processor. When $\overline{RD}$=1, status information is presented.
10	$\overline{WR}$	Write	I	The Write Control Signal is used to write commands or print data to the μPD781. When $\overline{WR}$=0, data on the data bus is written into the μPD781.
9	C/$\overline{D}$	Command/ Data Select	I	The C/$\overline{D}$ Select is used to indicate what kind of data is being input/output on the data bus by the host processor. When C/$\overline{D}$=1 in Read Operation, it is a Controller Status and in Write Operation it gives commands. When C/$\overline{D}$=0 in Read Operation it is a Printer Status and in Write Operation it is print data.

PIN IDENTIFICATION (CONT.)

PIN NUMBER	PIN SYMBOL	NAME	I/O	FUNCTION
12-19	D_{0-7}	Data Bus	I/O 3-State	It is an 8-bit bi-directional data bus and is used to transfer the data between the host processor and the μPD781.
5,26, 40	V_{CC1-3}	DC Power		These are connected to +5V power supply.
7,20	V_{SS1-2}	Signal Ground		
11,25	$OPEN_{1-2}$	No Connection		These pins must be open. Do not connect them to +5V, GND or any other signals.
21-24, 35-37	$\overline{PR_1}$-$\overline{PR_7}$	Print Solenoid	O	These are drive signals for the print solenoids. When these signals are 0, the print solenoid should be activated. They are synchronized with the timing signal ($\overline{TIM}$), which is issued from the printer.
38	$\overline{TIM}$	Timing Signal	I	The timing signal is issued from the printer. It is used to generate and synchronize all the basic printer operations such as paper feed, paper cut, etc.
1	RL	Reset Signal Left	I	The reset signal (RL=1) is issued by the printer and indicates that the print-head is positioned at the left margin.
39	RR	Reset Signal Right	I	The reset signal (RR=1) is issued by the printer and indicates that the print-head is positioned at the right margin.
30	$\overline{MTD}$	Motor Drive	O	The motor drive signal is issued to the printer, and is active during low state.
34	$\overline{PFR}$	Paper Feed Receipt	O	This is the drive signal for the paper feed magnet and is active during low state. In Model 512 and 542 it is used as a paper feed magnet drive signal, and in Model 522 it is used as a receipt paper feed magnet drive signal.
33	$\overline{PFJ}$	Paper Feed Journal	O	This is the drive signal for the journal paper feed and is active during low state. It is used only with Model 522, and is not used at all in Model 512 and 542.
32	$\overline{STM}$	Stamp	O	This is the drive signal for both the stamp magnet and the paper cutter and is active during the low state. This signal is used only with Model 522. If partial-cut or stamp and full-cut are required, they may be implemented by using the Fast Feed command which is synchronized with each timing pulse before it is output. This signal is not used in the Model 512 and 542.
31	$\overline{SLR}$	Slip Release	O	This is the drive signal for the slip release magnet and is active during low state. It is used only with Model 542, and is active only during the Print command or Fast Feed command. This signal is not used in the Model 512 and 522.
27	VDR/BOF	Validation Right/BOF Sensor ①	I	In Model 512 and 522, the Validation Right signal (VDR) is used to detect when the print-head is located at the right side of the paper. In Model 542, the BOF Sensor signal (BOF) is used to detect the end of the paper.
28	VDL/TOF	Validation Left/TOF Sensor ①	I	In Model 512 and 522, the Validation Left signal (VDL) is used to detect when the print-head is located at the left side of the paper. In Model 542, the TOF Sensor signal (TOF) is used to detect the top of the paper.
29	NE	Low Paper Detector①	I	This signal is used to indicate a low paper condition and is active in high state.

Note: ① The VDR/BOF, VDL/TOF and NE signals are available on the data bus when a Printer Status is requested by the host processor. The μPD781 passes these signals onto the host processor.

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +125°C
Voltage On Any Pin . . . . . -0.5 to +7 Volts①

Note: ① With Respect to Ground.

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC1-3} = +5V ± 5%; V_{SS1-2} = 0V

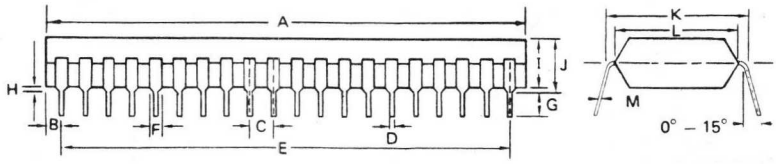
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage (All except XTAL 1, XTAL 2, $\overline{RESET}$)	V_{IH1}	2.0		VCC	V	
Input High Voltage (XTAL 1, XTAL 2, RESET)	V_{IH2}	3.5		V_{CC}	V	
Input Low Voltage (All except XTAL 1, XTAL 2)	V_{IL}	-0.5		0.8	V	
Output High Voltage (D_{0-7})	V_{OH1}	2.4			V	I_{OH} = -400 μA
Output High Voltage (All Other Outputs)	V_{OH2}	2.4			V	I_{OH} = -50 μA
Output Low Voltage (D_{0-7})	V_{OL1}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (All Other Outputs except D_{0-7})	V_{OL2}			0.45	V	I_{OL} = 1.6 mA
Low Input Source Current (VDR/$\overline{BOF}$, VDL/TOF, NE, $\overline{TIM}$)	I_{LI1}			0.4	mA	V_{IL} = 0.8V
Low Input Source Current ($\overline{RESET}$)	I_{LI2}			*0.2	mA	V_{IL} = 0.8V
Input Leakage Current (RL, RR, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, C/$\overline{D}$)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Output Leakage Current (D_{0-7}, High Impedance State)	I_{OL}			±10	μA	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$
Total Supply Current (I_{CC1} + I_{CC2} + I_{CC3})	I_{CC}		65	135	mA	T_a = 25°C

AC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC1-3} = +5V \pm 5\%$; $V_{SS1-2} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ OPERATION						
$\overline{CS}$, C/$\overline{D}$ Setup to $\overline{RD}$ ↓	t_{AR}	0			ns	D_{0-7} Input
CS, C/$\overline{D}$ Hold After $\overline{RD}$ ↑	t_{RA}	0			ns	
$\overline{RD}$ Pulse Width	t_{RR}	250		5000	ns	
$\overline{CS}$, C/$\overline{D}$ to Data Out Delay	t_{AD}			180	ns	
$\overline{RD}$ ↓ to Data Out Delay	t_{RD}			180	ns	
RD ↑ to Data Float Delay	t_{DF}	10		100	ns ns	
Recovery Time Between Reads And/Or Write	t_{RV}	1			μs	
WRITE OPERATION						
$\overline{CS}$, C/$\overline{D}$ Setup to $\overline{WR}$ ↓	t_{AW}	0			ns	D_{0-7} Output C_L = 100 pF
$\overline{CS}$, C/$\overline{D}$ Hold After $\overline{WR}$ ↑	t_{WA}	0			ns	
$\overline{WR}$ Pulse Width	t_{WW}	250		5000	ns	
Data Setup to $\overline{WR}$ ↑	t_{DW}	150			ns	
Data Hold After $\overline{WR}$ ↑	t_{WD}	0			ns	
PRINT OPERATION						
$\overline{TIM}$ ↓ to $\overline{PR}_{1-7}$ ↓ Delay	t_{TP}			167.5	μs	6 MHz Crystal
$\overline{PR}_{1-7}$ Pulse Width	t_{PP}		600		μs	
$\overline{TIM}$ ↓ to $\overline{PFJ}$, $\overline{PFR}$ ↓ Delay	t_{TF1}			140	μs	
$\overline{TIM}$ ↓ to $\overline{PFJ}$, $\overline{PFR}$ ↑ Delay	t_{TF2}			127.5	μs	
$\overline{TIM}$ ↓ to $\overline{SLR}$ ↓ Delay	t_{TR1}			60	μs	
$\overline{TIM}$ ↓ to $\overline{SLR}$ ↑ Delay	t_{TR2}			50	μs	
$\overline{TIM}$ ↓ to $\overline{STM}$ ↓ Delay	t_{TS1}			72.5	μs	
$\overline{TIM}$ ↓ to $\overline{STM}$ ↑ Delay	t_{TS2}			37.5	μs	

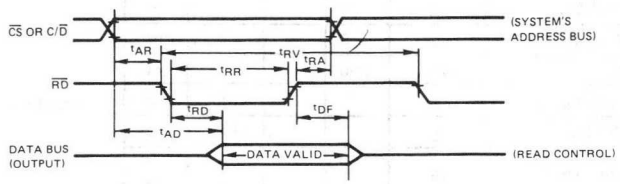
PACKAGE OUTLINE μPD781C



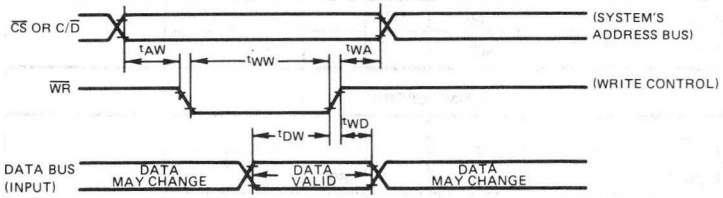
ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

TIMING WAVEFORMS

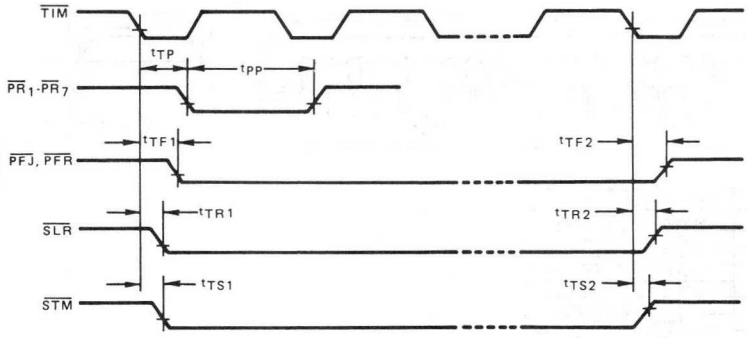
READ OPERATION



WRITE OPERATION



PRINT OPERATION



COMMANDS

All transfer of information between the μPD781 and the host processor is via the data bus, and the four (4) control signals, $\overline{CS}$, C/$\overline{D}$, $\overline{WR}$ and $\overline{RD}$. The four control signals determine what type of data transfer will occur on the data bus.

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	DATA BUS	OPERATION
0	0	0	0	–	Inhibited
0	0	1	0	Print Data	Write Data into Column Buffer
0	0	0	1	Printer Status	Read Printer Status
0	0	1	1	–	No Operation
0	1	0	0	–	Inhibited
0	1	1	0	Command	Write Command for Printer
0	1	0	1	Controller Status	Read Controller Status
0	1	1	1	–	No Operation
1	X	X	X	–	Disable μPD781

Before issuing any new command or loading new data into the column buffer, the host processor should check the controller status bits IOM, IOB and PSR. No new operation should be performed if IOB bit indicates that the μPD781 is busy.

Controller Status Register

X	X	X	X	X	IOM	IOB	PSR

Printer Status Register

X	X	X	X	R	S	T	U

COMMAND		DATA BUS							
		DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Initialize		0	0	0	L/R	x	x	x	x
Request Printer Status		0	0	1	x	x	x	x	x
Printer Format		0	1	b_1	b_0	x	x	x	x
Increment Column Printer		0	1	1	1	n_3	n_2	n_1	n_0
Print	Model 512 and 542	1	0	0	0	x	LF	x	SR
	Model 522	1	0	a_1	a_0	LFJ	LFR	x	x
Fast Feed		1	1	c_1	c_0	n_3	n_2	n_1	n_0
Write Print Data		x	d_6	d_5	d_4	d_3	d_2	d_1	d_0

Note: X = Not Acceptable

CONTROLLER STATUS REGISTER

IOM – Input/Output Buffer Mode

The IOM flag indicates the direction of data on the data bus. If IOM=1 data is from processor to μPD781 (write into μPD781). If IOM=0 data is from μPD781 to processor (read from μPD781). Immediately after reading printer status, IOM goes from 0 to 1.

IOB – Input/Output Buffer Busy

The IOB flag indicates when the I/O buffer is busy and an operation is in process. If IOB=1 I/O buffer is busy and no new command should be performed. If IOB=0 μPD781 is ready to accept new command.

PSR – Printer Status Ready

The PSR flag indicates that the printer status may be read by the processor. If PSR=1 printer status is ready to be read by processor. If PSR=0 printer status is not ready.

PRINTER STATUS REGISTER

R – Location of Print Head

R=1 Print Head located at left side of carriage.
R=0 Print Head located at right side of carriage.

R	S ①	T ①	U ①	OPERATION
x	x	x	1	Detection of R/BOF Sensor
x	x	1	x	Detection of L/TOF Sensor
x	1	x	x	Detection of Low Paper (NE)

Note: ① These bits could have other meanings depending on the signals connected to pins 27, 28, 29.

INITIALIZE COMMAND

This command is similar to the RESET command, but it also allows to position the print head.

L/R – Print Head Left/Right Side

L/R=1 Print Head is positioned at the left side.
L/R=0 Print Head is positioned at the right side.

Contents of column buffer is set to 20 hexadecimal (equal to blank), reset condition.

REQUEST PRINTER STATUS COMMAND

This command will latch the status of the printer in the internal register. It must be followed by a Printer Status Read Operation. No other command will be accepted until the printer status is read.

COMMAND SYMBOLS (CONT.)

PRINTER FORMAT COMMAND

This command sets the controller for the appropriate printer model.

b_1,b_0 – Format for Column Buffer

b_1	b_0	COLUMN FORMAT	MODEL PRINTER	COMMENTS
0	0	40 columns	512 or 542	Column Buffer Set at 40 Column
0	1	18 columns	522	Both Receipt and Journal Print Identical 18 Column
1	0	2 x 18 columns	522	Receipt and Journal Print Separate 18 Columns, With Receipt First and Journal Second

INCREMENT COLUMN POINTER COMMAND

The column pointer within the buffer is incremented to the right by the binary value indicated by n_0 through n_3. In the case of the 2 x 18 column format for the Model 522, the pointer can only move within the receipt or journal side, depending upon which side it is presently located.

PRINT COMMAND

The entire column buffer is printed and after the print operation is complete the contents of the buffer are reset to 20 hexidecimal (blank). During the execution of the print command no other commands are executed.

Models 512 and 542

LF	SR	OPERATION
0	0	Print Only
0	1	After Printing Perform Slip Release Only
1	0	After Printing Perform Line Feed Only
1	1	After Printing Perform Both Line Feed and Slip Release

Model 522

a_1	a_0	OPERATION
0	1	Print Receipt Only
1	0	Print Journal Only
1	1	Print Receipt and Journal

Model 522

LFJ	LFR	OPERATION
0	0	Print Only
0	1	After Printing Perform Line Feed on Receipt Only
1	0	After Printing Perform Line Feed on Journal Only
1	1	After Printing Perform Line Feed on Both Receipt and Journal

FAST FEED COMMAND

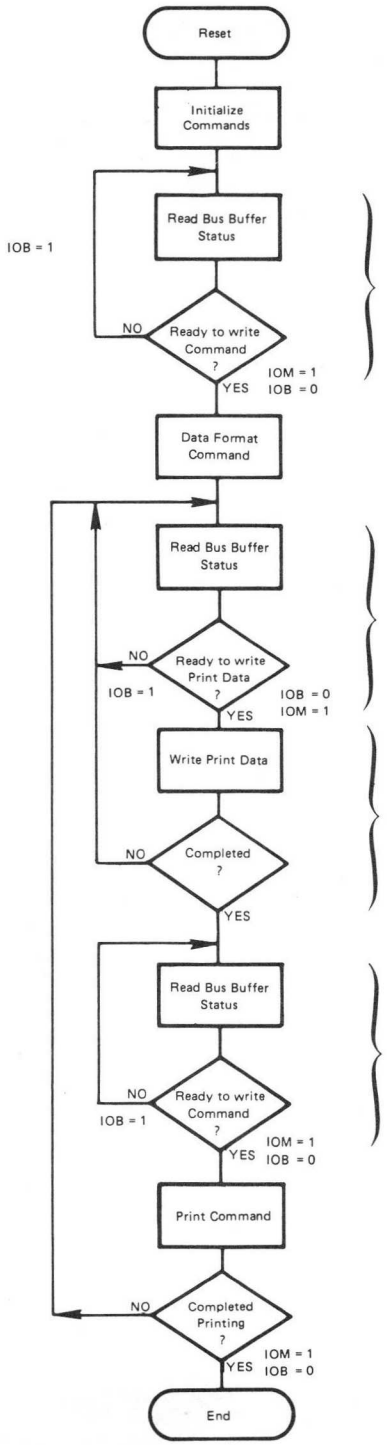
The binary number indicated by n_0 through n_3 determines the number of continuous line feeds which will be performed. After the last line feed, the contents of the column buffer is reset to 20 hexadecimal (blank). During this operation no other commands are accepted.

c_1	c_0	OPERATION	MODEL
0	0	Performs Fast Feed Only	512,522,542
0	1	After Fast Feed, Perform Partial Cut	522
1	0	After Fast Feed, Perform Stamp and Full Cut	522
1	1	After Fast Feed, Perform Slip Release	542

WRITE PRINT DATA COMMAND

After each character is written into the column buffer, the column printer is incremented by one. Do not exceed the column capacity defined in the printer format command. The following table defines the relationship between print data (d_0 through d_6) and the character set.

				(MSB) d_6	0	0	1	1	1	1
				d_5	1	1	0	0	1	1
				d_4	0	1	0	1	0	1
d_3	d_2	d_1	(LSB) d_0		2	3	4	5	6	7
0	0	0	0	0						
0	0	0	1	1						
0	0	1	0	2						
0	0	1	1	3						
0	1	0	0	4						
0	1	0	1	5						
0	1	1	0	6						
0	1	1	1	7						
1	0	0	0	8						
1	0	0	1	9						
1	0	1	0	A						
1	0	1	1	B						
1	1	0	0	C						
1	1	0	1	D						
1	1	1	0	E						
1	1	1	1	F						



Power-on Reset

Initialize the μPD781. (Reset the Column Buffer and set the Print-Head at the left/right side.)

Check the Bus Buffer Status.

Indicate the format of the Column Buffer. (40 columns, 18 columns x 1, 18 columns x 2.)

Check the Bus Buffer Status.

Write up to maximum number of characters into the column buffer.

Check the Bus Buffer Status.

Print the entire contents of the column buffer. Indicate "Line Feed" or "Slip Release."

9

DOT MATRIX PRINTER CONTROLLER

DESCRIPTION

The μPD782 is an LSI Dot Matrix Printer Controller chip which contains all the circuitry and control functions for interfacing an 8-bit processor to the Epson Model 210, 220 and 240 Dot Matrix Printers. These printers are capable of printing up to 31 columns per row with 7 x 7 dot matrix. The μPD782 is ideally suited for low-cost Electronic Cash Registers (ECR) and Point of Sale (POS) systems because it frees the processor from direct control of the printer and simplifies I/O software.

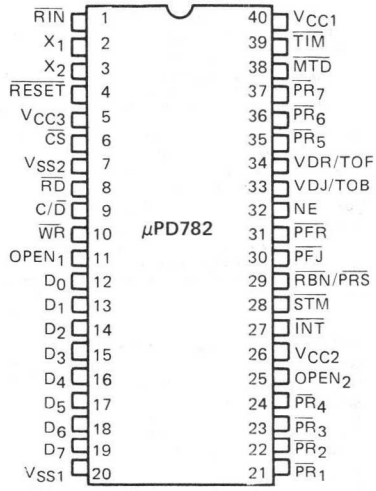
There are nine separate instructions, which the μPD782 will execute. Each of these instructions requires a single 8-bit byte from the processor to be executed. Upon receipt of the instruction, the μPD782 assumes the control of the printer, increments the position of the print head, activates the print solenoids, performs line feeds in either receipt or journal mode (or both), and performs all these operations for an entire print line.

The μPD782 contains its own on-board character generator of 96 symbols. It contains a 31 column printer buffer and is capable of supplying status information to the host processor on both the controller itself as well as the printer. After the character buffer is loaded from the host processor the entire row is printed out with a single print command.

FEATURES

- Compatible with most Microprocessors Including 8080A, 8085A, Z-80™ and others
- Capable of Interfacing to Epson Model 210, 210S, 220 and 240 Printers
- Print Technique – Serial Dot Matrix
- Print Font – 7 x 7 Dot Matrix
- Column Print Capacity
  - Model 210 – 31 Characters with 1 Dot Spacing; 26 Characters with 2 Dot Spacing
  - Model 210S – 28 Characters with 1 Dot Spacing; 23 Characters with 2 Dot Spacing
  - Model 220 – 14 + 14 Characters in Receipt/Journal Mode; 31 Characters in Normal Mode
  - Model 240 – 31 Characters
- 96 Character Set (Alphanumerics Plus Symbols)
- Print Speed – Approximately 3 Lines/Sec.
- Paper Feed Receipt and Journal; Fast Feed
- Paper Release and Ink Ribbon Change-Over Outputs
- Motor Error and Write Request Interrupt
- On-Board 6 MHz Oscillator (External Crystal Required)
- Operates from a Single +5V Power Supply (NMOS Technology)
- Available in 40 Pin Plastic Package

PIN CONFIGURATION



PIN NAMES

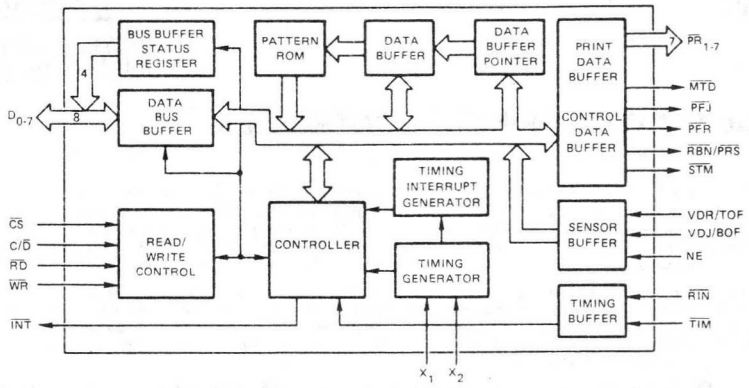
$\overline{RIN}$	Reset In
X_1 X_2	Crystal Inputs
$\overline{RESET}$	Reset
V_{CC1-3}	DC Power
V_{SS1-2}	Signal Ground
$\overline{CS}$	Chip Select
$\overline{RD}$	Read
$C/\overline{D}$	Command/Data
$\overline{WR}$	Write
$OPEN_{1-2}$	No Connection
D_0-D_7	Data Bus
$\overline{PR}_1$-$\overline{PR}_7$	Print Solenoids
$\overline{INT}$	Interrupt
$\overline{STM}$	Stamp
$\overline{RBN}/\overline{PRS}$	Ribbon/Paper Release
$\overline{PFJ}$	Paper Feed Journal
$\overline{PFR}$	Paper Feed Receipt
NE	Low Paper Detector
VDJ/BOF	Validation J/BOF Sensor
VDR/BOT	Validation R/BOT Sensor
$\overline{MTD}$	Motor Drive
$\overline{TIM}$	Timing Signal

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TM: Z-80 is a registered trademark of Zilog, Inc.

μPD782

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN			I/O	FUNCTION
NUMBER	SYMBOL	NAME		
1	$\overline{RIN}$	Reset In	I	This pin should be connected to the R Sensor from the printer so that it is active-low.
2,3	X_1, X_2	External Crystal Input	I	This is a connection to external crystal (Frequency: 6 MHz). X_1 could also be used as input for external oscillator.
4	$\overline{RESET}$	Reset	I	The Reset signal initializes the μPD782 When $\overline{RESET}$ = 0, the buffer and register contents are: Bus Buffer – (IOM-1, IOB=PSR=0). Column Buffer – All characters in this buffer become $20_{(16)}$ Column Buffer Pointer – It indicates the left side of the buffer.
5, 26 40	V_{CC1-3}	DC Power		These are connected to +5V power supply.
6	$\overline{CS}$	Chip Select	I	If the Chip Select is 0 when the data bus becomes active, it enables the transfer of data between the processor and the μPD782 via the data bus. If it is 1, the data bus goes into High-Impedance state (inactive). However, the operation of the printer is not affected when $\overline{CS}$=1.
7,20	V_{SS1-2}	Signal Ground		
8	$\overline{RD}$	Read	I	The Read Control Signal is used to read controller status or printer status to the host processor. When $\overline{RD}$ = 0, status information is presented.
9	$C/\overline{D}$	Command/ Data Select	I	The $C/\overline{D}$ Select is used to indicate what kind of data is being input/output on the data bus by the host processor. When $C/\overline{D}$=1 in Read Operation, it is a Controller Status and in Write Operation it gives commands. When $C/\overline{D}$=0 in Read Operation it is a Printer Status and in Write Operation it is print data.

PIN IDENTIFICATION (CONT.)

PIN			I/O	FUNCTION
NUMBER	SYMBOL	NAME		
10	$\overline{WR}$	Write	I	The Write Control Signal is used to write commands or print data to the μPD782. When $\overline{WR}$=0, data on the data bus is written into the μPD782.
12-19	D_{0-7}	Data Bus	I/O 3-State	It is an 8-bit bi-directional data bus and is used to transfer the data between the host processor and the μPD782.
11,25	$OPEN_{1-2}$	No Connection		These pins must be open. Do not connect them to +5V, GND or any other signals.
21-24, 35-37	$\overline{PR}_1$-$\overline{PR}_7$	Print Solenoid	O	These are drive signals for the print solenoids. When these signals are 0, the print solenoid should be activated. They are synchronized with the timing signal ($\overline{TIM}$), which is issued from the printer.
39	$\overline{TIM}$	Timing Signal	I	The timing signal is issued from the printer. It is used to generate and synchronize all the basic printer operations such as paper feed, paper cut, etc.
27	$\overline{INT}$	Interrupt	O	There are two reasons for this signal to go low. One is when the μPD782 is ready to receive data into the Data Buffer. It gets reset after the first byte of data is loaded. The other reason is the motor error during the printing or line feed. It will get set if the paper is jammed or if the print solenoid is kept on for more than 20 ms. It gets clear by the initialize command.
28	$\overline{STM}$	Stamp	O	Stamp output for Model M-220 printer. After the stamp command is given, this signal goes low for 200 ms.
29	$\overline{RBN}/\overline{PRS}$	Ribbon/ Paper Release	O	This is low active signal. For Model 210 and 210S it will select red ribbon. For Model 240 it will cause slip release. It is activated by print command.
30	$\overline{PFJ}$	Paper Feed Journal	O	This is the drive signal for the journal paper feed for Model 220 and for normal paper feed for other models. It is a low active signal.
31	$\overline{PFR}$	Paper Feed Receipt	O	This is the drive signal for the receipt paper feed for Model 220 and should be left open for other models.
32	NE	Low Paper Detector	I	This signal indicates a low paper condition in Model 220 and is active high.
33,34	VDR/TOF VDJ/TOB	Validation Sensors	I	These signals indicate the position of the print head in the printer. For Model 220 – right and left position. For Model 240 – top and bottom.
38	$\overline{MTD}$	Motor Drive	O	This signal activates the motor in the printer and is active low.

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μPD782

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +125°C
Voltage On Any Pin . . . . . -0.5 to +7 Volts①

Note: ① With Respect to Ground.

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

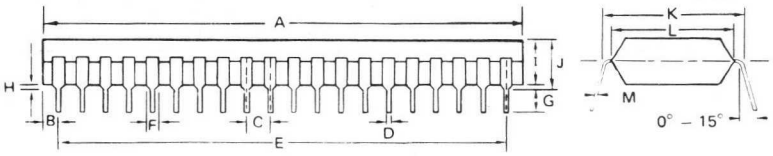
*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC1-3} = +5V ± 5%; V_{SS1-2} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage (All except XTAL 1, XTAL 2, $\overline{RESET}$)	V_{IH1}	2.0		VCC	V	
Input High Voltage (XTAL 1, XTAL 2, RESET)	V_{IH2}	3.5		V_{CC}	V	
Input Low Voltage (All except XTAL 1, XTAL 2)	V_{IL}	-0.5		0.8	V	
Output High Voltage (D_{0-7})	V_{OH1}	2.4			V	I_{OH} = -400 μA
Output High Voltage (All Other Outputs)	V_{OH2}	2.4			V	I_{OH} = -50 μA
Output Low Voltage (D_{0-7})	V_{OL1}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (All Other Outputs except D_{0-7})	V_{OL2}			0.45	V	I_{OL} = 1.6 mA
Low Input Source Current (VDR/$\overline{BOF}$, VDL/TOF, NE, $\overline{TIM}$)	I_{LI1}			0.4	mA	V_{IL} = 0.8V
Low Input Source Current ($\overline{RESET}$)	I_{LI2}			*0.2	mA	V_{IL} = 0.8V
Input Leakage Current (RL, RR, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, C/$\overline{D}$)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Output Leakage Current (D_{0-7}, High Impedance State)	I_{OL}			±10	μA	V_{SS} + 0.45 ≤ $V_{IN} \leq V_{CC}$
Total Supply Current (I_{CC1} + I_{CC2} + I_{CC3})	I_{CC}		65	135	mA	T_a = 25°C

PACKAGE OUTLINE μPD782C



ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

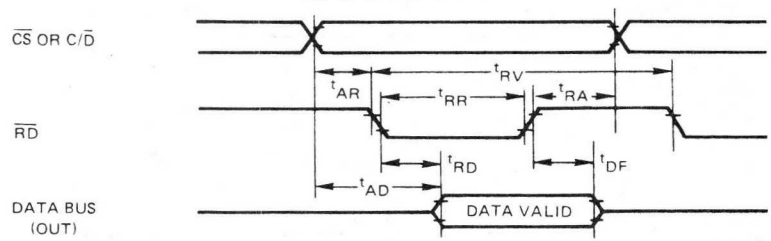
AC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC1-3} = +5V ± 5%; V_{SS1-2} = 0V

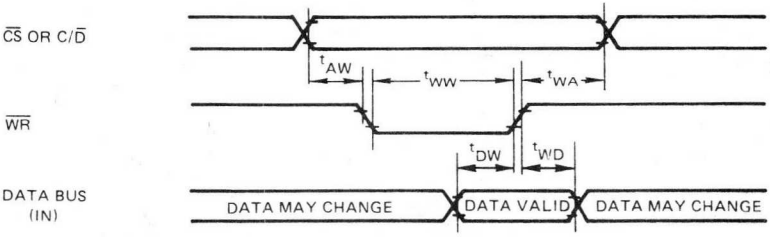
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ OPERATION						
$\overline{CS}$, C/$\overline{D}$ Setup to $\overline{RD}$ ↓	t_{AR}	0			ns	D_{0-7} Input
CS, C/$\overline{D}$ Hold After $\overline{RD}$ ↑	t_{RA}	0			ns	
$\overline{RD}$ Pulse Width	t_{RR}	250		5000	ns	
$\overline{CS}$, C/$\overline{D}$ to Data Out Delay	t_{AD}			180	ns	
$\overline{RD}$ ↓ to Data Out Delay	t_{RD}			180	ns	
$\overline{RD}$ ↑ to Data Float Delay	t_{DF}	10		100	ns ns	
Recovery Time Between Reads And/Or Write	t_{RV}	1			μs	
WRITE OPERATION						
$\overline{CS}$, C/$\overline{D}$ Setup to $\overline{WR}$ ↓	t_{AW}	0			ns	D_{0-7} Output C_L = 100 pF
$\overline{CS}$, C/$\overline{D}$ Hold After $\overline{WR}$ ↑	t_{WA}	0			ns	
$\overline{WR}$ Pulse Width	t_{WW}	250		5000	ns	
Data Setup to $\overline{WR}$ ↑	t_{DW}	150			ns	
Data Hold After $\overline{WR}$ ↑	t_{WD}	0			ns	
PRINT OPERATION						
$\overline{RIN}$ ↓ to $\overline{T}_1$ Preset Time	t_{RT}			140	μs	6 MHz Crystal
$\overline{TIM}$ ↓ to $\overline{PR}_{1-7}$ ↕ Delay	t_{TP}	40		50	μs	
$\overline{RBN}$ ↓ to $\overline{MTD}$ ↓ Delay	t_{RM}		5		μs	
$\overline{RIN}$ ↓ to $\overline{RBN}$ ↑ Delay	t_{RRBN}	10		15	μs	
$\overline{TIM}$ ↓ to $\overline{PFJ}$, $\overline{PFR}$ ↕ Delay	t_{TF}	135		500	μs	
$\overline{TIM}$ ↓ to $\overline{SLR}$ ↕ Delay	t_{TR}	365		385	μs	
$\overline{RIN}$ ↓ to $\overline{STM}$ ↓ Delay	t_{RS}		12.5		μs	
$\overline{T}_{125}$ ↓ to $\overline{STM}$ ↑ Delay	t_{TS}		42.5		μs	
Stamp Time	t_{STM}	150.03		200.03	ms	
$\overline{TIM}$ ↓ to $\overline{MTD}$ ↑	t_{TM}			510	μs	

TIMING WAVEFORMS

READ OPERATION



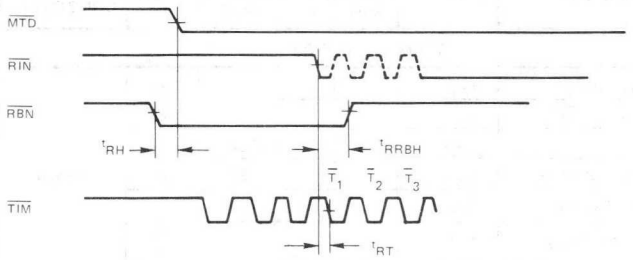
WRITE OPERATION



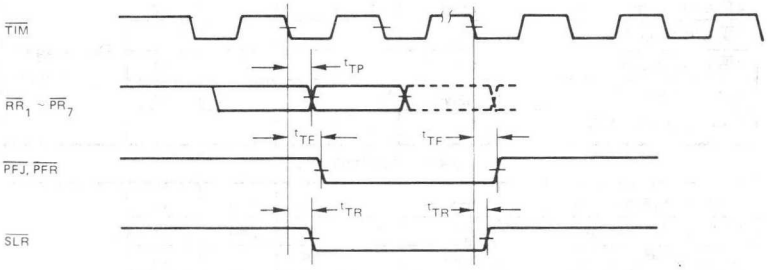
9

TIMING WAVEFORMS
(CONT.)

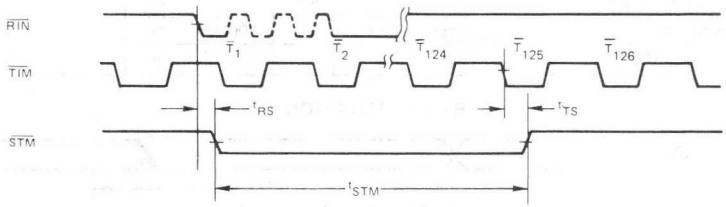
PRINT OPERATION



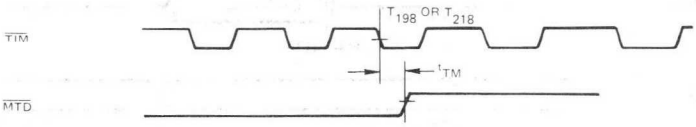
LINE FEED OPERATION



STAMP OPERATION



MOTOR ENABLE



COMMANDS

All transfer of information between the μPD782 and the host processor is via the data bus, and the four (4) control signals, $\overline{CS}$, C/$\overline{D}$, $\overline{WR}$ and $\overline{RD}$. The four control signals determine what type of data transfer will occur on the data bus.

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	DATA BUS	OPERATION
0	0	0	0	–	Inhibited
0	0	1	0	Print Data	Write Data into Column Buffer
0	0	0	1	Printer Status	Read Printer Status
0	0	1	1	–	No Operation
0	1	0	0	–	Inhibited
0	1	1	0	Command	Write Command for Printer
0	1	0	1	Controller Status	Read Controller Status
0	1	1	1	–	No Operation
1	X	X	X	–	Disable μPD782

Before issuing any new command or loading new data into the column buffer, the host processor should check the controller status bits IOM, IOB and PSR. No new operation should be performed if IOB bit indicates that the μPD782 is busy.

CONTROLLER STATUS REGISTER

X	X	X	X	X	IOM	IOB	PSR

PRINTER STATUS REGISTER

S	T	V	X	X	X	X	M

COMMAND DESCRIPTION

COMMAND	DATA BUS							
	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Initialize	0	0	0	1	0	0	0	0
Request Printer Status	0	0	0	0	X	X	X	X
Printer Format	0	1	a	b_4	b_3	b_2	b_1	b_0
Increment Column Printer	0	0	1	n_4	n_3	n_2	n_1	n_0
Print	1	0	LFJ	LFR	X	R	ST	SL
Fast Feed	1	1	k_1	k_0	m_3	m_2	m_1	m_0
Write Print Data	X	d_6	d_5	d_4	d_3	d_2	d_1	d_0

Note: X = Don't Care

CONTROLLER STATUS REGISTER

IOM – Input/Output Buffer Mode

The IOM flag indicates the direction of data on the data bus. If IOM=1 data is from processor to μPD782 (write into μPD782). If IOM=0 data is from μPD782 to processor (read from μPD782). Immediately after reading printer status, IOM goes from 0 to 1.

IOB – Input/Output Buffer Busy

The IOB flag indicates when the I/O buffer is busy and an operation is in process. If IOB=1 I/O buffer is busy and no new command should be performed. If IOB=0 μPD782 is ready to accept new command.

PSR – Printer Status Ready

The PSR flag indicates that the printer status may be read by the processor. If PSR=1 printer status is ready to be read by processor. If PSR=0 printer status is not ready.

PRINTER STATUS REGISTER

S	T	V	M	OPERATION
1	X	X	X	Status of the input pin 34
X	1	X	X	Status of the input pin 33
X	X	1	X	Status of the input pin 32
X	X	X	1	Motor Error – μPD782 will suspend output to $\overline{PR}_1$-$\overline{PR}_7$ solenoids and turn the motor off. Cleared by the initialize command.

INITIALIZE COMMAND

This command is the same as RESET signal. It clears the Data Buffer (set to blank 20H), set the Data Buffer Pointer to the left side. It also resets the motor error flag, and clears interrupt.

REQUEST PRINTER STATUS COMMAND

This command will latch the status of the input pins 32, 33 and 34 in the Printer Status Register. It must be followed by a Printer Status Read Operation. No other command will be accepted until the printer status is read.

PRINTER FORMAT COMMAND

This command sets the controller for the appropriate printer model and controls the format and timing of printing and line feed for different models of Epson printer. It should be issued after initialize command but before any other command.

a = 0 – 1 dot spacing between characters
a = 1 – 2 dot spacing between characters – only for Model 210 and 210S

b_4	b_3	b_2	b_1	b_0	MODEL PRINTER
1	1	1	1	0	M-210
1	1	1	0	1	M-210S
0	1	0	1	1	M-220 – Journal/Receipt mode(14 + 14 characters)
1	1	0	1	1	M-220 – One line print (31 characters)
1	0	1	1	1	M-240

COMMAND DESCRIPTION (CONT.)

INCREMENT DATA BUFFER POINTER COMMAND

The Data Buffer Pointer is incremented to the right by the binary value indicated by n_0 through n_4. In case of Model 220 in journal/receipt mode the pointer can only move within the receipt or journal side depending upon which side it is presently located.

PRINT COMMAND

The entire Data Buffer is printed and after the print operation is completed the contents of the buffer are reset to 20H (blank). During the execution of the print command no other commands are allowed.

Model 220

LFJ	LFR	OPERATION
0	0	After printing both receipt or journal line feed
0	1	After print performs line feed on receipt side only
1	0	After print performs line feed on journal side only
1	1	Print only
ST	1	No stamp
	0	The receipt side performs line feed 11 times after printing a line and the stamp solenoid is activated

Model 210, 210S

LFJ	R	OPERATION
0	X	After printing performs line feed
1	X	Print only
X	0	Print ribbon set to red
X	1	Print ribbon set to black

Model 240

LFJ	SL	OPERATION
0	X	After printing performs line feed
1	X	Print only
X	0	After print performs slip release (only 29 characters allowed in data buffer)
X	1	No slip release

FAST FEED COMMAND

The binary number indicated by m_3 through m_0 determines the number of continuous line feeds which is performed.

For Model 220

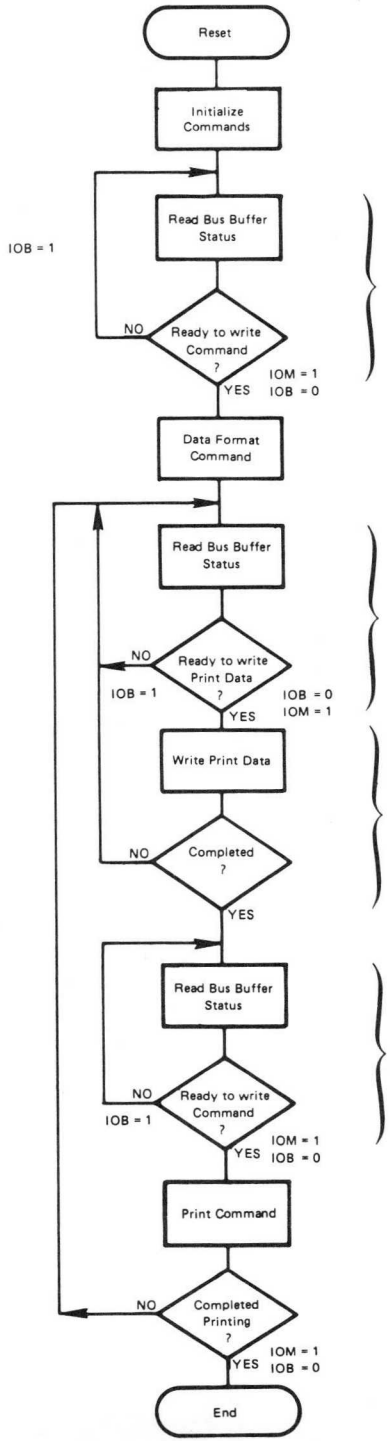
k_1	k_0	OPERATION
0	0	Receipt and Journal line feed
0	1	Receipt line feed only
1	0	Journal line feed only

WRITE PRINT DATA COMMAND

After each character is written into the column buffer, the column printer is incremented by one. Do not exceed the column capacity defined in the printer format command. The following table defines the relationship between print data (d_0 through d_6) and the character set.

				(MSB) d_6	0	0	1	1	1	1
				d_5	1	1	0	0	1	1
				d_4	0	1	0	1	0	1
d_3	d_2	d_1	(LSB) d_0		2	3	4	5	6	7
0	0	0	0	0						
0	0	0	1	1						
0	0	1	0	2						
0	0	1	1	3						
0	1	0	0	4						
0	1	0	1	5						
0	1	1	0	6						
0	1	1	1	7						
1	0	0	0	8						
1	0	0	1	9						
1	0	1	0	A						
1	0	1	1	B						
1	1	0	0	C						
1	1	0	1	D						
1	1	1	0	E						
1	1	1	1	F						

OPERATING PROCEDURES



Power-on Reset

Initialize the μPD782. (Reset the Column Buffer and set the Print-Head at the left side.)

Check the Bus Buffer Status.

Indicate the format of the Column Buffer. Set the controller mode for the printer model.

Check the Bus Buffer Status.

Write up to maximum number of characters into the column buffer.

Check the Bus Buffer Status.

Print the entire contents of the column buffer. Indicate "Line Feed" or "Slip Release."

9

NOTES

NEC
μPD3301-1
μPD3301-2
PRELIMINARY

PROGRAMMABLE CRT CONTROLLER

DESCRIPTION

The μPD3301 is an LSI chip designed for use in CRT controllers. It contains a synchronous signal generator, row buffer, and attribute memory. This CRT controller is capable of handling not only black and white CRT, but also color CRT. The μPD3301 provides control signals which simplify the design of the external circuitry needed in the systems. Thus, this device is a versatile controller that relieves the main CPU (and users) of many of the control burdens associated with implementing a CRT interface.

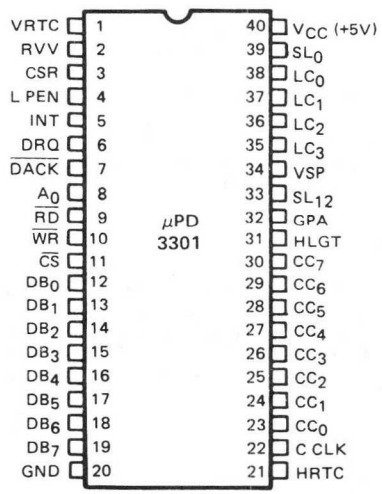
There are 8 separate commands which the μPD3301 will execute. Some of these commands require multiple bytes to fully specify the operation which the processor wishes the CRT controller to perform. The following commands are available:

- RESET
- SET INTERRUPT MASK
- RESET INTERRUPT
- STOP DISPLAY
- READ LIGHT PEN
- RESET COUNTERS
- START DISPLAY
- LOAD CURSOR POSITION

FEATURES

- Programmable Screen and Character Format Capabilities;
  - Characters per Row (up to 80 characters/row)
  - Lines per Character (up to 32 lines/character)
  - Rows per Frame (up to 64 rows/frame)
  - Horizontal Retrace Time
  - Vertical Retrace Time
  - Blinking Time
  - DMA Control Mode
  - Cursor Control Mode
- Three Independent Visual Field Attribute Modes such as;
  - Transparent Attribute Color Mode
  - Transparent Attribute Black and White Mode
  - Non-Transparent Attribute Black and White Mode
- 12 Independent Field Attribute Functions such as;
  - Vertical Line
  - Over-Line
  - Reverse Video
  - Secret
  - Blue
  - Red
  - Under-Line
  - High-Light
  - Blinking
  - General Purpose
  - Green
  - General Purpose Color
- Light Pen Detection
- Maximum 256 Different Characters Control Capability
- Fully Bus Compatible with 8080
- 3 MHz Single Clock Input
- Single Power Supply, +5V N-MOS Technology
- Available in 40 pin Plastic and Ceramic Dual-In-Line Packages

PIN CONFIGURATION

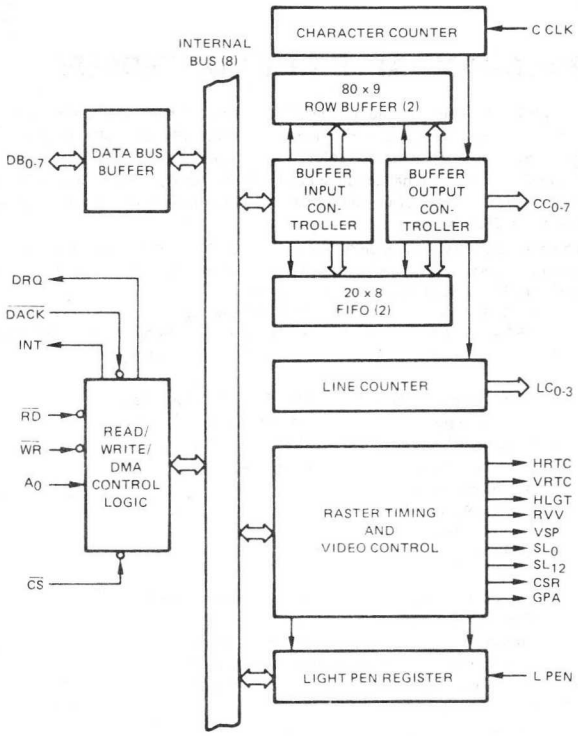


PIN NAMES

VRTC	Vertical Retrace
RVV	Reverse Video
CSR	Cursor
L PEN	Light Pen
INT	Interrupt
DRQ	DMA Request
DACK	DMA Acknowledge
A_0	Address Bus 0
RD	Read
WR	Write
CS	Chip Select
DB_{0-7}	Data Bus 0 to 7
HRTC	Horizontal Retrace
C CLK	Character Clock
CC_{0-7}	Character Codes 0 to 7
HLGT	High-light
GPA	General Purpose Attribute
SL_{12}	Slit Line 12
VSP	Video Suppression
LC_{0-3}	Line Counter 0 to 3
SL_0	Slit Line 0

9

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Character Counter

Counts the characters in a row, up to the number of the characters defined in Characters/Row.

Row Buffer

Consists of a dual RAM buffer. Each buffer can store up to 80 characters. During a DMA operation, the characters are written into the Row Buffer. One of the buffers is used for display. Each character in the buffer is read with Character Clock (C CLK), and the data appears in CC_{0-7}. At the same time, the data on the next row is written into another buffer by DMA control.

Buffer Input/Output Controller

- Writes the characters into the Row Buffer, up to the number defined by Characters/Row.
- Outputs the data from the Row Buffer to CC_{0-7}.
- Writes the attributes and special control character codes into the FIFO, up to the number defined by Attributes/Row.
- Reads the attribute codes from the FIFO and transfers them to the video circuit.
- In case of Non-Transparent Attribute Mode, it distinguishes an ordinary character code from an attribute code among the character data read from the Row Buffer.

FIFO (First Input, First Output)

Consists of a dual RAM buffer. Each buffer can store up to 20 characters. By DMA operation, attribute codes and special control characters are written into the FIFO. One of the buffers is used for display. Whenever the read flag bit for FIFO is detected, an attribute code is read and transferred to the video circuit. And at the same time, the attribute codes in the next row are written into the rest of the buffers (another buffer) by DMA operation.

FUNCTIONAL DESCRIPTION (CONT.)

Line Counter

Counts the events of Rasters/Line, up to the number indicated by Lines/Character.

Raster Timing and Video Control

- Outputs the HRTC based on the Character Counter during the time indicated by Horizontal Retrace Time.
- Outputs the VRTC based on Row Counter which counts up the contents, row by row, during the time indicated by Vertical Retrace Time.
- Outputs HLGT, RVV, VSP, SL_0, SL_{12}, GPA based on attribute codes transferred from the Buffer Output Controller.
- Outputs the CSR based on the Blinking Time etc. at the position indicated by Cursor Address.

Light Pen Register

Memorizes a row address and column address when the L PEN signal is input. By using READ LIGHT PEN instruction, the CPU can read the contents.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
All Output Voltages . . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −0.5 to +7 Volts
Supply Voltage V_{CC} . . . . . −0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.6 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	DB_{0-7}: I_{OH} = -150 μA, All Others: -80 μA
Low Level Input Leakage	I_{IL}			-10	μA	V_{IN} = 0V
High Level Input Leakage	I_{IH}			+10	μA	V_{IN} = V_{CC}
Low Level Output Leakage	I_{OL}			-10	μA	V_{OUT} = 0V
High Level Output Leakage	I_{OH}			+10	μA	V_{OUT} = V_{CC}
Power Supply Current	I_{CC}		90		mA	

CAPACITANCE

T_a = 25°C; V_{CC} = 0V

PARAMETER	SYMBOL	LIMITS		UNIT	TEST CONDITIONS
		MIN	MAX		
Input Capacitance	C_{IN}		10	pF	fc = 1 MHz, All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}		20	pF	

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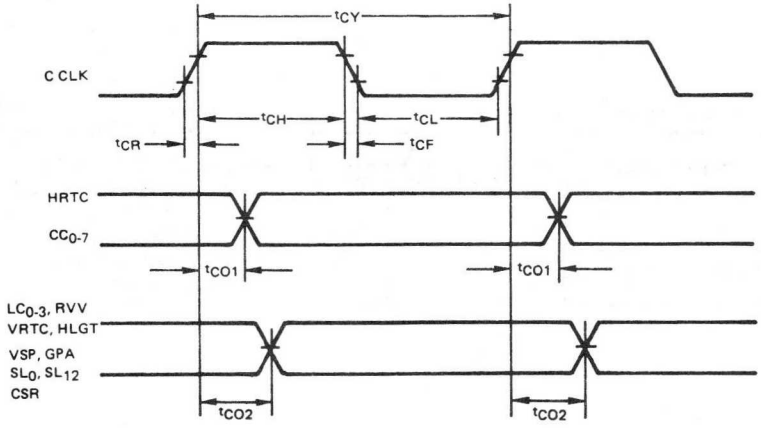
AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$

PARAMETER		SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Cycle Time	μPD3301-1	t_{CY}	0.5	10	μs	
	μPD3301-2	t_{CY}	0.38	10	μs	
Clock High Level		t_{CH}	150		ns	
Clock Low Level		t_{CL}	150	1000	ns	
Clock Rise Time		t_{CR}	5	30	ns	
Clock Fall Time		t_{CL}	5	30	ns	
Output Delay from C CLK ↑		t_{CO1}	0	150	ns	1TTL + 15 pF: HRTC, CC_{0-7}
Output Delay from C CLK ↑	μPD3301-1	t_{CO2}		400	ns	1TTL + 15 pF: Except HRTC, CC_{0-7}
	μPD3301-2	t_{CO2}		300	ns	
Command Cycle Time		t_E	$2t_{CY} + 200$		ns	$t_{CY} \geq 400$ μs
		t_E	1		μs	$t_{CY} < 400$ μs
A_0, $\overline{CS}$ Set Up Time to $\overline{WR}$		t_{AW}	0		ns	
A_0, $\overline{CS}$ Hold Time to $\overline{WR}$		t_{WA}	0		ns	
$\overline{WR}$ Pulse Width		t_{WW}	200		ns	
Data Set Up Time to $\overline{WR}$		t_{DW}	150		ns	
Data Hold Time to $\overline{WR}$		t_{WD}	30		ns	
$\overline{DACK}$ ↓ Set Up Time to $\overline{WR}$		t_{KW}	0		ns	
$\overline{DACK}$ ↑ Hold Time to $\overline{WR}$		t_{WK}	0		ns	
DRQ Delay from $\overline{DACK}$ ↓		t_{KQ}	0	250	ns	1TTL + 50 pF
INT Delay from $\overline{WR}$ ↑		t_{WI}	$t_{CY} + 20$	$2t_{CY} + 300$	ns	1TTL + 50 pF
INT Delay from C CLK ↑		t_{CI}		300	ns	1TTL + 50 pf
A_0, $\overline{CS}$ Set Up Time to $\overline{RD}$		t_{AR}	0		ns	
A_0, $\overline{CS}$ Hold Time to $\overline{RD}$		t_{RA}	0		ns	
$\overline{RD}$ Pulse Width		t_{RR}	300		ns	
Data Access Time from $\overline{RD}$ ↓		t_{RD}	0	250	ns	$C_L = 100$ pF
Data Float Delay from $\overline{RD}$ ↑		t_{DR}		150	ns	$C_L = 100$ pF
			20		ns	$C_L = 15$ pF

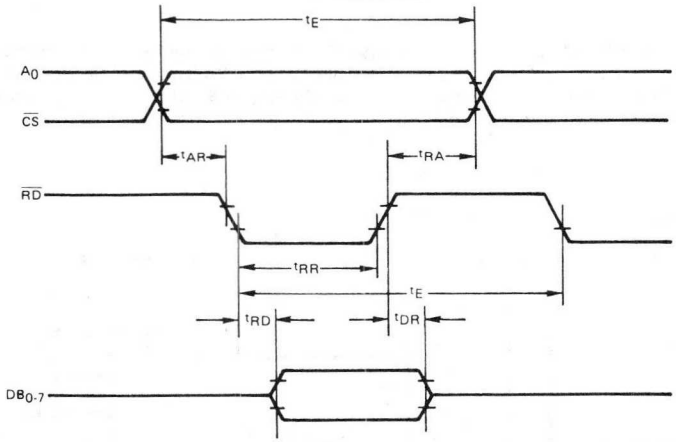
TIMING WAVEFORMS

CLOCK AND OUTPUT DELAY

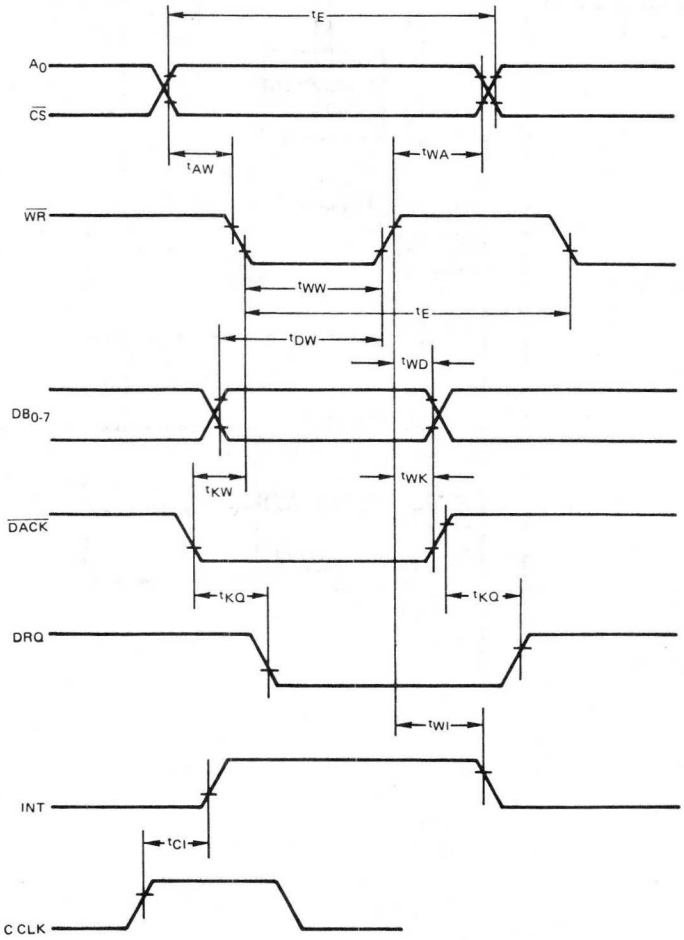


TIMING WAVEFORMS (CONT.)

READ OPERATION



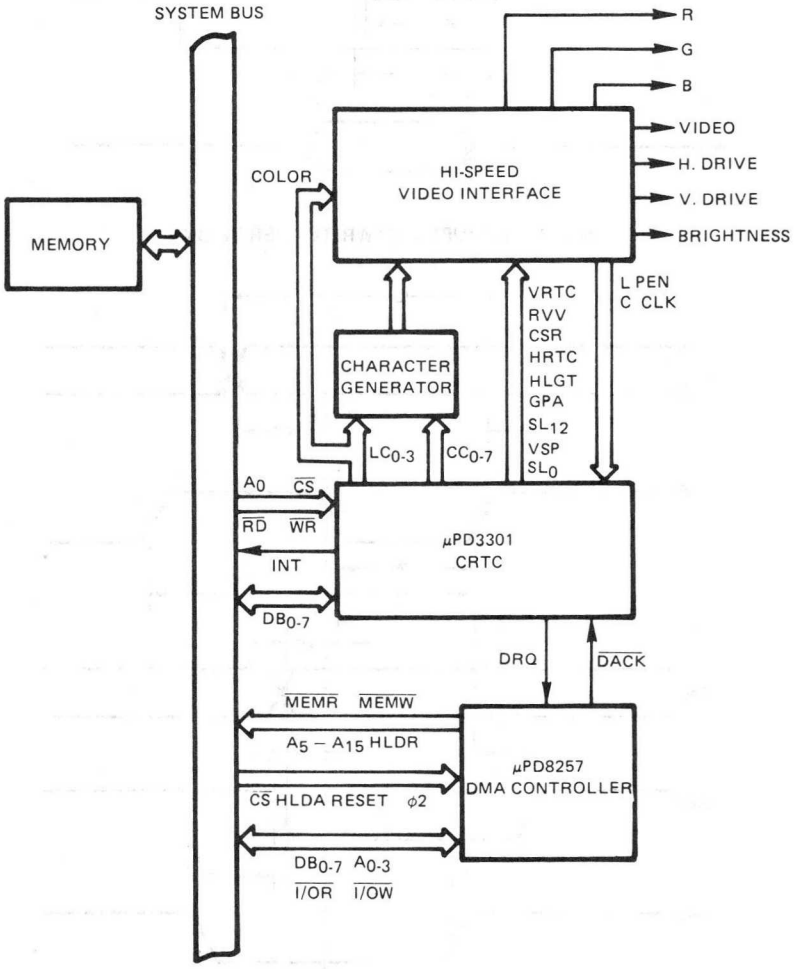
DMA, INTERRUPT AND WRITE OPERATION



9

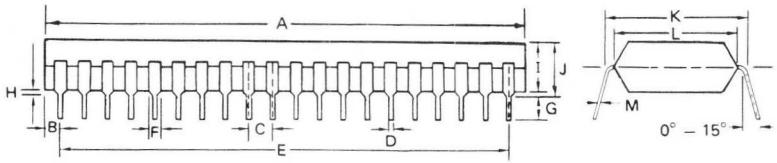
SYSTEM CONFIGURATION

The data is transferred from the external memory which contains the information about characters and attributes to the Row Buffer under the control of μPD8257 DMA Controller. The data read from the Row Buffer are Video Control Outputs and ROM Address Signal Outputs toward External Character Generator. The μPD3301 also outputs horizontal and vertical retrace signals.



PACKAGE OUTLINES

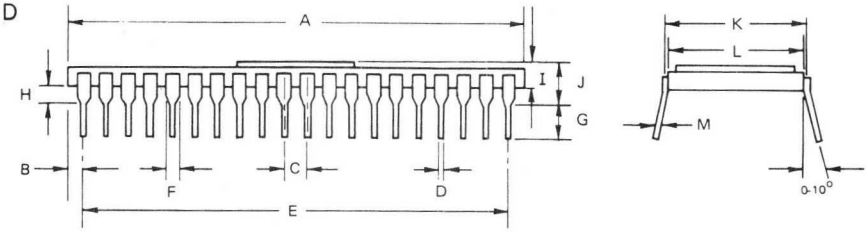
μPD3301C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.028 MAX.
B	1.62 MAX.	0.064 MAX.
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.2 MIN.	0.047 MIN.
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.019 MIN.
I	5.22 MAX.	0.206 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24 TYP.	0.600 TYP.
L	13.2 TYP.	0.520 TYP.
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

μPD3301D



(CERAMIC)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.03 MAX.
B	1.62 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.0019

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8-BIT SERIAL OUTPUT A/D CONVERTER

DESCRIPTION

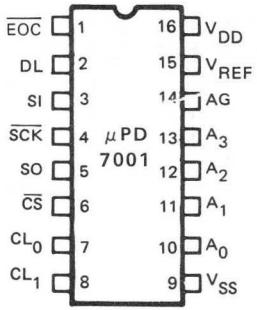
The μPD7001 is a high performance, low power 8-bit CMOS A/D converter which contains a 4 channel analog multiplexer and a digital interface circuit for serial data I/O. The A/D converter uses a successive approximation as a conversion technique.

A/D conversion system can be easily designed with the μPD7001 including all circuits for A/D convertion. The μPD7001 can be directly connected to 8-bit or 4-bit microprocessors.

FEATURES

- Single chip A/D Converter
- Resolution: 8 Bit
- 4 Channel Analog Multiplexer
- Auto-Zeroscale and Auto-Fullscale Corrections without any external components
- Serial Data Transmission
- High Input Impedance: 1,000 MΩ
- Single +5V Power Supply
- Low Power Operation
- Available in 16 Pin Plastic Package
- Conversion Speed 140 μs Typ.

PIN CONFIGURATION



(TOP VIEW)

PIN NAMES

$\overline{EOC}$*	End of Conversion
DL	Analog Channel Data Load
SI	Serial Data Input
$\overline{SCK}$	Serial Data Clock
SO*	Serial Data Output
$\overline{CS}$	Chip Select
CL_0,CL_1	Successive Approximation Clock
V_{SS}	Digital Ground
A_0,A_1,A_2,A_3	Analog Inputs
AG	Analog Ground
V_{REF}	Reference Voltage Input
V_{DD}	+5V

*Open Drain

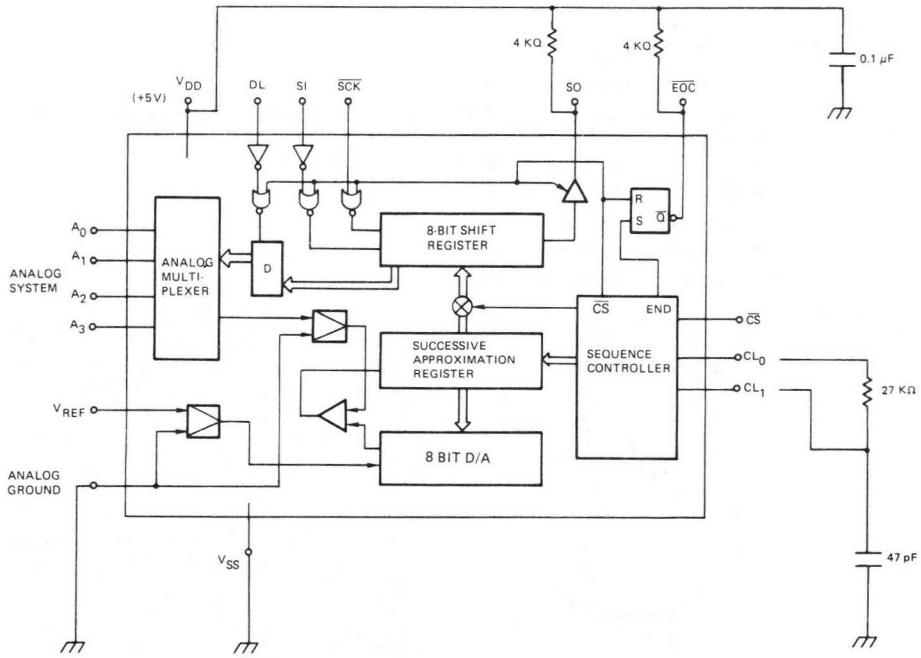
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μPD7001

FUNCTIONAL DESCRIPTION

The 4 channel analog inputs are selected by the 2-bit signal which is applied to a serial input and latched with a DL signal. The converted 8-bit digital signals are output from an open collector serial output (SO). The serial digital signals are synchronized with an external clock signal applied to a $\overline{SCK}$ terminal. The internal sequence controller controls A/D conversion by initiating a conversion cycle at a rise of the Chip Select ($\overline{CS}$). At the final step of each A/D conversion cycle the converted data is transmitted to an 8-bit shift register and immediately the next conversion cycle is started. This results in storage of the newest data in a shift register. At the final step of the first A/D conversion cycle, an end of conversion signal ($\overline{EOC}$) is output indicating that the converted data is stored in a shift register. At a low level (active) of the chip select, the sequence controller and $\overline{EOC}$ are reset and the A/D conversion is stopped.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-0°C to +70°C
Storage Temperature	-65°C to +125°C
Analog Input Voltage	-0.3 to V_{DD} +0.3 Volts
Reference Input Voltage	-0.3 to V_{DD} +0.3 Volts
Digital Input Voltage	-0.3 to +12 Volts
Max. Pull-up Voltage	+12 Volts
Supply Voltages	-0.3 to +7 Volts
Power Dissipation	200 mW

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

AC CHARACTERISTICS

$T_a = 25 \pm 2°C$; $f_{CK} = 400$ kHz; $V_{DD} = +5V$; ①

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
$\overline{EOC}$ Hold Time	t_{HECS}	0			μs	$\overline{EOC}$ to $\overline{CS}$
$\overline{CS}$ Setup Time	t_{SCSK}	12.5			μs	$\overline{CS}$ to $\overline{SCK}$, ①
Address Data Setup Time	t_{SIK}	150			ns	
Address Data Hold Time	t_{HKI}	100			ns	
High Level Serial Clock Pulse Width	t_{WHK}	400			ns	
Low Level Serial Clock Pulse Width	t_{WLK}	400			ns	
Data Latch Hold Time	t_{HKDL}	200			ns	$\overline{SCK}$ to DL
Data Latch Pulse Width	t_{WHDL}	200			ns	
Serial Data Delay Time	t_{DKO}			500	ns	$\overline{SCK}$ to SO, $R_L = 3K$, ② $C_L = 30$ pF
Delay Time to Floating SO	t_{FCSO}			250	ns	$\overline{CS}$ to High Impedance SO
$\overline{CS}$ Hold Time	t_{HKCS}	200			ns	

Notes: ① At a low level of $\overline{CS}$ the data is exchanged with external digital circuit and at a high level of $\overline{CS}$ the μPD7001 performs A/D conversion and does not accept any external digital signal. However, 5 pulses of internal clock are needed before digital data output and then the μPD7001 remains at the previous state of high level $\overline{CS}$.

The rating corresponds to the 5 pulses of clock signal.

t_{SCSK} (Min.) = $5/f_{CK}$

② The serial data delay time depends on load capacitance and pull-up resistance.

DC CHARACTERISTICS

$T_a = 25 \pm 2°C$; $V_{DD} = +5V \pm 10\%$; $V_{REF} = 2.5V$; $f_{CK} = 400$ kHz.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Resolution			8		Bit	$V_{DD} = 5V$ $V_{REF} = 2.25$ to $2.75V$
Non Linearity				0.8	%FSR	$V_{DD} = 5V$ $V_{REF} = 2.25$ to $2.75V$
Full-Scale Error				2	LSB	$V_{DD} = 5V$ $V_{REF} = 2.25$ to $2.75V$
Full-Scale Error Temp. Coefficient			30		ppm/°C	$V_{DD} = 5V$ $V_{REF} = 2.25$ to $2.75V$
Zero Error				2	LSB	$V_{DD} = 5V$ $V_{REF} = 2.25$ to $2.75V$
Zero Error Temp. Coefficient			30		ppm/°C	$V_{DD} = 5V$ $V_{REF} = 2.25$ to $2.75V$
Total Unadjusted Error 1	T.U.E. 1			2	LSB	$V_{DD} = 5V$ $V_{REF} = 2.25$ to $2.75V$
Total Unadjusted Error 2	T.U.E. 2			2	LSB	$V_{DD} = 4.5$ to $5.5V$ $V_{REF} = 2.5V$
Analog Input Voltage	V_I	0		V_{REF}	V	①
Analog Input Resistance	R_I		1000		MΩ	$V_I = 0$ to V_{DD}
Conversion Time	t_{CONV}		140		μs	②
Clock Frequency Range	f_{CK}	0.01	0.4	0.5	MHz	
Clock Frequency Distribution	Δf_{CK}		±5	±20	%	$R = 27$ KΩ, $C = 47$ pF ($f_{CK} = 0.4$ MHz)
Serial Clock Frequency	f_{SCK}			1	MHz	③
High Level Voltage	V_{IH}	3.6			V	
Low Level Voltage	V_{IL}			1.4	V	
Digital Input Leakage Current	I_I		1.0	10	μA	$V_I = V_{SS}$ to $+12V$
Low Level Output Voltage	V_{OL}			0.4	V	$I_{OL} = 1.7$ mA
Output Leakage Current	I_L		1.0	10	μA	$V_O = +12V$
Power Dissipation	P_d		5	15	mW	

Notes: ① All digital outputs are put at a high level when $V_I > V_{REF}$.

② The A/D conversion is started with CS going to a high level and at the final step of the first A/D conversion the EOC is at a low.

The conversion time is:

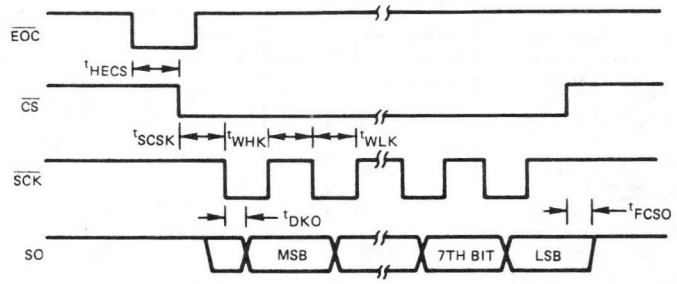
$t_{CONV} = 14 \times 4 \times 1/f_{CK}$

③ For $f_{SCK} > 500$ kHz, the load capacitor (stray capacitance included) and the pull-up resistor which are connected to serial output are required to be not more than 30 pF and 4 KΩ respectively.

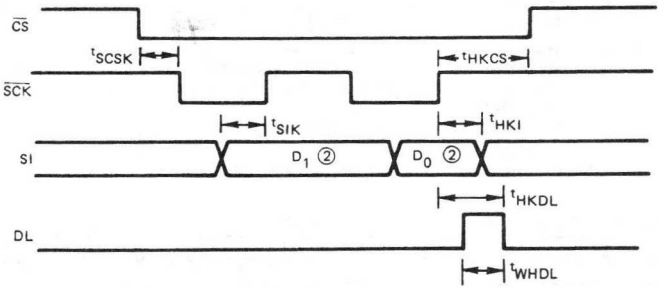
9

TIMING WAVEFORMS

DIGITAL DATA OUTPUT



ANALOG CHANNEL SELECTION



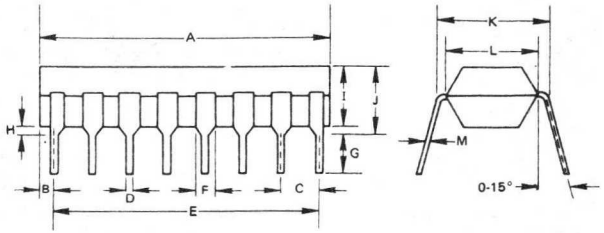
Notes: ① The address set can be performed simultaneously with the digital data outputting.

② Analog Multiplexer Channel Selections:

Analog Input Address	D_0	D_1
A_0	L	L
A_1	H	L
A_2	L	H
A_3	H	H

③ Rise and fall time of the above waveforms should not be more than 50 ns.

PACKAGE OUTLINE μPD7001C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

12-BIT BINARY A/D CONVERTER

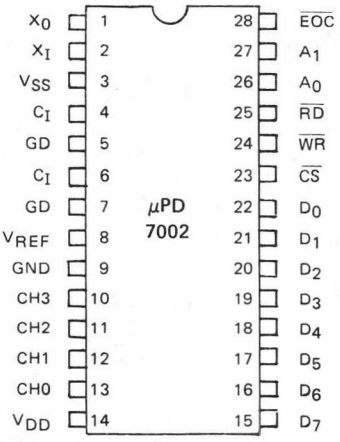
DESCRIPTION

The μPD7002 is a high performance, low power, monolithic CMOS A/D converter designed for microprocessor applications. The analog input voltage is applied to one of the four analog inputs. By loading the input register with the multiplexer channel and the desired resolution (8 or 12 bits) the integrating A/D conversion sequence is started. At the end of conversion $\overline{EOC}$ signal goes low and if connected to the interrupt line of microprocessor it will cause an interrupt. At this point the digital data can be read in two bytes from the output registers. The μPD7002 also features a status register that can be read at any time.

FEATURES

- Single Chip CMOS LSI
- Resolution: 8 or 12 Bits
- 4 Channel Analog Multiplexer
- Auto-Zeroscale and Auto-Fullscale Corrections without any External Components
- High Input Impedance: 1000MΩ
- Readout of Internal Status Register Through Data Bus
- Single +5V Power Supply
- Interfaces to Most 8-Bit Microprocessors
- Conversion Speed: 5 ms
- Power Consumption: 20 mW
- Available in a 28 Pin Plastic Package

PIN CONFIGURATION

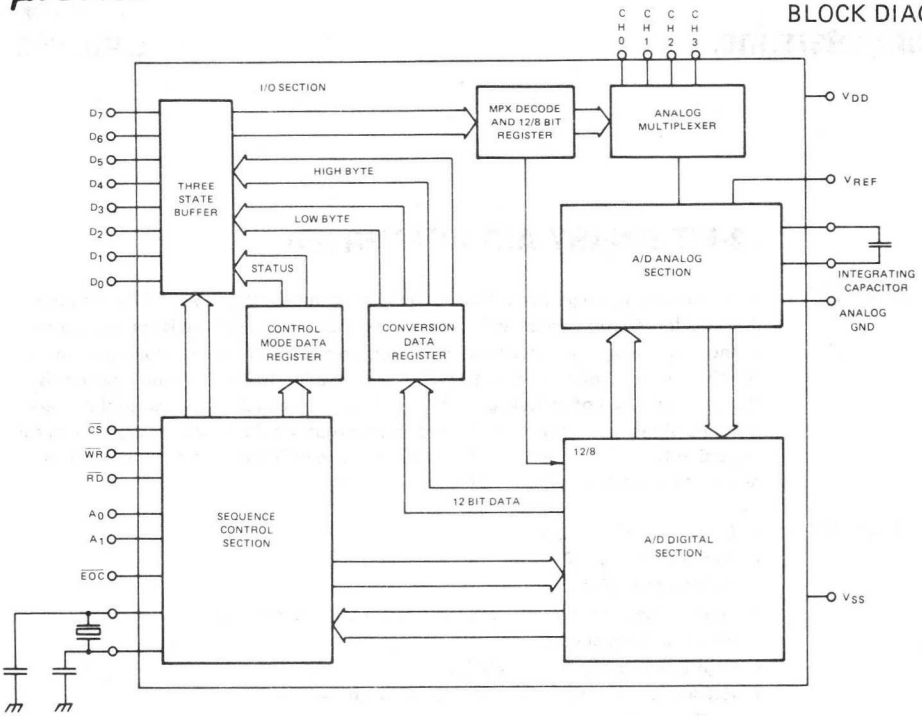


PIN NAMES

X_0,X_I	External Clock Input
V_{SS}	TTL Ground
C_I	Integrating Capacitor
GD	Guard
V_{REF}	Reference Voltage Input
GND	Analog Ground
CH3	Analog Channel 3
CH2	Analog Channel 2
CH1	Analog Channel 1
CH0	Analog Channel 0
V_{DD}	TTL Voltage (+5V)
D_0-D_7	Data Bus
$\overline{CS}$	Chip Select
$\overline{WR}$, $\overline{RD}$	Control Bus
A_0,A_1	Address Bus
$\overline{EOC}$	End of Conversion Interrupt

9

BLOCK DIAGRAM



DC CHARACTERISTICS

T_a = 25 ± 2°C; V_{DD} = +5 ± 0.25V, V_{REF} = +2.50V, f_{CK} = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Resolution			12		Bits	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
Non Linearity			0.05	0.08	%FSR	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
Fullscale Error			0.05	0.08	%FSR	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
Zeroscale Error			0.05	0.08	%FSR	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
Fullscale Temperature Coefficient			10		PPM/°C	V_{DD} = 5V
Zeroscale Temperature Coefficient			10		PPM/°C	V_{DD} = 5V
Analog Input Voltage Range	V_{IA}	0		V_{REF}	V	
Analog Input Resistance	R_{IA}		1000		MΩ	V_{IA} = V_{SS} to V_{DD}
Total Unadjusted Error 1	T.U.E. 1		0.05	0.08	%FSR	V_{REF} = 2.25 to 2.75V, V_{DD} = 5V
Total Unadjusted Error 2	T.U.E. 2		0.05	0.08	%FSR	V_{REF} = 2.5V, V_{DD} = 4.75 to 5.25V
Clock Input Current	I_{XI}		5	50	μA	
Clock Input High Level	V_{XIH}	V_{DD}−1.4			V	
Clock Input Low Level	V_{XIL}			V_{SS}+1.4	V	
High Level Input Voltage	V_{IH}	2.2			V	T_a = −20°C to +70°C
Low Level Input Voltage	V_{IL}			0.8	V	T_a = −20°C to +70°C
High Level Output Voltage	V_{OH}	3.5			V	I_O = −1.6 mA, T_a = −20°C to +70°C
Low Level Output Voltage	V_{OL}			0.4	V	I_O = +16 mA, T_a = −20°C to +70°C
Digital Input Leakage Current	I_I		1	10	μA	V_I = V_{SS} to V_{DD}
High-Z Output Leakage Current	I_{Leak}		1	10	μA	V_O = V_{SS} to V_{DD}
Power Dissipation	Pd		15	25	mW	$f_{CK} \leq$ 1 MHz

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−20°C to +70°C
Storage Temperature	−65°C to +125°C
All Input Voltages	−0.3 to V_{DD} + 0.3 Volts
Power Supply	−0.3 to +7 Volts
Power Dissipation	300 mW
Analog GND Voltage	V_{SS} ± 0.3 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

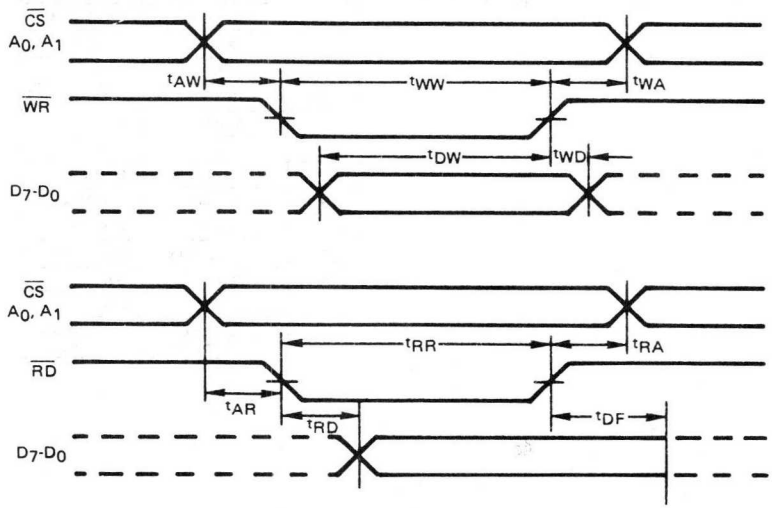
AC CHARACTERISTICS

T_a = 25° ± 2°C; V_{DD} = +5 ± 0.25V; V_{REF} = 2.5V; f_{CK} = 1 MHz; C_{INT} = 0.033 μF

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Conversion Speed (12 bit)	t_{CONV}	8.5	10	15	ms	f_{CK} = 1 MHz
Conversion Speed (8 bit)	t_{CONV}	2.4	4	5	ms	f_{CK} = 1 MHz
Clock Frequency Range	f_{CK}	0.1	1	3	MHz	
Integrating Capacitor Value	C_{INT}*	0.029			μF	V_{REF} = 2.50V, f_{CK} = 1 MHz
Address Setup Time $\overline{CS}$, A_0, A_1, to $\overline{WR}$	t_{AW}	50			ns	
Address Setup Time $\overline{CS}$, A_0, A_1, to $\overline{RD}$	t_{AR}	50			ns	
Address Hold Time $\overline{WR}$ to CS, A_0, A_1	t_{WA}	50			ns	
Address Hold Time $\overline{RD}$ to CS, A_0, A_1	t_{RA}	50			ns	
Low Level $\overline{WR}$ Pulse Width	t_{WW}	400			ns	
Low Level $\overline{RD}$ Pulse Width	t_{RR}	400			ns	
Data Setup Time Input Data to $\overline{WR}$	t_{DW}	300			ns	
Data Hold Time $\overline{WR}$ to Input Data	t_{WD}	50			ns	
Output Delay Time $\overline{RD}$ to Output Data	t_{RD}			300	ns	1TTL + 100 pF
Delay Time to High Z Output $\overline{RD}$ to Floating Output	t_{DF}			150	ns	

* C_{INT}(μF)(Min)=0.029/f_{CK}(MHz)

TIMING WAVEFORMS



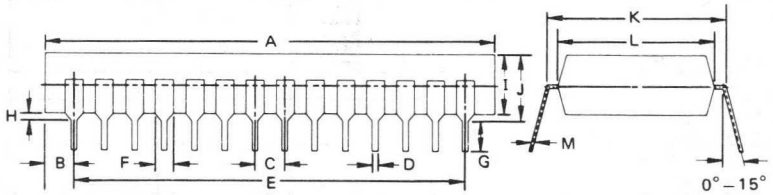
CONTROL TERMINAL FUNCTIONS

CONTROL TERMINALS					MODE	INTERNAL FUNCTION	DATA INPUT-OUTPUT TERMINALS
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0			
H	x	x	x	x	Not selected		High impedance
L	H	H	x	x	Not selected	–	
L	H	L	L	L	Write mode	Data latch A/D start	Input status, D_1, D_0 = MPX address D_3 = 8 bit/12 bit conversion designation. ① D_2 = Flag Input
L	H	L	L	H	Not selected	–	High impedance
L	H	L	H	L	Not selected	–	
L	H	L	H	H	Test mode	Test status	Input status ②
L	L	H	L	L	Read mode	Internal status	$D_7 = \overline{EOC}$, $D_6 = \overline{BUSY}$, D_5 = MSB, D_4 = 2nd MSB, D_3 = 8/12, D_2 = Flag Output D_1 = MPX, D_0 = MPX
L	L	H	L	H	Read mode	High data byte	D_7-D_0 = MSB – 8th bit
L	L	H	H	L	Read mode	Low data byte	D_7-D_4 = 9th – 12th bit, D_3-D_0 = L
L	L	H	H	H	Read mode	Low data byte	

Notes: ① Designation of number of conversion bits: 8 bit = L; 12 bit = H

② Test Mode: Used for inspecting the device. The data input-output terminals assume an input state and are connected to the A/D counter. Therefore, the A/D conversion data read out after this is meaningless.

PACKAGE OUTLINE μPD7002C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

MULTI-PROTOCOL SERIAL CONTROLLER

DESCRIPTION

The μPD7201 is a dual-channel multi-function peripheral controller designed to satisfy a wide variety of serial data communication requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller and within that role it is configurable by systems software so its "personality" can be optimized for a given serial data communications application.

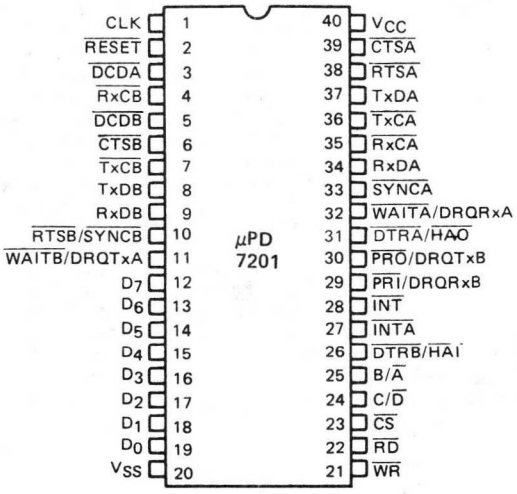
The μPD7201 is capable of handling asynchronous and synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device can also be used to support virtually any other serial protocol for applications other than data communications.

The μPD7201 can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

FEATURES

- Two Fully Independent Duplex Serial Channels
- Four Independent DMA Channels for Send/Received Data for Both Serial Inputs/Outputs
- Programmable Interrupt Vectors and Interrupt Priorities
- Modem Controls Signals
- Variable, Software Programmable Data Rate, Up to 880K Baud at 3 MHz Clock
- Double Buffered Transmitter Data and Quadruply Buffered Received Data
- Programmable CRC Algorithm
- Selection of Interrupt, DMA or Polling Mode of Operation
- Asynchronous Operation:
  - Character Length: 5, 6, 7 or 8 Bits
  - Stop Bits: 1, 1-1/2, 2
  - Transmission Speed: x1, x16, x32 or x64 Clock Frequency
  - Parity: Odd, Even, or Disable
  - Break Generation and Detection
  - Interrupt on Parity, Overrun, or Framing Errors
- Monosync, Bisync, and External Sync Operations:
  - Software Selectable Sync Characters
  - Automatic Sync Insertion
  - CRC Generation and Checking
- HDLC and SDLC Operations:
  - Abort Sequence Generation and Detection
  - Automatic Zero Insertion and Detection
  - Address Field Recognition
  - CRC Generation and Checking
  - I-Field Residue Handling
- N-Channel MOS Technology
- Single +5V Power Supply; Interface to Most Microprocessors Including 8080, 8085, 8086 and Others.
- Single Phase TTL Clock
- Available in Plastic and Ceramic Dual-in-Line Packages

PIN CONFIGURATION



9

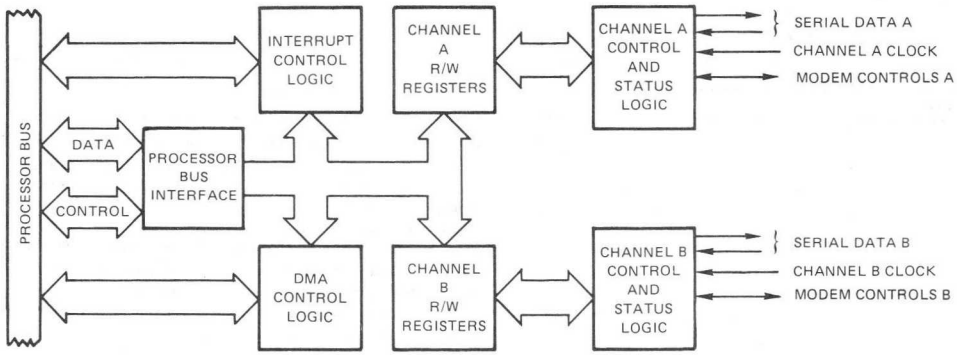
PIN DESCRIPTION

NO.	PIN SYMBOL	PIN NAME	DESCRIPTION
12-19	D_0-D_7	System Data Bus (bidirectional, 3-state)	The system data bus transfers data and commands between the processor and the μPD7201. D_0 is the least significant bit.
25	B/$\overline{A}$	Channel A or B Select (input, High selects Channel B)	This input defines which channel is accessed during a data transfer between the processor and the μPD7201.
24	C/$\overline{D}$	Control or Data Select (input, High selects Control)	This input defines the type of information transfer performed between the processor and the μPD7201. A High at this input during a processor write to or read from the μPD7201 causes the information on the data bus to be interpreted as a command for the channel selected by B/$\overline{A}$. A low at C/$\overline{D}$ means that the information on the data bus is data.
23	$\overline{CS}$	Chip Select (input, active Low)	A low level at this input enables the μPD7201 to accept command or data inputs from the processor during a write cycle, or to transmit data to the processor during a read cycle.
1	CLK	System Clock (input)	The μPD7201 uses standard TTL clock.
22	$\overline{RD}$	Read (input active Low)	If $\overline{RD}$ is active, a memory or I/O read operation is in progress. $\overline{RD}$ is used with C/$\overline{D}$, B/$\overline{A}$ and $\overline{CS}$ to transfer data from the μPD7201 to the processor or the memory.
21	$\overline{WR}$	Write (input, active Low)	The $\overline{WR}$ signal is used to control the transfer of either command or data from the processor or the memory to the μPD7201.
2	$\overline{RESET}$	Reset (input, active Low)	A low $\overline{RESET}$ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls high and disables all interrupts. The control registers must be rewritten after the μPD7201 is reset and before data is transmitted or received. $\overline{RESET}$ must be active for a minimum of one complete CLK cycle.
10,38	$\overline{RTSA}$, $\overline{RTSB}$	Request to Send (outputs, active Low)	When the $\overline{RTS}$ bit is set, the $\overline{RTS}$ output goes Low. When the $\overline{RTS}$ bit is reset in the Asynchronous mode, the output goes High after the transmitter is empty. In Synchronous modes, the $\overline{RTS}$ pin strictly follows the state of the $\overline{RTS}$ bit. Both pins can be used as general-purpose outputs.
10,33	$\overline{SYNCA}$, $\overline{SYNCB}$	Synchronization (inputs/outputs, active Low)	These pins can act either as inputs or outputs. In the Asynchronous Receive mode, they are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, the transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, $\overline{SYNC}$ must be driven Low on the second rising edge of $\overline{RxC}$ after that rising edge of $\overline{RxC}$ on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{SYNC}$ input. Once $\overline{SYNC}$ is forced Low, it is wise to keep it Low until the processor informs the external sync logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of $\overline{RxC}$ that immediately precedes the falling edge of $\overline{SYNC}$ in the External Sync mode. In the Internal Synchronization mode (Monosync and Bisync), these pins act as outputs that are active during the part of the receive clock ($\overline{RxC}$) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync pattern is recognized, regardless of character boundaries.
26,31	$\overline{DTRA}$, $\overline{DTRB}$	Data Terminal Ready (outputs, active Low)	These outputs follow the state programmed into the DTR bit. They can also be programmed as general-purpose outputs.

PIN DESCRIPTION
(CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	DESCRIPTION
27	$\overline{INTA}$	Interrupt Acknowledge (input, active Low)	This signal is generated by the processor and is sent to all peripheral devices. It serves to acknowledge the interrupt and to allow the highest priority interrupting device to put an 8-bit vector on the bus. $\overline{INT}$ and $\overline{INTA}$ are compatible with the fully nested option of the μPD8259A-5.
29	$\overline{PRI}$	Priority In (input, active Low)	These signals are daisy chained through the peripheral device controllers. The signal on these lines is intact until a device with a pending interrupt request is found on the chain. After that device, this signal holds off lower priority device interrupts. A higher priority device can interrupt the processing of an interrupt from a lower priority device, provided the processor has interrupts enabled. $\overline{PRI}$ is used with $\overline{PRO}$ to form a priority daisy chain when there is more than one interrupt-driven device. A Low on this line indicates that no other device of higher priority is being serviced by a processor interrupt service routine. $\overline{PRO}$ is Low only if $\overline{PRI}$ is Low and the processor is not servicing an interrupt from the μPD7201. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its processor interrupt service routine.
30	$\overline{PRO}$	Priority Out (output, active Low)	
11,29, 30,32	DRQTxA, DRQTxB DRQRxA, DRQRxB	DMA Request (outputs, active High)	These signals are generated by the receiver or transmitter of Channel A and Channel B. These signals can be connected to an 8257 DMA Controller and are used for handshaking during DMA transfer.
26	$\overline{HAI}$	DMA Acknowledge (input, active Low)	Typically, the HLDA signal driven from the processor is input to the $\overline{HAI}$ terminal of the highest priority μPD7201, and the $\overline{HAO}$ output of that μPD7201 is daisy chained to the $\overline{HAI}$ input of the lower priority μPD7201 and propagated downstream. $\overline{HAI}$ and $\overline{HAO}$ signals provide acknowledgement for the highest priority outstanding DMA request.
31	$\overline{HAO}$	DMA Acknowledge (output, active Low)	
28	$\overline{INT}$	Interrupt Request (output, open collector, active Low)	When the μPD7201 is requesting an interrupt, it pulls $\overline{INT}$ low.
11,32	$\overline{WAITA}$, $\overline{WAITB}$	(Outputs, open drain)	Wait lines for both channels that synchronize the processor to the μPD7201 data rate. The reset state is open drain.
6,39	$\overline{CTSA}$, $\overline{CTSB}$	Clear to Send (inputs, active Low)	When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime inputs. The μPD7201 detects pulses on these inputs and interrupts the processor on both logic level transitions. The Schmitt-trigger inputs do not guarantee a specified noise-level margin.
3,5	$\overline{DCDA}$, $\overline{DCDB}$	Data Carrier Detect (inputs, active Low)	These signals are similar to the $\overline{CTS}$ inputs, except they can be used as receiver enables.
9,34	RxDA, RxDB	Receive Data (inputs, active High)	
8,37	TxDA, TxDB	Transmit Data (outputs, active High)	
4,35	$\overline{RxCA}$, $\overline{RxCB}$	Receiver Clocks (inputs)	The Receiver Clocks may be 1, 16, 32, or 64 times the data rate in asynchronous modes. Receive data is sampled on the rising edge of $\overline{RxC}$.
7,36	$\overline{TxCA}$, $\overline{TxCB}$	Transmitter Clocks (inputs)	In asynchronous modes, the Transmitter Clocks may be 1, 16, 32, or 64 times the data rate. The multiplier for the transmitter and the receiver must be the same. Both $\overline{TxC}$ and $\overline{RxC}$ inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise margin is specified). TxD changes on the falling edge of $\overline{TxC}$. Note that $\overline{TxC}$ and $\overline{RxC}$ in Channel B are on a common pin, $\overline{RxCB}/\overline{TxCB}$.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature . . . . . 0° to +70°C
Storage Temperature . . . . . -65° to +125°C
Voltage on Any Pin . . . . . -0.5 to +7 Volts ①

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±10%

PARAMETER	SYMBOL	LIMITS		UNIT	TEST CONDITIONS
		MIN	MAX		
Input Low Voltage	V_{IL}	-0.5	+0.8	V	
Input High Voltage	V_{IH}	+2.0	V_{CC}+0.5	V	
Output Low Voltage	V_{OL}		+0.45	V	I_{OL} = +2.0 mA
Output High Voltage	V_{OH}	+2.4		V	I_{OH} = -200 μA
Input Leakage Current	I_{IL}		±10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{OL}		±10	μA	V_{OUT} = V_{CC} to 0V
V_{CC} Supply Current	I_{CC}		180	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

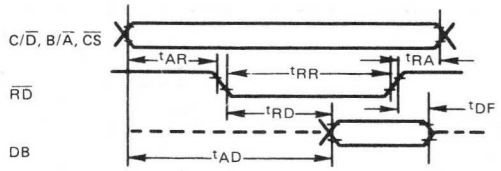
PARAMETER	SYMBOL	LIMITS		UNIT	TEST CONDITIONS
		MIN	MAX		
Input Capacitance	C_{IN}		10	pF	fc = 1 MHz
Output Capacitance	C_{OUT}		15	pF	Unmeasured pins Returned to GND
Input/Output Capacitance	$C_{I/O}$		20	pF	

AC CHARACTERISTICS T_a = 0°C to +70°C; V_{CC} = +5V ±10%

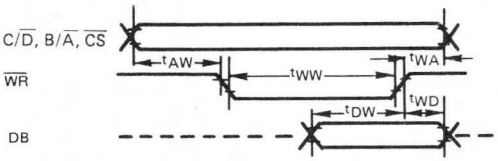
PARAMETER	SYMBOL	LIMITS		UNIT
		MIN	MAX	
Clock Cycle	t_{CY}	250	4000	ns
Clock High Width	t_{CH}	105	2000	ns
Clock Low Width	t_{CL}	105	2000	ns
Clock Rise and Fall Time	t_r, t_f	0	30	ns
Address Setup to $\overline{RD}$	t_{AR}	0		ns
Address Hold from $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ Pulse Width	t_{RR}	250		ns
Data Delay from Address	t_{AD}		200	ns
Data Delay from $\overline{RD}$	t_{RD}		200	ns
Output Float Delay	t_{DF}	10	100	ns
Address Setup to $\overline{WR}$	t_{AW}	0		ns
Address Hold from $\overline{WR}$	t_{WA}	0		ns
$\overline{WR}$ Pulse Width	t_{WW}	250		ns
Data Setup to $\overline{WR}$	t_{DW}		150	ns
Data Hold from $\overline{WR}$	t_{WD}	0		ns
$\overline{PRO}$ Delay from $\overline{INTA}$	t_{IAPO}		200	ns
$\overline{PRI}$ Setup to $\overline{INTA}$	t_{PIN}	0		ns
$\overline{PRI}$ Hold from $\overline{INTA}$	t_{IP}	0		ns
$\overline{INTA}$ Pulse Width	t_{II}	250		ns
$\overline{PRO}$ Delay from $\overline{PRI}$	t_{PIPO}		100	ns
Data Delay from $\overline{INTA}$	t_{ID}		200	ns
Request Hold from $\overline{RD}/\overline{WR}$	t_{CO}		150	ns
$\overline{HAI}$ Setup to $\overline{RD}/\overline{WR}$	t_{LR}	300		ns
$\overline{HAI}$ Hold from $\overline{RD}/\overline{WR}$	t_{RL}	0		ns
$\overline{HAO}$ Delay from $\overline{HAI}$	t_{HIHO}		100	ns
Recovery Time Between Controls	t_{RV}	300		ns
$\overline{WAIT}$ Delay from Address	t_{CW}		120	ns
Data Clock Cycle	t_{DCY}	400		ns
Data Clock Low Width	t_{DCL}	180		ns
Data Clock High Width	t_{DCH}	180		ns
Tx Data Delay	t_{TD}		300	ns
Data Set up to $\overline{RxC}$	t_{DS}	0		ns
Data Hold from $\overline{RxC}$	t_{DH}	140		ns
$\overline{INT}$ Delay Time from $\overline{TxC}$	t_{ITD}		4 ~ 6	t_{CY}
$\overline{INT}$ Delay Time from $\overline{RxC}$	t_{IRD}		7 ~ 11	t_{CY}
Low Pulse Width	t_{PL}	200		ns
High Pulse Width	t_{PH}	200		ns
External $\overline{INT}$ from $\overline{CST}$, $\overline{DCD}$, $\overline{SYNC}$	t_{IPD}		500	ns
Delay from $\overline{RxC}$ to $\overline{SYNC}$	t_{DRxC}		100	ns

TIMING WAVEFORMS

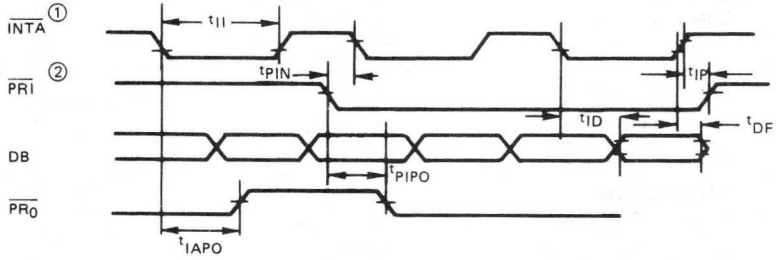
READ CYCLE



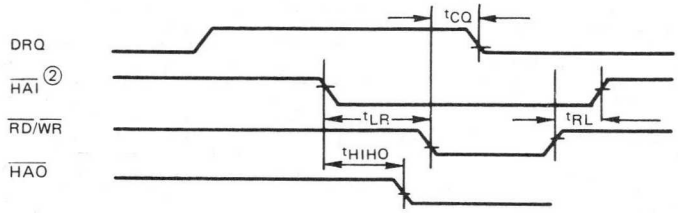
WRITE CYCLE



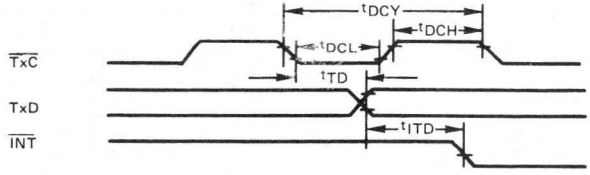
INTA CYCLE



DMA CYCLE



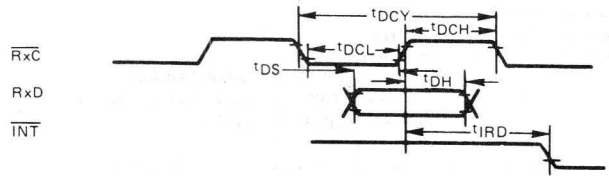
TRANSMIT DATA CYCLE



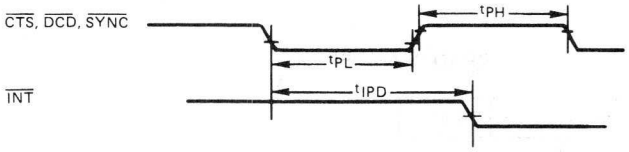
Notes: ① INTA signal acts as RD signal.
② PRI and HAI signals act as CS signal.

TIMING WAVEFORMS (CONT.)

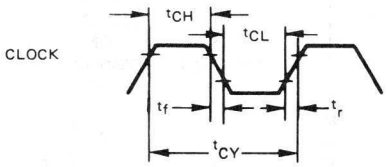
RECEIVE DATA CYCLE



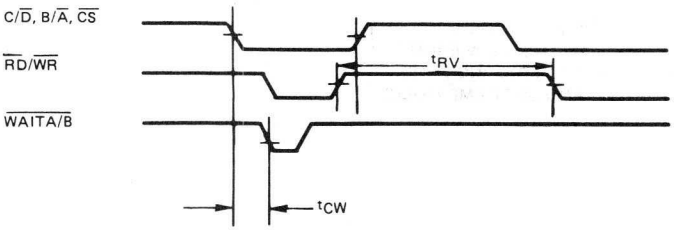
OTHER TIMING



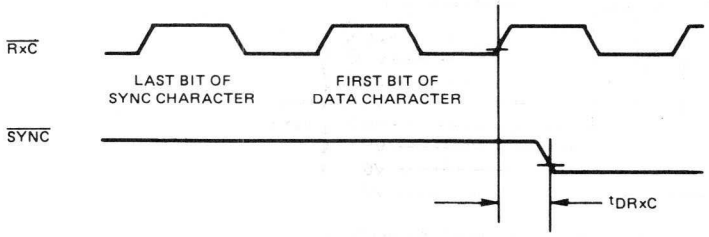
CLOCK



READ/WRITE CYCLE (SOFTWARE BLOCK TRANSFER MODE)



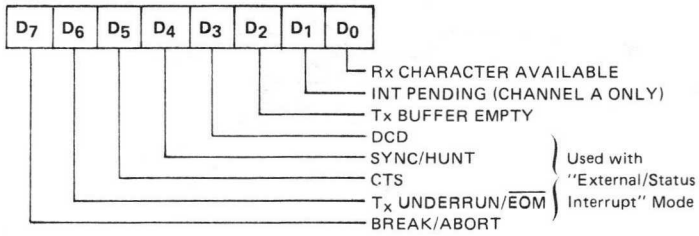
SYNC PULSE GENERATION (EXTERNAL SYNC MODE)



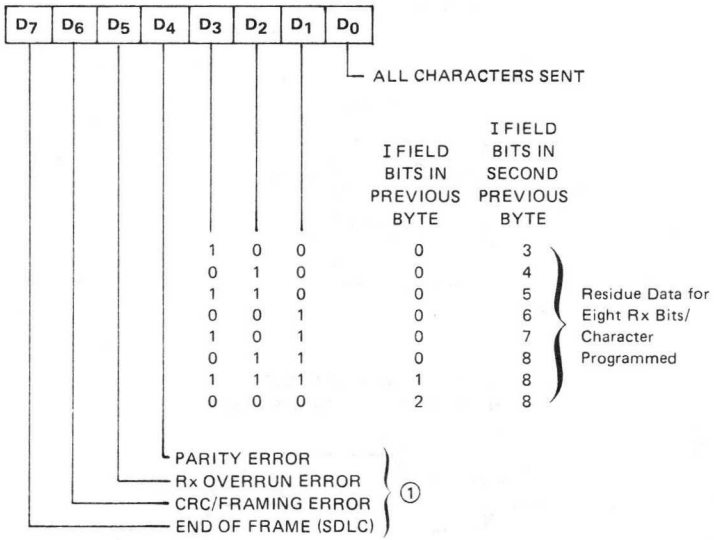
9

READ REGISTER BIT FUNCTIONS

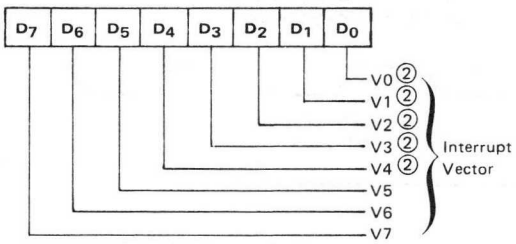
READ REGISTER 0



READ REGISTER 1 ①



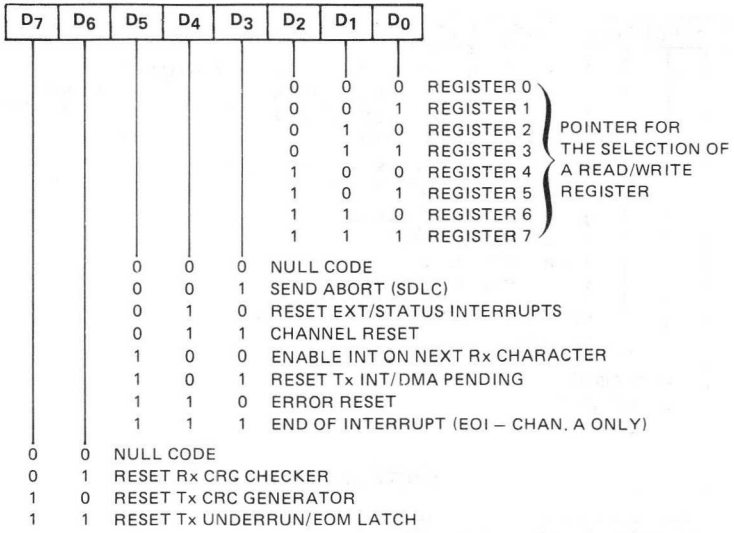
READ REGISTER 2



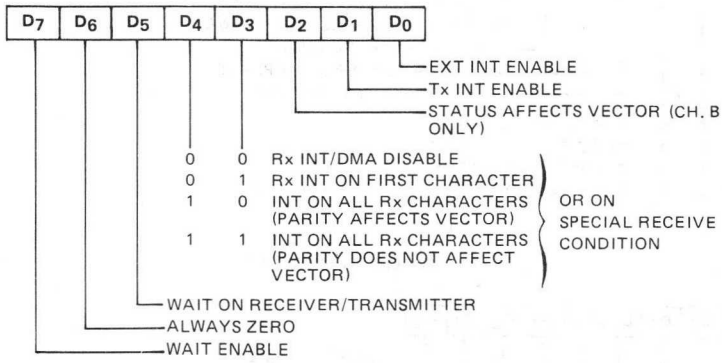
Notes: ① Used with Special Receive Condition Mode.
② Variable if "Status Affects Vector" is programmed.

WRITE REGISTER BIT FUNCTIONS

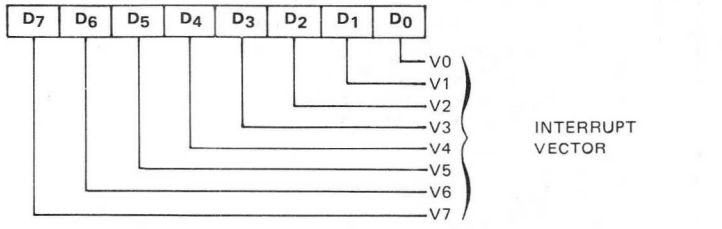
WRITE REGISTER 0



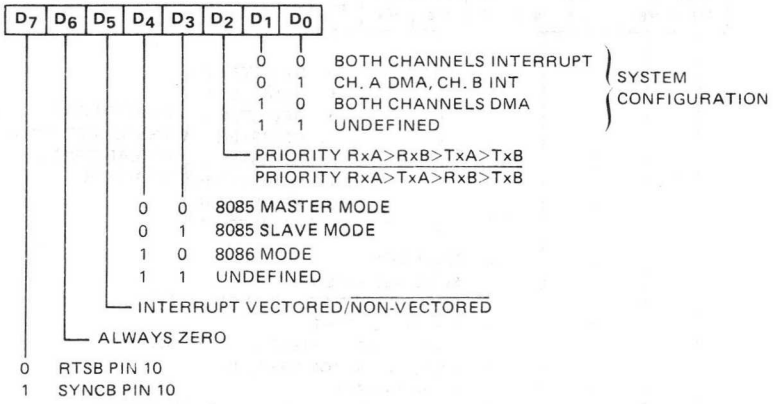
WRITE REGISTER 1



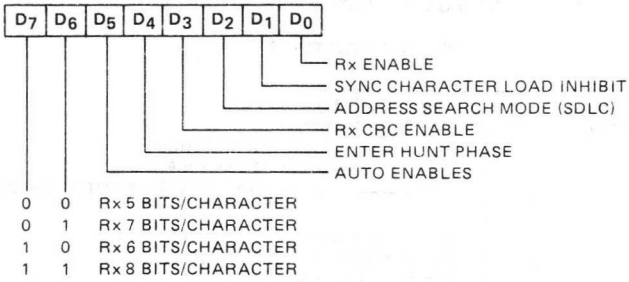
WRITE REGISTER 2 (CHANNEL B)



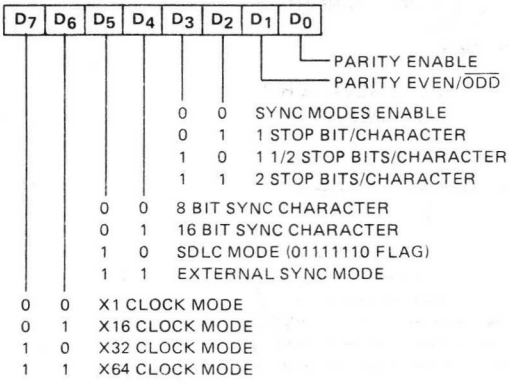
WRITE REGISTER 2
(CHANNEL A)



WRITE REGISTER 3

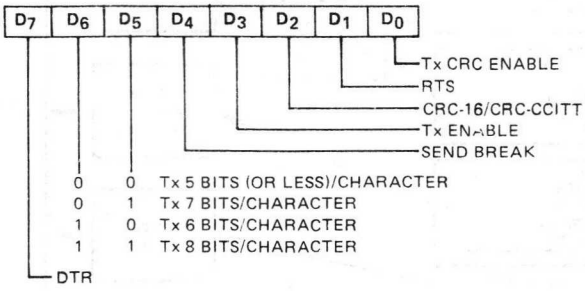


WRITE REGISTER 4

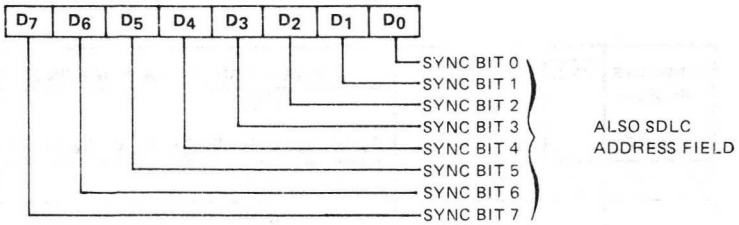


WRITE REGISTER BIT FUNCTIONS (CONT.)

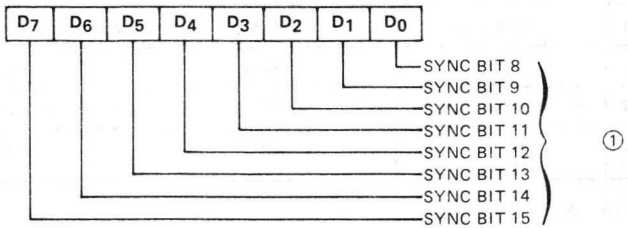
WRITE REGISTER 5



WRITE REGISTER 6



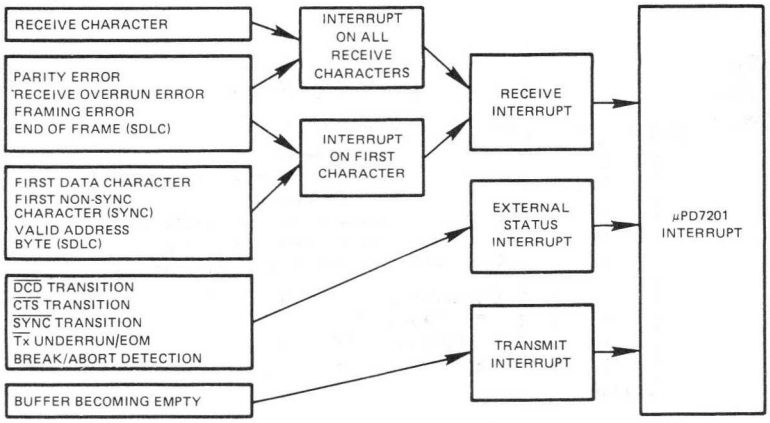
WRITE REGISTER 7



Note: ① For SDLC it must be programmed to "01111110" for flag recognition.

9

INTERRUPT STRUCTURE



WR2s BITS IN CH. A			PRIN	MODE	CONTENTS ON DATA BUS DRIVEN BY THE μPD7201 AT EACH INTA SEQUENCE																			
					1st $\overline{INTA}$								2nd $\overline{INTA}$								3rd $\overline{INTA}$ (*)							
D_5	D_4	D_3			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Ø	x	x	x	Non-vectored	High-Z								High-Z								High-Z							
1	Ø	Ø	Ø	8085 Master	(Call) 1	1	Ø	Ø	1	1	Ø	1	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
1	Ø	Ø	1	8085 Master	1	1	Ø	Ø	1	1	Ø	1	High-Z								High-Z							
1	Ø	1	Ø	8085 Slave	High-Z								V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
1	Ø	1	1	8085 Slave	High-Z								High-Z								High-Z							
1	1	Ø	Ø	8086	High-Z								V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0								
1	1	Ø	1	8086	High-Z								High-Z															

(*) 3rd $\overline{INTA}$ is 8085 Mode

INTELLIGENT GPIB INTERFACE CONTROLLER

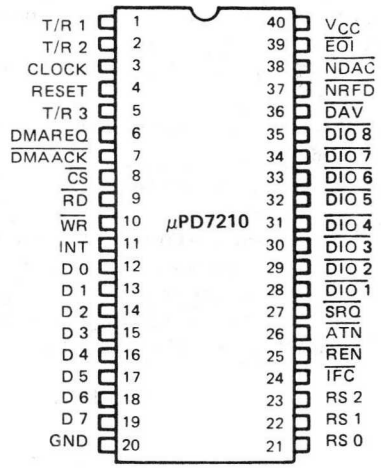
DESCRIPTION

The μPD7210 TLC is an intelligent GPIB Interface Controller designed to meet all of the functional requirements for Talkers, Listeners, and Controllers as specified by the IEEE Standard 488-1978. Connected between a processor bus and the GPIB, the TLC provides high level management of the GPIB to unburden the processor and to simplify both hardware and software design. Fully compatible with most processor architectures, Bus Driver/Receivers are the only additional components required to implement any type of GPIB interface.

FEATURES

- All Functional Interface Capability Meeting IEEE Standard
  - SH1 (Source Handshake)
  - AH1 (Acceptor Handshake)
  - T5 or TE5 (Talker or Extended Talker)
  - L3 or LE3 (Listener or Extended Listener)
  - SR1 (Service Request)
  - RL1 (Remote Local)
  - PP1 or PP2 (Parallel Port (Remote or Local Configuration))
  - DC1 (Device Clear)
  - DT1 (Device Trigger)
  - C1-5 (Controller (All Functions))
- Programmable Data Transfer Rate
- 16 MPU Accessible Registers – 8 Read/8 Write
- 2 Address Registers
  - Detection of MTA, MLA, MSA (My Talk/Listen/Secondary Address)
  - 2 Device Addresses
- EOS Message Automatic Detection
- Command (IEEE Standard 488-78) Automatic Processing and Undefined Command Read Capability
- DMA Capability
- Programmable Bus Transceiver I/O Specification (Works with T.I./Motorola/Intel)
- 1 to 8 MHz Clock Range
- TTL Compatible
- N Channel MOS
- +5V Single Power Supply
- 40-Pin Plastic DIP
- 8080/85/86 Compatible

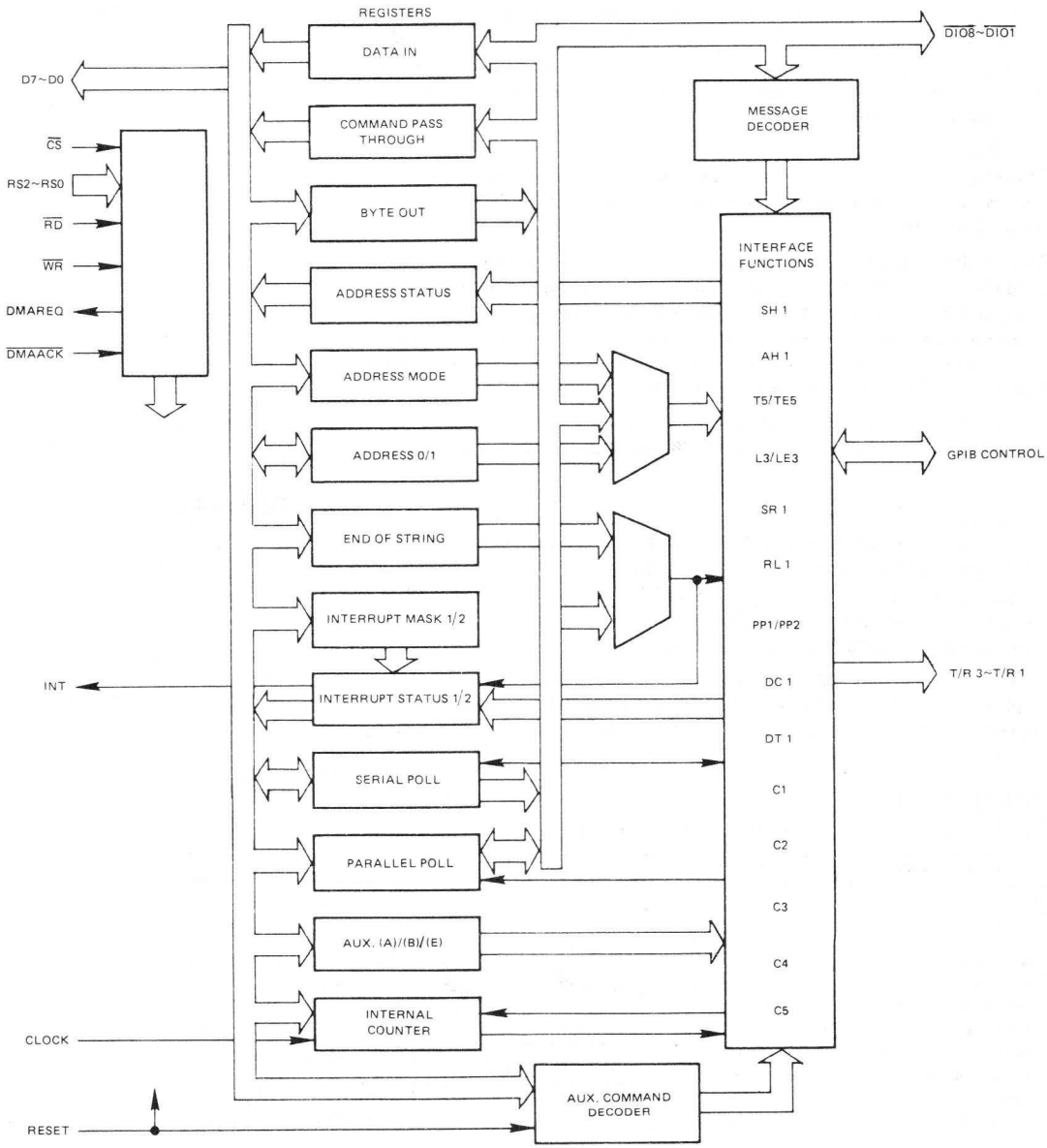
PIN CONFIGURATION



PIN IDENTIFICATION

PIN	NAME	I/O	DESCRIPTION
1	T/R1	O	Transmit/Receive Control – Input/Output Control Signal for the GPIB Bus Transceivers.
2	T/R2	O	Transmit/Receive Control – The function of T/R2, T/R3 are determined by the value of TRM1, TRM0 of the address mode register.
3	CLK	I	Clock – (1-8 MHz) Reference Clock for generating the state change prohibit times T1, T6, T7, T9 specified in IEEE Standard 488-1978.
4	RST	I	Reset – Resets 7210 to an idle state when high (active high).
5	T/R3	O	Transmit/Receive Control – Function determined by TRM1 and TRM0 of address mode register (See T/R2).
6	DRQ	O	DMA Request – 7210 requests data transfer to the computer system, becomes low on input of DMA acknowledge signal $\overline{\text{DACK}}$.
7	$\overline{\text{DACK}}$	I	DMA Acknowledge – (Active Low) Signal connects the computer system data bus to the data register of the 7210.
8	$\overline{\text{CS}}$	I	Chip Select – (Active Low) Enables access to the register selected by RS0-2 (read or write operation).
9	$\overline{\text{RD}}$	I	Read – (Active Low) Places contents of read register specified by RS0-2 – on D0-7 (Computer Bus).
10	$\overline{\text{WR}}$	I	Write – (Active Low) writes data on D0-7 into the write register specified by RS0-2.
11	INT / $\overline{\text{INT}}$	O	Interrupt Request – (Active High/Low) Becomes active due to any 1 of 13 internal interrupt factors (unmasked) active state software configurable, active high on chip reset.
12-19	D0-7	I/O	Data Bus – 8 bit bidirectional data bus, for interface to computer system.
20	GND		Ground.
21-23	RS0-2	I	Register Select – These lines select one of eight read (write) registers during a read (write) operation.
24	$\overline{\text{IFC}}$	I/O	Interface Clear – Control line used for clearing the interface functions.
25	$\overline{\text{REN}}$	I/O	Remote Enable – Control line used to select remote or local control of the devices.
26	$\overline{\text{ATN}}$	I/O	Attention – Control line which indicates whether data on DIO lines is an interface message or device dependent message.
27	$\overline{\text{SRQ}}$	I/O	Service Request – Control line used to request the controller for service.
28-35	$\overline{\text{DIO1-8}}$	I/O	Data Input/Output – 8 bit bidirectional bus for transfer of message on the GPIB.
36	$\overline{\text{DAV}}$	I/O	Data Valid – Handshake line indicating that data on DIO lines is valid.
37	$\overline{\text{NRFD}}$	I/O	Ready for Data – Handshake line indicating that device is ready for data.
38	$\overline{\text{NDAC}}$	I/O	Data Accepted – Handshake line indicating completion of message reception.
39	$\overline{\text{EOI}}$	I/O	End or Identify – Control line used to indicate the end of multiple byte transfer sequence or to execute a parallel polling in conjunction with ATN.
40	V_{CC}		+5V DC – Technical Specifications: +5V; NMOS; 500 MW; 40 Pins; TTL Compatible; 1-8 MHz.

BLOCK DIAGRAM



μPD7210

INTRODUCTION

The IEEE Standard 488 describes a "Standard Digital Interface for Programmable Instrumentation" which, since its introduction in 1975, has become the most popular means of interconnecting instruments and controllers in laboratory, automatic test and even industrial applications. Refined over several years, the 488-1978 standard, also known as the General Purpose Interface Bus (GPIB), is a highly sophisticated standard providing a high degree of flexibility to meet virtually most all instrumentation requirements. The μPD7210 TLC implements all of the functions that are required to interface to the GPIB. While it is beyond the scope of this document to provide a complete explanation of the IEEE 488 Standard, a basic description follows:

The GPIB interconnects up to 15 devices over a common set of data control lines. Three types of devices are defined by the standard: Talkers, Listeners, and Controllers, although some devices may combine functions such as Talker/Listener or Talker/Controller.

Data on the GPIB is transferred in a bit parallel, byte serial fashion over 8 Data I/O lines (D101 – D108). A 3 wire handshake is used to ensure synchronization of transmission and reception. In order to permit more than one device to receive data at the same time, these control lines are "Open Collector" so that the slowest device controls the data rate. A number of other control lines perform a variety of functions such as device addressing, interrupt generation, etc.

The μPD7210 TLC implements all functional aspects of Talker, Listener and Controller functions as defined by the 488-1978 Standard, and on a single chip.

GENERAL

The μPD7210 TLC is an intelligent controller designed to provide high level protocol management of the GPIB, freeing the host processor for other tasks. Control of the TLC is accomplished via 16 internal registers. Data may be transferred either under program control or via DMA using the TLC's DMA control facilities to further reduce processor overhead. The processor interface of the TLC is general in nature and may be readily interfaced to most processor lines.

In addition to providing all control and data lines necessary for a complete GPIB implementation, the TLC also provides a unique set of bus transceiver controls permitting the use of a variety of different transceiver configurations for maximum flexibility.

INTERNAL REGISTERS

The TLC has 16 registers, eight of which are read and 8 write.

REGISTER NAME	ADDRESSING					SPECIFICATION							
	R	R	R	WR	CS								
	S	S	S	WR	CS								
	2	1	0	WR	CS								
Data In [0R]	0	0	0	WR	CS	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Interrupt Status 1 [1R]	0	0	1	WR	CS	CPT	APT	DET	END	DEC	ERR	DO	DI
Interrupt Status 2 [2R]	0	1	0	WR	CS	INT	SRQ1	LOK	REM	CO	LOKC	REMC	ADSC
Serial Poll Status [3R]	0	1	1	WR	CS	S8	PEND	S6	S5	S4	S3	S2	S1
Address Status [4R]	1	0	0	WR	CS	CIC	$\overline{ATN}$	SPMS	LPAS	TPAS	LA	TA	MJMN
Command Pass Through [5R]	1	0	1	WR	CS	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0
Address 0 [6R]	1	1	0	WR	CS	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
Address 1 [7R]	1	1	1	WR	CS	EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
Byte Out [0W]	0	0	0	WR	CS	BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0
Interrupt Mask 1 [1W]	0	0	1	WR	CS	CPT	APT	DET	END	DEC	ERR	DO	DI
Interrupt Mask 2 [2W]	0	1	0	WR	CS	0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC
Serial Poll Mode [3W]	0	1	1	WR	CS	S8	rsv	S6	S5	S4	S3	S2	S1
Address Mode [4W]	1	0	0	WR	CS	ton	lon	TRM1	TRM0	0	0	ADM1	ADM0
Auxiliary Mode [5W]	1	0	1	WR	CS	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0
Address 0/1 [6W]	1	1	0	WR	CS	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1
End of String [7W]	1	1	1	WR	CS	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

DATA REGISTERS

The data registers are used for data and command transfers between the GPIB and the microcomputer system.

DATA IN (0R)

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

Holds data sent from the GPIB to the computer

BYTE OUT (0W)

BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0

Holds information written into it for transfer to the GPIB

INTERRUPT REGISTERS

The interrupt registers are composed of interrupt status bits, interrupt mask bits, and some other noninterrupt related status bits.

READ

INTERRUPT STATUS 1 [1R]	CPT	APT	DET	END	DEC	ERR	DO	DI
INTERRUPT STATUS 2 [2R]	INT	SRQ1	LOK	REM	CO	LOKC	REMC	ADSC

WRITE

INTERRUPT MASK 1 [1W]	CPT	APT	DET	END	DEC	ERR	DO	DI
INTERRUPT MASK 2 [2W]	0	SRQ1	DMAO	DMAI	CO	LOKC	REMC	ADSC

There are thirteen factors which can generate an interrupt from the μPD7210, each with their own status bit and mask bit.

The interrupt status bits are always set to one if the interrupt condition is met. The interrupt mask bits decide whether the INT bit and the interrupt pin will be active for that condition.

Interrupt Status Bits

INT	OR of All Unmasked Interrupt Status Bits
CPT	Command Pass Through
APT	Address Pass Through
DET	Device Trigger
END	End (END or EOS Message Received)
DEC	Device Clear
ERR	Error
DO	Data Out
DI	Data In
SRQI	Service Request Input
LOKC	Lockout Change
REMC	Remote Change
ADSC	Address Status Change
CO	Command Output

Non Interrupt Status Bits

LOK	Lockout
REM	Remote/Local
DMAO	Enable/Disable DMA Out
DMAI	Enable/Disable DMA In

SERIAL POLL REGISTERS

READ

	S8	PEND	S6	S5	S4	S3	S2	S1
SERIAL POLL STATUS [3R]								

WRITE

	S8	rsv	S6	S5	S4	S3	S2	S1
SERIAL POLL MODE [3W]								

The Serial Poll Mode register holds the STB (status byte: S8, S6-S1) sent over the GPIB and the local message rsv (request service). The Serial Poll Mode register may be read through the Serial Poll Status register. The PEND is set by rsv = 1, and cleared by NPRS • $\overline{\text{rsv}}$ = 1 (NPRS = Negative Poll Response State).

ADDRESS MODE/STATUS REGISTERS

	CIC	$\overline{\text{ATN}}$	SPMS	LPAS	TPAS	LA	TA	MJMN
ADDRESS STATUS [4R]								
ADDRESS MODE [4W]	ton	lon	TRM1	TRM0	0	0	ADM1	ADM0

The Address Mode register selects the address mode of the device and also sets the mode for T/R3 and T/R2 the transceiver control lines.

The TLC is able to automatically detect two types of addresses which are held in address registers 0 and 1. The addressing modes are outlined below.

ADDRESS MODES

ton	lon	ADM1	ADM0	ADDRESS MODE	CONTENTS OF ADDRESS (0) REGISTER	CONTENTS OF ADDRESS (1) REGISTER
1	0	0	0	Talk only mode	Address Identification Not Necessary	
0	1	0	0	Listen only mode	Not Used	
0	0	0	1	Address mode 1	Major talk address or Major listen address	Minor talk address or Minor listen address
0	0	1	0	Address mode 2	Primary address (talk or listen)	Secondary address (talk or listen)
0	0	1	1	Address mode 3	Primary address (major talk or major listen)	Primary address (minor talk or minor listen)
Combinations other than above indicated Prohibited.						

Notes: A1 — Either MTA or MLA reception is indicated by coincidence of either address with the received address. Interface function T or L.

A2 — Address register 0 = primary, Address register 1 = secondary, interface function TC or LC.

A3 — CPU must read secondary address via Command Pass Through Register. TE or LC Command.

ADDRESS STATUS BITS

$\overline{ATN}$	Data Transfer Cycle (device in CSBS)
LPAS	Listener Primary Addressed State
TPAS	Talker Primary Addressed State
CIC	Controller Active
LA	Listener Addressed
TA	Talker Addressed
MJMN	Sets minor T/L address Reset = Major T/L address
SPMS	Serial Poll Mode State

ADDRESS REGISTERS

ADDRESS 0 [6R]	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
ADDRESS 1 [7R]	EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
ADDRESS 0/1 [6W]	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1

Address settings are made by writing into the address 0/1 register. The function of each bit is described below.

ADDRESS 0/1 REGISTER BIT SELECTIONS

ARS – Selects which address register 0 or 1
DT – Permits or Prohibits address to be detected as Talk
DL – Permits or Prohibits address to be detected as Listen
AD5 – AD1 – Device address value
EOI – Holds the value of EOI line when data is received

COMMAND PASS THROUGH REGISTER

COMMAND PASS THROUGH [5R]	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0

The CPT register is used such that the CPU may read the DIO lines in the cases of undefined command, secondary address, or parallel poll response.

END OF STRING REGISTER

END OF STRING [7W]	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

This register holds either a 7 or 8 bit EOS message byte used in the GPIB system to detect the end of a data block. Aux Mode Register A controls the specific use of this register.

AUXILIARY MODE REGISTER

AUXILIARY MODE [5W]	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0

This is a multipurpose register. A write to this register generates one of the following operations according to the values of the CNT bits.

CNT 2	1	0	COM 4	3	2	1	0	OPERATION
0	0	0	C_4	C_3	C_2	C_1	C_0	Issues an auxiliary command specified by C_4 to C_0.
0	0	1	0	F_3	F_2	F_1	F_0	The reference clock frequency is specified and T_1, T_6, T_7, T_9 are determined as a result.
0	1	1	U	S	P_3	P_2	P_1	Makes write operation to the parallel poll register.
1	0	0	A_4	A_3	A_2	A_1	A_0	Makes write operation to the aux. (A) register.
1	0	1	B_4	B_3	B_2	B_1	B_0	Makes write operation to the aux. (B) register.
1	1	0	0	0	0	E_1	E_0	Makes write operation to the aux. (E) register.

AUXILIARY COMMANDS 0 0 0 C_4 C_3 C_2 C_1 C_0

COM 43210			
00000	iepon	–	Immediate Execute pon – Generate local pon Message
00010	crst	–	Chip Reset – Same as External Reset
00011	rrfd	–	Release RFD
00100	trig	–	Trigger
00101	rtl	–	Return to Local Message Generation
00110	seoi	–	Send EOI Message
00111	nvld	–	Non Valid (OSA reception) – Release DAC Holdoff
01111	vld	–	Valid (MSA reception, CPT, DEC, DET) – Release DAC Holdoff
0X001	sppf	–	Set/Reset Parallel Poll Flag
10000	gts	–	Go To Standby
10001	tca	–	Take Control Asynchronously
10010	tcs	–	Take Control Synchronously
11010	tcse	–	Take Control Synchronously on End
10011	ltn	–	Listen
11011	ltnc	–	Listen with Continuous Mode
11100	lun	–	Local Unlisten
11101	epp	–	Execute Parallel Poll
1X110	sifc	–	Set/Reset IFC
1X111	sren	–	Set/Reset REN
10100	dsc	–	Disable System Control

INTERNAL COUNTER 0 0 1 0 F_3 F_2 F_1 F_0

The internal counter generates the state change prohibit times (T_1, T_6, T_7, T_9) specified in the IEEE std 488-1978 with reference to the clock frequency.

AUXILIARY A REGISTER 1 0 0 A_4 A_3 A_2 A_1 A_0

Of the 5 bits that may be specified as part of its access word, two bits control the GPIB data receiving modes of the 7210 and 3 bits control how the EOS message is used.

A_1	A_0	DATA RECEIVING MODE
0	0	Normal Handshake Mode
0	1	RFD Holdoff on all Data Mode
1	0	RFD Holdoff on End Mode
1	1	Continuous Mode

BIT NAME			FUNCTION
A_2	0	Prohibit	Permits (prohibits) the setting of the END bit by reception of the EOS message.
	1	Permit	
A_3	0	Prohibit	Permits (prohibits) automatic transmission of END message simultaneously with the transmission of EOS message TACS.
	1	Permit	
A_4	0	7 bit EOS	Makes the 8 bits/7 bits of EOS register the valid EOS message.
	1	8 bit EOS	

AUXILIARY B REGISTER 1 0 1 B_4 B_3 B_2 B_1 B_0

The Auxiliary B Register is much like the A Register in that it controls the special operating features of the device.

BIT NAME			FUNCTION
B_0	1	Permit	Permits (prohibits) the detection of undefined command. In other words, it permits (prohibits) the setting of the CPT bit on reception of an undefined command.
	0	Prohibit	
B_1	1	Permit	Permits (prohibits) the transmission of the END message when in serial poll active state (SPAS).
	0	Prohibit	
B_2	1	T_1 (high-speed)	T_1 (high speed) as T_1 of handshake after transmission of 2nd byte following data transmission.
	0	T_1 (low-speed)	
B_3	1	INT	Specifies the active level of INT pin.
	0	INT	
B_4	1	1st = SRQS	SRQS indicates the value of 1st level local message (the value of the parallel poll flag is ignored). SRQS = 1 . . . 1st = 1. SRQS = 0 . . . 1st = 0.
	0	1st = Parallel Poll Flag	The value of the parallel poll flag is taken as the 1st local message.

9

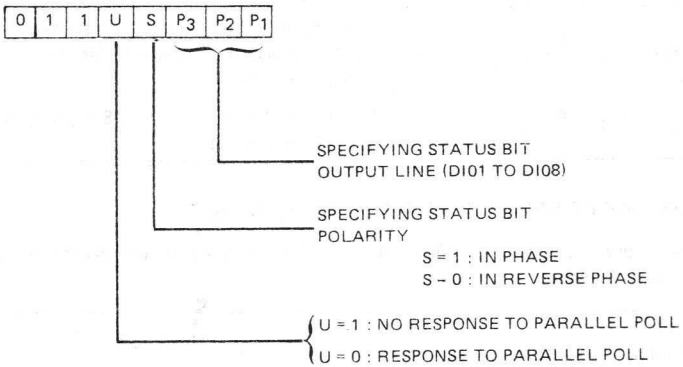
AUXILIARY E REGISTER 1 1 0 0 0 0 E_1 E_0

This register controls the Data Acceptance Modes of the TLC.

BIT	FUNCTION		
E_0	1	Enable	DAC Holdoff by initiation of DCAS
	0	Disable	
E_1	1	Enable	DAC Holdoff by initiation of DTAS
	0	Disable	

Parallel Poll Register 0 1 1 U S P_3 P_2 P_1

The Parallel Poll Register defines the parallel poll response of the μPD7210.



PROGRAMMABLE LCD CONTROLLER/DRIVER

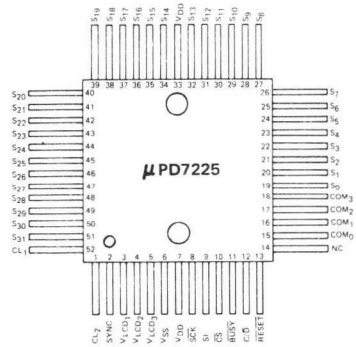
DESCRIPTION

The μPD7225 is a programmable peripheral device containing all the circuitry necessary for interfacing a microprocessor to a wide variety of alpha-numeric Liquid Crystal Displays (LCDs). The display controller hardware automatically synchronizes the drive signals for any static or multiplexed LCD containing up to 4 backplanes, and up to 32 segments . The μPD7225 is fully compatible with most microprocessors, and communicates with them through a 2-line, 8-bit Serial port. It can be easily configured into multiple chip designs for larger LCD applications. In addition, the μPD7225 includes on board 8-segment Numeric and 15-segment Alpha-Numeric decoders, and programmable blinking capabilities. The μPD7225 is manufactured with a low-power single 5V CMOS process, and is available in a 52-pin plastic flat package.

FEATURES

- Single Chip LCD Controller
- Direct LCD Drive
- Selectable Backplace Drive Configuration
  - Static; 2-, 3-, or 4-Backplane Multiplexed
- Programmable Display Configurations
  - 8-Segment Numeric – up to 16 Characters
  - 15-Segment Alpha-Numeric – up to 8 Characters
- 32-Segment Drive Lines
- Selectable Display Bias Configuration
  - Static; 1/2 or 1/3
- Automatic Synchronization of Segment and Backplane Drive Lines
- Dual 32 x 4 Bit RAMs for Display Data Storage
- Programmable Display Data Addressing
  - Individual Segment
  - 16-Character, 8-Segment Numeric Decoder
  - 64-Character, 15-Segment Alpha-Numeric Decoder
- Programmable Blinking Capability
  - Individual Segment, Individual Character, or Entire Display
- 8-Bit Serial Interface
- Compatible with most 4-Bit, 8-Bit, and 16-Bit Microprocessors
- Fully Cascadable for Larger LCD Applications
- Single +5V Power Supply
- CMOS Technology
- 52-Pin Plastic Flat Package

PIN CONFIGURATION

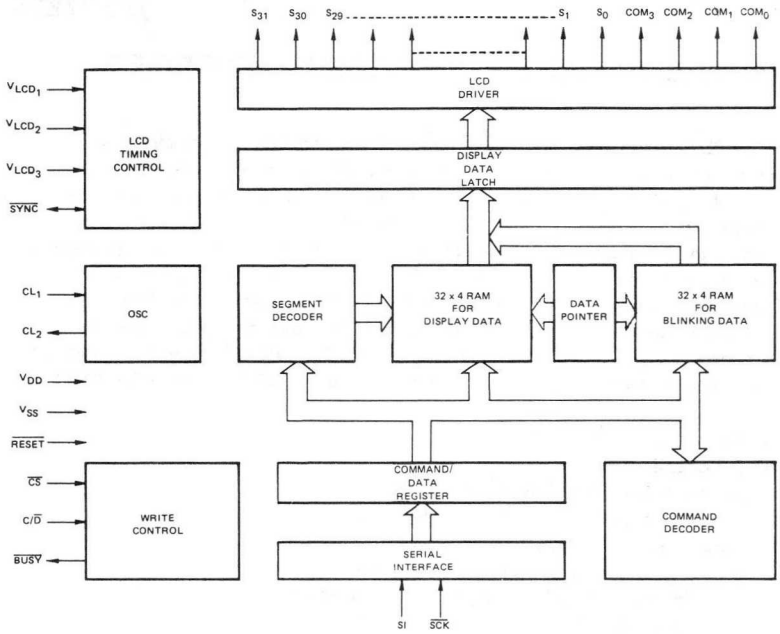


PIN DESCRIPTION

SYMBOL	DESCRIPTION
S_0-S_{31}	LCD Segment Drive Outputs
COM_0-COM_3	LCD Backplane Drive Outputs
V_{SS}	Ground
V_{DD}	Power Supply Positive
V_{LCD_1}-V_{LCD_3}	LCD Power Supply
$\overline{SCK}$	Serial Clock Input
SI	Serial Input
$\overline{CS}$	Chip Select
$C/\overline{D}$	Command/Data Select
CL_1, CL_2	System Clock Input, Output
$\overline{SYNC}$	Synchronization Signal I/O Port for multiple chip
$\overline{BUSY}$	Busy Output
$\overline{RESET}$	Reset Input
NC	No Connection

9

BLOCK DIAGRAM



COMMAND DESCRIPTION

1. MODE SET

0	1	0	D_4	D_3	D_2	D_1	D_0	40-5F

The MODE SET command sets up the Backplane Drive Configuration, the Display Bias Voltage Configuration, and the A/C Drive Frequency for the μPD7225.

The Backplane Drive Configuration is defined as follows:

D_3	D_2	Backplane Drive Configuration
0	1	Static (1-Backplane)
1	1	2-Backplane Multiplexed
1	0	3-Backplane Multiplexed
0	0	4-Backplane Multiplexed

The Display Bias Voltage Configuration is defined as follows:

D_4	Display Bias Voltage Configuration
0	1/3 (three voltage)
1	1/2 (two voltage)
X	Static (single voltage; default when $D_3D_2 = 00$)

The A/C Drive Frequency is defined as follows:

D_1	D_0	A/C Drive Frequency
0	0	$f_c/2^7$ Hz
0	1	$f_c/2^8$ Hz
1	0	$f_c/2^9$ Hz
1	1	$f_c/2^{11}$ Hz

Note: LCD Frame Frequency = $\frac{\text{A/C Drive Frequency}}{\text{\# of active Backplane Drive lines}}$

2. UNSYNCHRONOUS DATA TRANSFER

0	0	1	1	0	0	0	0	30

The Normal Transfer of data from the Display Data RAM to the segment output latches latches occurs with the rising edge of CS. The UNSYNCHRONOUS DATA TRANSFER command implements this mode of data transfer, and also disables the SYNCHRONOUS DATA TRANSFER operation.

3. SYNCHRONOUS DATA TRANSFER

0	0	1	1	0	0	0	1	31

Data can also be transferred from the Display Data RAM to the segment output latches with the rising edge of f_c. The SYNCHRONOUS DATA TRANSFER command implements this mode of data transfer, and also disables the UNSYNCHRONOUS DATA TRANSFER operation.

4. INTERRUPT DATA TRANSFER

0 0 1 1 1 0 0 0	38

Occasionally, the Host microprocessor system may experience events, such as prioritized Hardware interrupts, that may disrupt communications with the μPD7225. Display Data transfers to the μPD7225 may be interrupted, without disrupting the μPD7225 internal display data protocol, by issuing an INTERRUPT DATA TRANSFER command at the beginning of the interrupt service routine. Display data updating may be resumed in an orderly fashion after the interrupt service routine is completed.

5. CLEAR Display Data

0 0 1 0 0 0 0 0	20

All locations in the Display Data RAM are set to zero by executing the CLEAR DISPLAY DATA command. The Data Pointer is also cleared, and set to its initial location.

6. CLEAR BLINKING DATA

0 0 0 0 0 0 0 0	00

All locations in to Blinking Data RAM are set to zero by executing the CLEAR BLINKING DATA command. The Data Pointer is also cleared, and set to its initial location.

7. LOAD DATA POINTER

0 0 0 D_4 D_3 D_2 D_1 D_0	E0-FF

To access a particular location in either the Display Data RAM, or the BLINKING DATA RAM the Data Pointer must be given the corresponding address of that location. The LOAD DATA POINTER command transfers 5 bits of immediate data to the Data Pointer.

8. WRITE DISPLAY DATA

1 1 0 1 D_3 D_2 D_1 D_0	D0-DF

The WRITE DISPLAY DATA command transfers 4 bits of immediate data to the Display Data RAM location addressed by the Data Pointer. After the transfer is complete, the Data Pointer is automatically incremented.

9. WRITE BLINKING DATA

1 1 0 0 D_3 D_2 D_1 D_0	C0-CF

The WRITE BLINKING DATA command transfers 4 bits of immediate data to the Blinking Data RAM location addressed by the Data Pointer. After the transfer is complete, the Data Pointer is automatically incremented.

10. ENABLE DISPLAY

0 0 0 1 0 0 0 1	11

The ENABLE DISPLAY command turns on the LCD, and starts the automatic display controller hardware of the μPD7225.

11. DISABLE DISPLAY

0 0 0 1 0 0 0 0	10

The DISABLE DISPLAY command turns off the LCD, and stops the automatic display controller hardware of the μPD7225.

12. ENABLE BLINKING

0 0 0 1 1 0 1 D_0	1A-1B

If a particular LCD application requires blinking several segments, the appropriate information must have been transferred to the Blinking Data RAM previously. The ENABLE BLINKING command selects the Blinking frequency according to the value of D_0, and turns the Blinking feature on.

D_0	Blinking Frequency
0	$f_c/2^{16}$ Hz
1	$f_c/2^{17}$ Hz

13. DISABLE BLINKING

0 0 0 1 1 0 0 0	18

The DISABLE BLINKING command turns the Blinking feature OFF.

14. ENABLE SEGMENT DECODER

0 0 0 1 0 1 0 1	15

The μPD7225 has an internal 8-segment Numeric data decoder, and an internal 15-segment Alpha-Numeric data decoder. These decoders can be used for automatic display data addressing, by the Host microprocessor to absorb some of the system overhead required to decode display data for the μPD7225.

The ENABLE SEGMENT DECODER command implements this mode of display data addressing. Upon execution, display data received by the μPD7225 is diverted to one of the segment decoders. The segment decoder then writes display data to the Display Data RAM. The distinction between 8-segment decoding and 15-segment decoding is made by the MSB of the display data:

MSB	Decoding Selected
0	8-segment Numeric
1	15-segment Alpha-Numeric

15. DISABLE SEGMENT DECODER

0 0 0 1 0 1 0 0	14

The DISABLE SEGMENT DECODER command stops the segment decode addressing, and enables the transfers of Display Data from the Host microprocessor directly to the Display Data RAM.

16. OR DISPLAY DATA

1	0	1	1	D_3	D_2	D_1	D_0	B0-BF

The OR DISPLAY DATA command performs a LOGICAL OR between the Display Data addressed by the Data Pointer, and 4 bits of immediate data. The result is written to the same Display Data location, and the Data Pointer is automatically incremented.

17. AND DISPLAY DATA

1	0	0	1	D_3	D_2	D_1	D_0	90-9F

The AND DISPLAY DATA command performs a LOGICAL AND between the Display Data addressed by the Data Pointer, and 4 bits of immediate data. The result is written to the same Display Data location, and the Data Pointer is automatically incremented.

18. OR BLINKING DATA

1	0	1	0	D_3	D_2	D_1	D_0	A0-AF

The OR BLINKING DATA command performs a LOGICAL OR between the Blinking Data addressed by the Data Pointer, and 4 bits of immediate data. The result is written to the same Blinking Data location, and the Data Pointer is automatically incremented.

19. AND BLINKING DATA

1	0	0	0	D_3	D_2	D_1	D_0	80-8F

The AND BLINKING DATA command performs a LOGICAL AND between the Blinking Data addressed by the Data Pointer, and 4 bits of immediate data. The result is written to the same Blinking Data location, and the Data Pointer is automatically incremented.

COMMAND SUMMARY

COMMAND	DESCRIPTION	INSTRUCTION CODE								
		BINARY								
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX
1. Mode Set	Set up Driving Mode of LCD, including: 1) Backplane drive 2) Display Bias 3) LCD Frame Frequency	0	1	0	D_4	D_3	D_2	D_1	D_0	40-5F
2. Unsychronous Data Transfer	Synchronize writing of display data with CS	0	0	1	1	0	0	0	0	30
3. Synchronous Data Transfer	Synchronize writing of display data with LCD Frame Frequency	0	0	1	1	0	0	0	1	31
4. Interrupt Data Transfer	Interrupt writing of display data	0	0	1	1	1	0	0	0	38
5. Clear Display Data	Clear the Display Data RAM and the Data Pointer	0	0	1	0	0	0	0	0	20
6. Clear Blinking Data	Clear the Blinking Data RAM and the Data Pointer	0	0	0	0	0	0	0	0	00
7. Load Data Pointer	Load Data Pointer with 5 Bits of Immediate Data	1	1	1	D_4	D_3	D_2	D_1	D_0	E0-FF
8. Write Display Data	Write 4 Bits of Immediate Data to the Display Data Location addressed by the Data Pointer; Increment Data Pointer	1	1	0	1	D_3	D_2	D_1	D_0	D0-DF
9. Write Blinking Data	Write 4 Bits of Immediate Data to the Blinking Data Location addressed by the Data Pointer; Increment Data Pointer	1	1	0	0	D_3	D_2	D_1	D_0	C0-CF
10. Enable Display	Start Automatic LCD Controller Hardware	0	0	0	1	0	0	0	1	11
11. Disable Display	Stop Automatic LCD Controller Hardware	0	0	0	1	0	0	0	0	10
12. Enable Blinking	Start the Blinking Operation at the Frequency Specified by 1 Bit of Immediate Data	0	0	0	1	1	0	1	D_0	1A-1B
13. Disable Blinking	Stop Blinking Operation	0	0	0	1	1	0	0	0	18
14. Enable Segment Decoder	Select 8-Segment Numeric or 15-Segment Alphanumeric Decoder Addressing	0	0	0	1	0	1	0	1	15
15. Disable Segment Decoder	Stop Segment Decoder Addressing; Return to individual segment addressing	0	0	0	1	0	1	0	0	14
16. OR Display Data	Perform a Logical OR between the Display Data addressed by the Data Pointer and 4 Bits of Immediate Data; Write Results to same Display Data Location; Increment Data Pointer	1	0	1	1	D_3	D_2	D_1	D_0	B0-BF
17. AND Display Data	Perform a Logical AND between the Display Data addressed by the Data Pointer and 4 Bits of Immediate Data; Write Result to same Display Data Location; Increment Data Pointer	1	0	0	1	D_3	D_2	D_1	D_0	90-9F
18. OR Blinking Data	Perform a Logical OR between Blinking Data addressed by the Data Pointer and 4 Bits of Immediate Data; Write Result to same Blinking Data Location; Increment Data Pointer	1	0	1	0	D_3	D_2	D_1	D_0	A0-AF
19. AND Blinking Data	Perform a Logical AND between Blinking Data addressed by the Data Pointer and 4 Bits of Immediate Data; Write Result to same Location; Increment Data Pointer	1	0	0	0	D_3	D_2	D_1	D_0	80-8F

ABSOLUTE MAXIMUM RATINGS*

Power Supply	−0.3V to +7.0V
All Inputs and Outputs with Respect to VSS	−0.3V to V_{DD} + 0.3V
Storage Temperature	−40°C to +125°C
Operating Temperature	−10°C to +70°C

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC ELECTRICAL CHARACTERISTICS

T_a = −10°C to +70°C; V_{DD} = +5.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
Supply Current	I_{DD}		100		μA	No Load
Input High Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	SI, $\overline{SCK}$, C/$\overline{D}$, $\overline{CS}$, $\overline{SYNC}$, $\overline{RESET}$
Input Low Voltage	V_{IL}	0		0.3 V_{DD}	V	SI, $\overline{SCK}$, C/$\overline{D}$, $\overline{CS}$, $\overline{SYNC}$, $\overline{RESET}$
Clock High Voltage	$V_{\phi H}$	0.7 V_{DD}		V_{DD}	V	CL_1, External Clock
Clock Low Voltage	$V_{\phi L}$	0		0.3 V_{DD}	V	CL_1, External Clock
High Level Leakage Current	I_{LIH}			10	μA	SI, $\overline{SCK}$, C/$\overline{D}$, $\overline{CS}$, $\overline{RESET}$ $V_I = V_{DD}$
Low Level Leakage Current	I_{LIL}			−10	μA	SI, $\overline{SCK}$, C/$\overline{D}$, $\overline{CS}$, $\overline{RESET}$ V_I = 0V
High Level Output Voltage	V_{OH}	V_{DD} −0.5			V	$\overline{BUSY}$, I_{OH} = −10 μA
Low Level Output Voltage	V_{OL}			0.5	V	$\overline{SYNC}$, $\overline{BUSY}$, I_{OL} = 550 μA, V_{DD} = 5.5V, T_a = 25°C
High Level Output Current	I_{OH}			−180	μA	$\overline{SYNC}$, V_O = 0.5, V_{DD} = 5.5V, T_a = 25°C

DC ELECTRICAL CHARACTERISTICS FOR LCD

$2.7 \leq V_{LCD} \leq V_{DD}$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
Backplane Drive Output Impedance	R_{COM}		2		kΩ	COM_0 - COM_3, Display Bias = 1/3 or Static
					kΩ	COM_0 - COM_3 Display Bias = 1/2
Segment Drive Output Impedance	$R_{\overline{SEG}}$		11		kΩ	$\overline{S_0}$ - $\overline{S_{31}}$

CAPACITANCE

$T_a = 25°C$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
Input Capacitance	C_I				pF	SI, $\overline{SCK}$, C/$\overline{D}$, $\overline{CS}$, $\overline{RESET}$
Output Capacitance	C_O				pF	CL_2, BUSY, COM_0 - COM_3, S_0-S_{31}
Input/Output Capacitance	C_{IO}				pF	SYNC
Clock Capacitance	C_{CLK}				pF	CL_1

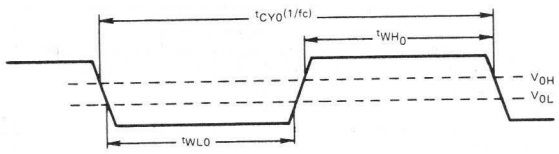
AC ELECTRICAL CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{DD} = +5.0V \pm 10\%$

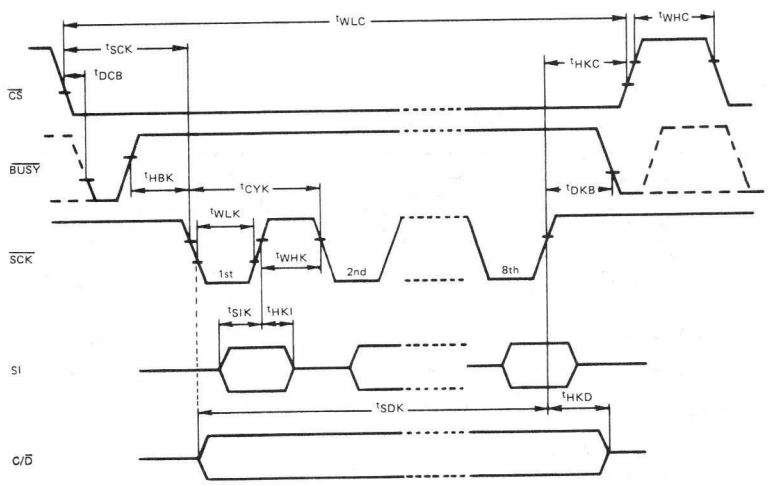
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
Clock Frequency	f_c		200		kHz	R_f = kΩ
Clock Cycle	$t_{CY\phi}$		5		μS	External Clock
Clock Pulse Width High	$t_{W\phi H}$				μS	External Clock
Clock Pulse Width Low	$t_{W\phi L}$				μS	External Clock
$\overline{SCK}$ Cycle	t_{CYK}	1			μS	
$\overline{SCK}$ Pulse Width High	t_{WK_H}				nS	
$\overline{SCK}$ Pulse Width Low	t_{WK_L}				nS	
$\overline{SCK}$ Hold Time	t_{HK_B}	0			nS	after $\overline{BUSY}$↑
SI Setup Time	t_{SI_K}	250			nS	to $\overline{SCK}$↑
SI Hold Time	t_{HK_I}	200			nS	after $\overline{SCK}$↑
$\overline{BUSY}$↓ Delay Time	t_{DB_C}	1			μS	after $\overline{CS}$↓
$\overline{BUSY}$↓ Delay Time	t_{DK_B}			3	μS	after 8th $\overline{SCK}$↑
C/$\overline{D}$ Setup Time	t_{SD_K}	9			μS	to 8th $\overline{SCK}$↑
C/$\overline{D}$ Hold Time	t_{HK_D}	1			μS	after 8th $\overline{SCK}$↑
$\overline{CS}$ Setup Time	t_{SC_K}				μS	to 1st $\overline{SCK}$↓
$\overline{CS}$ Hold Time	t_{HK_C}	1			μS	after 8th $\overline{SCK}$↑
High Level $\overline{CS}$ Pulse Width	t_{WH_C}	8 $t_{CY\phi}$			μS	
Low Level $\overline{CS}$ Pulse Width	t_{WL_C}	8 $t_{CY\phi}$			μS	

9

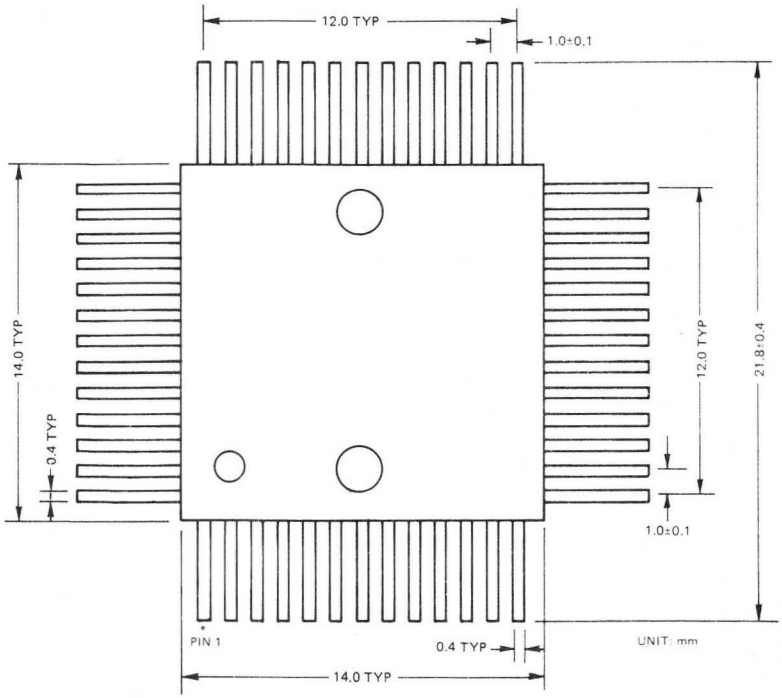
CLOCK WAVE FORM

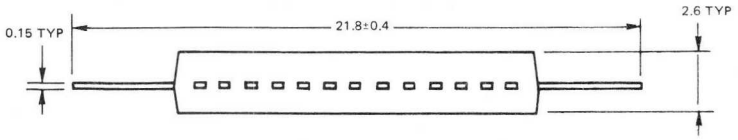


SERIAL INTERFACE TIMING



μPD7225G PACKAGE
DIMENSION





9

PROGRAMMABLE LCD CONTROLLER/DRIVER

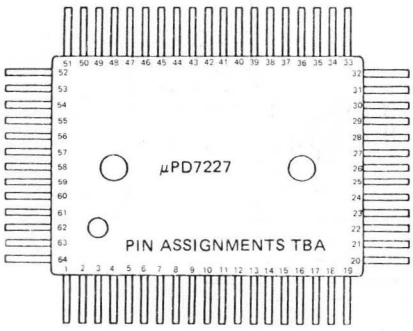
DESCRIPTION

The μPD7227 is a programmable peripheral device containing all the circuitry necessary for interfacing a microprocessor to a wide variety of dot matrix Liquid Crystal Displays (LCDs). The display controller hardware automatically synchronizes the drive signals for a multiplexed dot matrix LCD containing up to 16 rows and up to 48 columns. The μPD7227 is fully compatible with most microprocessors, and communicates with them through a 3-line, 8-bit serial I/O port. It can be easily configured into multiple chip designs for larger LCD applications, and includes an ASCII 5 x 7 dot matrix decoder to simplify alphanumeric display data decoding. The μPD7227 is manufactured with a low-power single 5V CMOS process, and is available in a 64-pin plastic flat package.

FEATURES

- Single Chip LCD Controller
- Direct LCD Drive
- Selectable 8- or 16-Backplane Multiplexed Drive
- Programmable Display Configurations
  - 8-Row by 40-Column Dot Matrix
  - Cascadable into
    - 16-Row Multiplexed Backplane Applications
    - 40-Column Drive Applications
- Selectable Display Bias Configuration
- Automatic Synchronization of Row and Column Drive Lines
- Dual 40 x 8 Bit RAMs for Display Data Storage
- Programmable Display Data Addressing
  - Individual Dot
  - 64-Character ASCII 5 x 7 Dot Matrix Decoder
- 8-Bit Serial Interface
- Compatible with most 4-Bit, 8-Bit, and 16-Bit Microprocessors
- Fully Cascadable for Larger LCD Applications
- Single +5V Power Supply
- CMOS Technology
- 64-Pin Plastic Flat Package

PIN CONFIGURATION

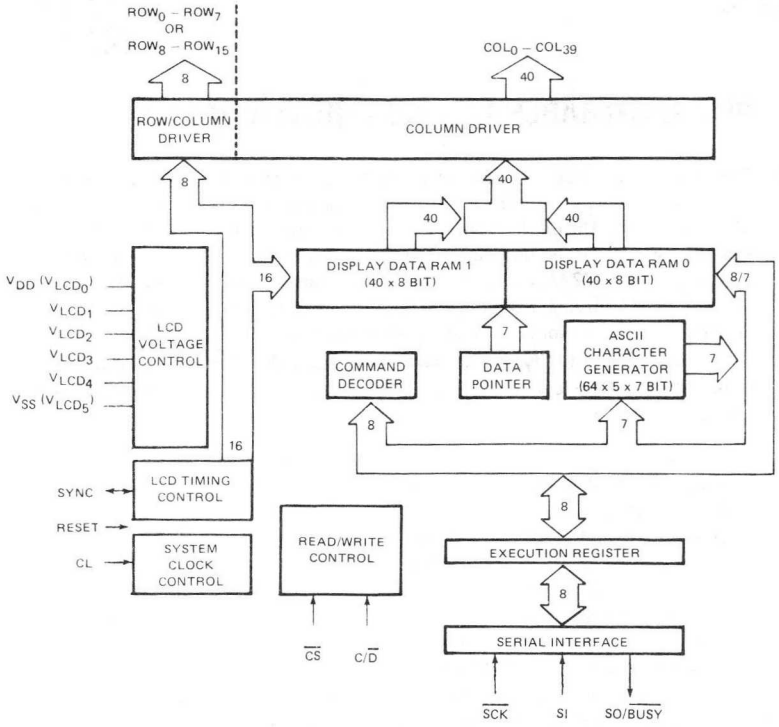


PIN NAMES

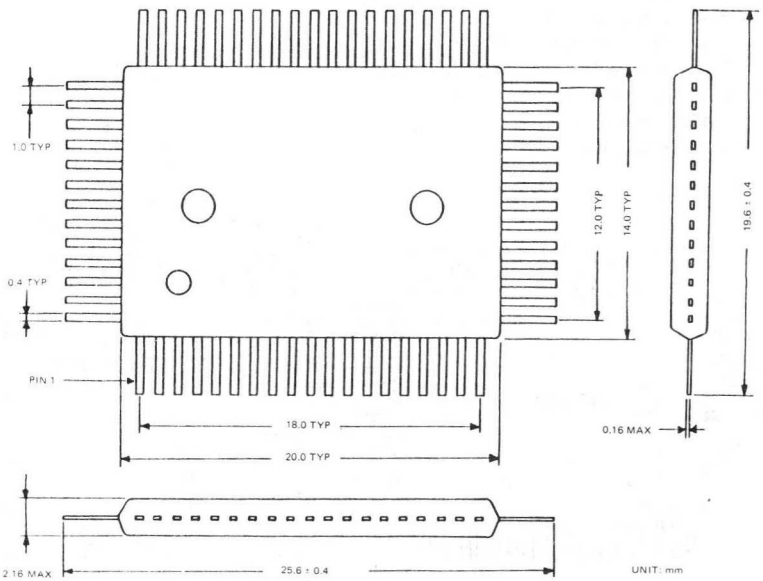
SYMBOL	DESCRIPTION
COL_0-COL_{39}	LCD Column Drive Outputs
ROW_0-ROW_7	LCD Row/Column Drive Outputs
V_{SS} (V_{LCD_0})	Ground
V_{LCD_1}-V_{LCD_4}	LCD Power Supply
V_{DD} (V_{LCD_5})	Power Supply Positive
$\overline{SCK}$	Serial Clock Input
SI	Serial Input
SO/$\overline{BUSY}$	Serial Output/Busy Output
$\overline{CS}$	Chip Select
C/$\overline{D}$	Command Data Select
SYNC	Synchronization Signal I/O Port for cascaded applications
CL	System Clock Input
RESET	Reset Input
NC	No Connection

9

BLOCK DIAGRAM



μPD7227G PACKAGE DIMENSIONS



DIGITAL SIGNAL PROCESSOR

DESCRIPTION

The NEC μPD7720 Signal Processing Interface (SPI) is an advanced architecture microcomputer optimized for signal processing algorithms. Its speed and flexibility allow the SPI to efficiently implement signal processing functions in a wide range of environments and applications.

The NEC SPI is the state of the art in signal processing today, and for the future.

APPLICATIONS

- Speech Synthesis and Analysis
- Digital Filtering
- Fast Fourier Transforms (FFT)
- Dual-Tone Multi-Frequency (DTMF) Transmitters/Receivers
- High Speed Data Modems
- Equalizers
- Adaptive Control
- Sonar/Radar Image Processing
- Numerical Processing

PERFORMANCE BENCHMARKS

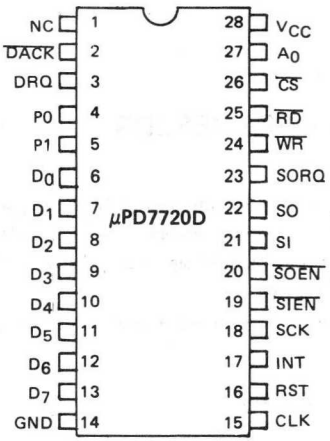
• Second Order Digital Filter (BiQuad)	2.25 μs
• SINE/COS of Angles	5.25 μs
• μ/A LAW to Linear Conversion	0.50 μs
• FFT: 32 Point Complex	0.7 ms
64 Point Complex	1.6 ms

FEATURES

- Fast Instruction Execution – 250 ns
- 16 Bit Data Word
- Multi-Operation Instructions for Optimizing Program Execution
- Large Memory Capacities
  - Program ROM 512 x 23 Bits
  - Coefficient ROM 510 x 13 Bits
  - Data RAM 128 x 16 Bits
- Fast (250 ns) 16 x 16-31 Bit Multiplier
- Dual Accumulators
- Four Level Subroutine Stack for Program Efficiency
- Multiple I/O Capabilities
  - Serial
  - Parallel
  - DMA
- Compatible with Most Microprocessors, Including:
  - μPD8080
  - μPD8085
  - μPD8086
  - μPD780 (Z80™*)
- Power Supply +5V
- Technology NMOS
- Package – 28 Pin Dip

*Z80 is a trademark of Zilog Corporation.

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

Fabricated in high speed NMOS, the μPD7720 SPI is a complete 16-bit microcomputer on a single chip. ROM space is provided for program and coefficient storage, while the on-chip RAM may be used for temporary data, coefficients and results. Computational power is provided by a 16-bit Arithmetic/Logic Unit (ALU) and a separate 16 x 16 bit fully parallel multiplier. This combination allows the implementation of a "sum of products" operation in a single 250 nsec instruction cycle. In addition, each arithmetic instruction provides for a number of data movement operations to further increase throughput. Two serial I/O ports are provided for interfacing to codecs and other serially-oriented devices while a parallel port provides both data and status information to conventional μP for more sophisticated applications. Handshaking signals, including DMA controls, allow the SPI to act as a sophisticated programmable peripheral as well as a stand alone microcomputer.

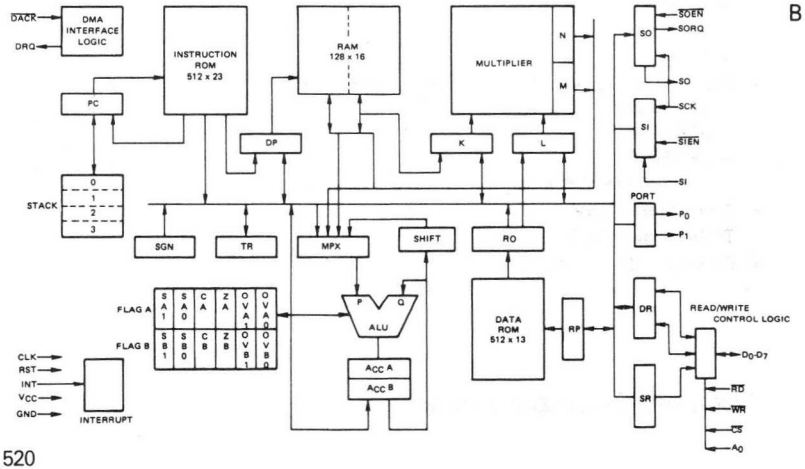
MEMORY

Memory is divided into three types, Program ROM, Data ROM, and Data RAM. The 512 x 23 bit words of Program ROM are addressed by a 9-bit Program Counter which can be modified by an external reset, interrupt, call, jump, or return instruction.

The Data ROM is organized in 512 x 13 bit words and is also addressed through a 9-bit ROM pointer (RP Reg.) which may be modified as part of an arithmetic instruction so that the next value is available for the next instruction. The Data ROM is ideal for storing the necessary coefficients, conversion tables and other constants for all your processing needs.

The Data RAM is 128 x 16 bit words and is addressed through a 7-bit Data Pointer (DP Reg.). The DP has extensive addressing features that operate simultaneously with arithmetic instructions so that no added time is taken for addressing or address modification.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN	NAME	I/O	FUNCTION
1	NC	I	No Connection.
2	$\overline{DACK}$	I	DMA Request Acknowledge. Indicates to the μPD7720 that the Data Bus is ready for a DMA transfer. ($\overline{DACK} = \overline{CS} \bullet A_0 = 0$)
3	DRQ	O	DMA Request signals that the μPD7720 is requesting a data transfer on the Data Bus.
4,5	P_0, P_1	O	P_0, P_1 are general purpose output control lines.
6-13	D_0-D_7	I/O Tristate	Port for data transfer between the Data Register or Status Register and Data Bus.
14	GND		
15	CLK	I	Single phase Master Clock input.
16	RST	I	Reset initializes the μPD7720 internal logic and sets the PC to 0.
17	INT	I	Interrupt. A low to high transition on this pin will (if interrupts are enabled by the program) execute a call instruction to location 100H.
18	SCK	I	Serial Data Input/Output Clock. A serial data bit is transferred when this pin is high.
19	$\overline{SIEN}$	I	Serial Input Enable. This line enables the shift clock to the Serial Input Register.
20	$\overline{SOEN}$	I	Serial Output Enable. This pin enables the shift clock to the Serial Output Register.
21	SI	I	Serial Data Input. This pin inputs 8 or 16 bit serial data words from an external device such as an A/D converter.
22	SO	O	Serial Data Output. This pin outputs 8 or 16 bit data words to an external device such as an D/A converter.
23	SORQ	O	Serial Data Output Request. Specifies to an external device that the Serial Data Register has been loaded and is ready for output. SORQ is reset when the entire 8 or 16 bit word has been transferred.
24	$\overline{WR}$	I	Write Control Signal writes the contents of data bus into the Data Register.
25	$\overline{RD}$	I	Read Control Signal. Enables an output to the Data Port from the Data or Status Register.
26	$\overline{CS}$	I	Chip Select. Enables data transfer with Data or Status Port with $\overline{RD}$ or $\overline{WR}$.
27	A_0	I	Selects Data Register for Read/Write (low) or Status Register for read (high).
28	V_{CC}		+5V Power

ARITHMETIC CAPABILITIES

General

One of the unique features of the SPI's architecture is its arithmetic facilities. With a separate multipler, ALU, and multiple internal data paths, the SPI is capable of carrying out a multiply, an add, or other arithmetic operation, and move data between internal registers in a single instruction cycle.

ALU

The ALU is a 16-bit 2's complement unit capable of executing 16 distinct operations on virtually any of the SPI's internal registers, thus giving the SPI both speed and versatility for efficient data management.

Accumulators (ACCA/ACCB)

Associated with the ALU are a pair of 16-bit accumulators, each with its own set of flags, which are updated at the end of each arithmetic instruction (except NOP). In addition to Zero Result, Sign Carry, and Overflow Flags, the SPI incorporates auxiliary Overflow and Sign Flags (SA1, SB1, OVA1, OVB1). These flags enable the detection of an overflow condition and maintain the correct sign after as many as 3 successive additions or subtractions.

FLAG A	SA1	SA0	CA	ZA	OVA1	OVA0
FLAG B	SB1	SB0	CB	ZB	OVB1	OVB0

ACC A/B FLAG REGISTERS

Sign Register (SGN)

When OVA1 (or OVB1) is set, the SA1 (or SB1) bit will hold the corrected sign of the overflow. The SGN Register will use SA1 (SB1) to automatically generate saturation constants 7FFFH(+) or 8000H(−) to permit efficient limiting of a calculated valve.

Multiplier

Thirty-one bit results are developed by a 16 x 16 bit 2's complement multiplier in 250 ns. The result is automatically latched in 2-16-bit registers M&N (LSB in N is zero) at the end of each instruction cycle. The ability to have a new product available and to be able to use it in each instruction cycle, provides significant advantages in maximizing processing speed for real time signal processing.

Stack

The SPI contains a 4-level program stack for efficient program usage and interrupt handling.

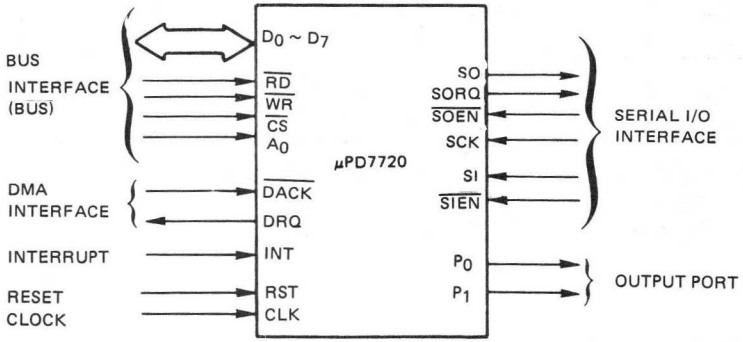
Interrupt

A single level interrupt is supported by the SPI. Upon sensing a high level on the INT terminal, a subroutine call to location 100H is executed. The EI bit of the status register is automatically reset to 0 thus disabling the interrupt facilities until reenabled under program control.

INPUT/OUTPUT

General

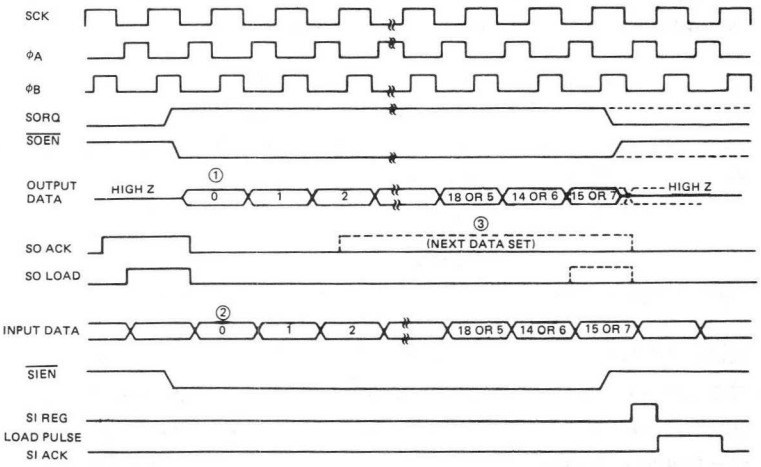
The NEC SPI has 3 communication ports; 2 serial and one 8-bit parallel, each with their own control lines for interface handshaking. The parallel port also includes DMA control lines (DRQ and $\overline{DACK}$) for high speed data transfer and reduced processor overhead. A general purpose 2 bit output (see Figure 1) port, rounds out a full complement of interface capability.



Serial I/O

Two shift registers (SI, SO) that are software-configurable to 8 or 16 bits and are externally clocked (SCK) provide simple interface between the SPI and serial peripherals such as, A/D and D/A converters, codecs, or other SPIs.

SERIAL I/O TIMING



① Data clocked out on falling edge of SCK.
② Data clocked in on rising edge of SCK.
③ Broken line denotes consecutive sending of next data.

PARALLEL I/O

The 8-bit parallel I/O port may be used for transferring data or reading the SPI's status. Data transfer is handled through a 16-bit Data Register (DR) that is software-configurable for double or single byte data transfers. The port is ideally suited for operating with 8080, 8085 and 8086 processor buses and may be used with other processors and computer systems.

PARALLEL R/W OPERATION

$\overline{CS}$	A_0	$\overline{WR}$	$\overline{RD}$	OPERATION
1	X	X	X	No effect on internal operation. D_0-D_7 are at high impedance levels.
X	X	1	1	
0	0	0	1	Data from D_0-D_7 is latched to DR ①
0	0	1	0	Contents of DR are output to D_0-D_7 ①
0	1	0	1	Illegal
0	1	1	0	Eight MSBs of SR are output to D_0-D_7
0	X	0	0	Illegal

① Eight MSBs or 8 LSBs of data register (DR) are used depending on DR status bit (DRS).
The condition of $\overline{DACK}$ = 0 is equivalent to A_0 = $\overline{CS}$ = 0.

Status Register (SR)

MSB LSB

RQM	USF1	USF0	DRS	DMA	DRC	SOC	SIC	EI	0	0	0	0	0	P1	P0

The status register is a 16-bit register in which the 8 most significant bits may be read by the system's MPU for the latest I/O and processing status.

RQM – (Request for Master): A read or write from DR to IDB sets RQM = 1. An Ext read (write) resets RQM = 0.

USF1 – (User Flag 1):
USF0 – (User Flag 0): General purpose flags which may be read by an external processor for user defined signalling

DRS – (DR Status): For 16 bit DR transfers (DRC = 0) DRS = 1 after first 8 bits have been transferred, DRS = 0 after all 16 bits

DMA– (DMA Enable): DMA = 0 (Non DMA transfer mode)
DMA = 1 (DMA transfer mode)

DRC – (DR Control): DRC = 0 (16 bit mode), DRC = 1 (8 bit mode)

SOC – (SO Control): SOC = 0 (16 bit mode), SOC = 1 (8 bit mode)

SIC – (SI Control): SIC = 0 (16 bit mode), SIC = 1 (8 bit mode)

EI – (Enable Interrupt): EI = 0 (interrupts disabled), EI = 1 (interrupts enabled)

P0/P1 (Ports 0 and 1): P0 and P1 directly control the state of output pins P0 and P1

INSTRUCTIONS

The SPI has 3 types of instructions all of which are one word, 23 bits long and execute in 250 ns.

A) Arithmetic/Move-Return (OP = 00/RT = 01)

	22 21	20 19 18 17 16 15	14	13 12	11 10 9	8	7 6 5 4	3 2 1 0
OP	0 0	P-SELECT / ALU	ASL	DP_L	DP_H·M	RPDCR	SRC	DST
RT	0 1	Same as OP instruction						

There are two instructions of this type, both of which are capable of executing all ALU functions listed in Table 2 on the value specified by the ALU input (i.e., P select field see Table 1).

Table 1. OP, RT

Mnemonic	P-Select Field D_{20} D_{19}	ALU Input
RAM	0 0	RAM
IDB	0 1	*Internal Data Bus
M	1 0	M Register
N	1 1	N Register

*Any value on the on-chip data bus. Value may be selected from any of registers listed in Table 7 source register selections.

Table 2. OP, RT

Mnemonic	ALU Field D_{18}	D_{17}	D_{16}	D_{15}	ALU Function	Flag A / Flag B	Flags Affected SA1 / SB1	SA0 / SB0	CA / CB	ZA / ZB	OVA1 / OVB1	OVA0 / OVB0
NOP	0	0	0	0	No Operation		–	–	–	–	–	–
OR	0	0	0	1	OR		Ø	‡	‡	Ø	Ø	Ø
AND	0	0	1	0	AND		Ø	‡	‡	Ø	Ø	Ø
XOR	0	0	1	1	Exclusive OR		Ø	‡	‡	Ø	Ø	Ø
SUB	0	1	0	0	Subtract		‡	‡	‡	‡	‡	Ø
ADD	0	1	0	1	ADD		‡	‡	‡	‡	‡	‡
SBB	0	1	1	0	Subtract with Borrow		‡	‡	‡	‡	‡	‡
ADC	0	1	1	1	Add with Carry		‡	‡	‡	‡	‡	‡
DEC	1	0	0	0	Decrement A_{CC}		‡	‡	‡	‡	‡	‡
INC	1	0	0	1	Increment A_{CC}		‡	‡	‡	‡	‡	‡
CMP	1	0	1	0	Complement A_{CC} (1's Complement)		‡	‡	‡	Ø	Ø	Ø
SHR1	1	0	1	1	1-bit R-Shift		‡	‡	‡	Ø	Ø	Ø
SHL1	1	1	0	0	1-bit L-Shift		‡	‡	‡	Ø	Ø	Ø
SHL2	1	1	0	1	2-bit L-Shift		Ø	‡	‡	Ø	Ø	Ø
SHL4	1	1	1	0	4-bit L-Shift		Ø	‡	‡	Ø	Ø	Ø
XCHG	1	1	1	1	8-bit Exchange		Ø	‡	‡	Ø	Ø	Ø

‡ Affected by result
– No affect
Ø Reset

Table 3. OP, RT

Mnemonic	ASL Field D_{14}	A_{CC} Selection
ACCA	0	A_{CC} A
ACCB	1	A_{CC} B

Table 4. OP, RT

Mnemonic	DP_L Field D_{13}	D_{12}	DP_3-DP_0
DPNOP	0	0	No Operation
DPINC	0	1	Increment DP_L
DPDEC	1	0	Decrement DP_L
DPCLR	1	1	Clear DP_L

Table 5. OP, RT

Mnemonic	DP_H-M Field D_{11}	D_{10}	D_9	Exclusive OR
M0	0	0	0	(DP_6 DP_5 DP_4) ¥ (0 0 0)
M1	0	0	1	DP_6 DP_5 DP_4 ¥ (0 0 1)
M2	0	1	0	DP_6 DP_5 DP_4 ¥ (0 1 0)
M3	0	1	1	DP_6 DP_5 DP_4 ¥ (0 1 1)
M4	1	0	0	DP_6 DP_5 DP_4 ¥ (1 0 0)
M5	1	0	1	DP_6 DP_5 DP_4 ¥ (1 0 1)
M6	1	1	0	DP_6 DP_5 DP_4 ¥ (1 1 0)
M7	1	1	1	DP_6 DP_5 DP_4 ¥ (1 1 1

Table 6. OP,RT

Mnemonic	RPDCR D_8	Operation
RPNOP	0	No Operation
RPDEC	1	Decrement RP

Besides the arithmetic functions these instructions can also modify (1) the RAM Data Pointer DP, (2) the Data ROM Pointer RP, and (3) move data along the on-chip data bus from a source register to a destination register (the possible source and destination registers are listed in Tables 7 and 8 respectively). The difference in the two instructions of this type is that one executes a subroutine or interrupt return at the end of the instruction cycle while the other does not.

Table 7. OP, RT

Mnemonic	SRC Field D_7	D_6	D_5	D_4	Specified Register
NON	0	0	0	0	NO Register
A	0	0	0	1	ACC A (Accumulator A)
B	0	0	1	0	ACC B (Accumulator B)
TR	0	0	1	1	TR Temporary Register
DP	0	1	0	0	DP Data Pointer
RP	0	1	0	1	RP ROM Pointer
RO	0	1	1	0	RO ROM Output Data
SGN	0	1	1	1	SGN Sign Register
DR	1	0	0	0	DR Data Register
DRNF	1	0	0	1	DR Data No Flag ①
SR	1	0	1	0	SR Status
SIM	1	0	1	1	SI Serial in MSB ②
SIL	1	1	0	0	SI Serial in LSB ③
K	1	1	0	1	K Register
L	1	1	1	0	L Register
MEM	1	1	1	1	RAM

① DR to IDB RQM not set. IN DMA DRQ not set.
② First bit in goes to MSB, last bit to LSB.
③ First bit in goes to LSB, last bit to MSB (bit reversed).

Table 7 — List of Registers Specified by the Source Field (SRC)

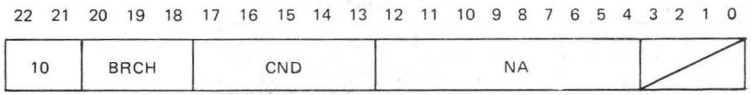
Table 8. OP, RT, LDI

Mnemonic	DST Field D_3	D_2	D_1	D_0	Specified Register
@NON	0	0	0	0	NO Register
@A	0	0	0	1	ACC A (Accumulator A)
@B	0	0	1	0	ACC B (Accumulator B)
@TR	0	0	1	1	TR Temporary Register
@DP	0	1	0	0	DP Data Pointer
@RP	0	1	0	1	RP ROM Pointer
@DR	0	1	1	0	DR Data Register
@SR	0	1	1	1	SR Status Register
@SOL	1	0	0	0	SO Serial Out LSB ①
@SOM	1	0	0	1	SO Serial Out MSB ②
@K	1	0	1	0	K (Mult)
@KLR	1	0	1	1	IDB → K ROM → L ③
@KLM	1	1	0	0	Hi RAM → K IDB → L ④
@L	1	1	0	1	L (Mult)
@NON	1	1	1	0	NO Register
@MEM	1	1	1	1	RAM

① LSB is first bit out.
② MSB is first bit out.
③ Internal data bus to K and ROM to L register.
④ Contents of RAM address specified by $DP_6 = 1$ (i.e., 1, DP_5, DP_4,-DP_0) is placed in K register. IDB is placed in L.

Table 8 — List of Registers Specified by the Destination Field (DST)

B) Jump/Call/Branch



JP Instruction Field Specifications

Three types of execution address modification instructions are accommodated by the processor and are listed in Table 9. All of the instructions, if unconditional or the specified condition is true, take their next program execution address from the Next Address field (NA), otherwise PC = PC + 1.

Table 9. Branch Field Selections (BRCH)

20	19	18	Instruction
1	0	0	Uncondition jump
1	0	1	Subroutine call
0	1	0	Condition jump

For the conditional jump instruction, the condition field specifies the jump condition. Table 10 lists all the instruction mnemonics of the J/C/B OP codes.

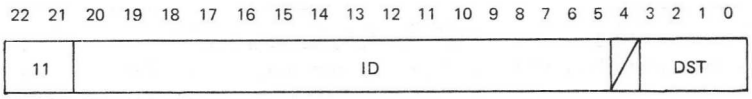
The SPI offers all the execution modification instructions necessary for efficient, data, I/O and arithmetic control.

Table 10. Condition Field Specifications

Mnemonic	BRCH/CND Fields								Conditions
	D_{20}	D_{19}	D_{18}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	
JMP	1	0	0	0	0	0	0	0	No Condition
CALL	1	0	1	0	0	0	0	0	No Condition
JNCA	0	1	0	0	0	0	0	0	CA = 0
JCA	0	1	0	0	0	0	0	1	CA = 1
JNCB	0	1	0	0	0	0	1	0	CB = 0
JCB	0	1	0	0	0	0	1	1	CB = 1
JNZA	0	1	0	0	0	1	0	0	ZA = 0
JZA	0	1	0	0	0	1	0	1	ZA = 1
JNZB	0	1	0	0	0	1	1	0	ZB = 0
JZB	0	1	0	0	0	1	1	1	ZB = 1
JNOVA0	0	1	0	0	1	0	0	0	OVA0 = 0
JOVA0	0	1	0	0	1	0	0	1	OVA0 = 1
JNOVB0	0	1	0	0	1	0	1	0	OVB0 = 0
JOVB0	0	1	0	0	1	0	1	1	OVB0 = 1
JNOVA1	0	1	0	0	1	1	0	0	OVA1 = 0
JOVA1	0	1	0	0	1	1	0	1	OVA1 = 1
JNOVB1	0	1	0	0	1	1	1	0	OVB1 = 0
JOVB1	0	1	0	0	1	1	1	1	OVB1 = 1
JNSA0	0	1	0	1	0	0	0	0	SA0 = 0
JSA0	0	1	0	1	0	0	0	1	SA0 = 1
JNSB0	0	1	0	1	0	0	1	0	SB0 = 0
JSB0	0	1	0	1	0	0	1	1	SB0 = 1
JNSA1	0	1	0	1	0	1	0	0	SA1 = 0
JSA1	0	1	0	1	0	1	0	1	SA1 = 1
JNSB1	0	1	0	1	0	1	1	0	SB1 = 0
JSB1	0	1	0	1	0	1	1	1	SB1 = 1
JDPL0	0	1	0	1	1	0	0	0	$DP_L = 0$
JDPLF	0	1	0	1	1	0	0	1	DP_L = F (HEX)
JNSIAK	0	1	0	1	1	0	1	0	SI ACK = 0
JSIAK	0	1	0	1	1	0	1	1	SI ACK = 1
JNSOAK	0	1	0	1	1	1	0	0	SO ACK = 0
JSOAK	0	1	0	1	1	1	0	1	SO ACK = 1
JNRQM	0	1	0	1	1	1	1	0	RQM = 0
JRQM	0	1	0	1	1	1	1	1	RQM = 1

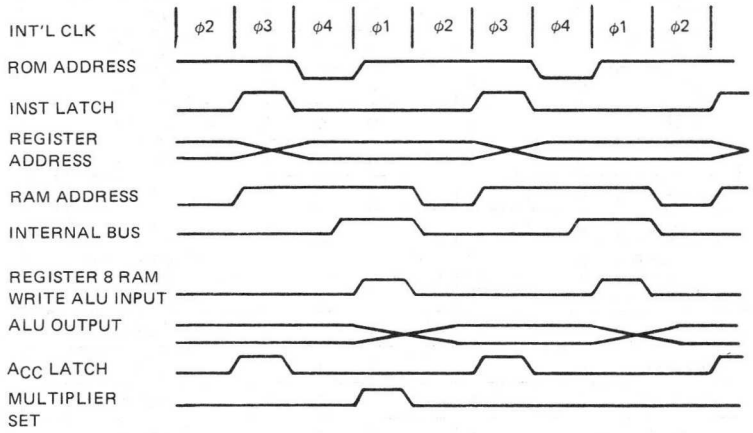
*BRCH or CND values not in this table are prohibited.

C) Load Data (LDI)



The Load Data instruction will take the 16-bit value contained in the Immediate Data field (ID) and place it in the location specified by the Destination field (DST) (see Table 8).

Load Data Field Specifications



INSTRUCTION EXECUTION TIMING

ABSOLUTE MAXIMUM RATINGS*

Voltage (V_{CC} Pin) . . . . . −0.5 to +7.0 Volts ①
Voltage, Any Input . . . . . −0.5 to +7.0 Volts ①
Voltage, Any Output . . . . . −0.5 to +7.0 Volts ①
Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +150°C

Note: ① With respect to GND.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10 ~ +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} +0.5	V	
CLK Low Voltage	$V_{\phi L}$	−0.5		0.45	V	
CLK High Voltage	$V_{\phi H}$	3.5		V_{CC} +0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Input Load Current	I_{LIL}			−10	μA	V_{IN} = 0V
Input Load Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Output Float Leakage	I_{LOL}			−10	μA	V_{OUT} = V_{CC}
Output Float Leakage	I_{LOH}			10	μA	V_{OUT} = 0.47V
Power Supply Current	I_{CC}		200	280	mA	

CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
CLK, SCK Input Capacitance	C_ϕ			20	pF	f_c = 1 MHz
Input Pin Capacitance	C_{IN}			10	pF	
Output Pin Capacitance	C_{OUT}			20	pF	

9

AC CHARACTERISTICS

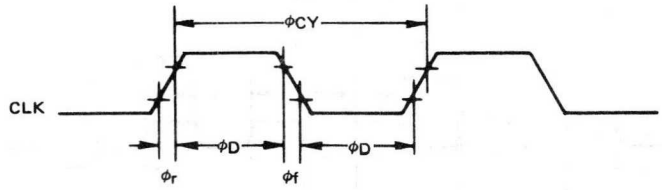
$T_a = -10 \sim +70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
CLK Cycle Time	ϕCY	125		2000	ns	
CLK Pulse Width	ϕD	50			ns	
CLK Rise Time	ϕR			20	ns	
CLK Fall Time	ϕF			20	ns	
Address Setup Time for $\overline{RD}$	t_{AR}	0			ns	
Address Hold Time for $\overline{RD}$	t_{RA}	0			ns	
RD Pulse Width	t_{RR}	200			ns	
Data Delay from $\overline{RD}$	t_{RD}			150	ns	$C_L = 100$ pF
Read to Data Floating	t_{DF}	20		100	ns	$C_L = 100$ pF
Address Setup Time for $\overline{WR}$	t_{AW}	0			ns	
Address Hold Time for $\overline{WR}$	t_{WA}	0			ns	
$\overline{WR}$ Pulse Width	t_{WW}	200			ns	
Data Setup Time for $\overline{WR}$	t_{DW}	150			ns	
Data Hold Time for $\overline{WR}$	t_{WD}	0			ns	
DRQ Delay	t_{AM}			150	ns	$C_L = 100$ pF
SCK Cycle Time	t_{SCY}	480		DC	ns	
SCK Pulse Width	t_{SCK}	230			ns	
SCK Rise/Fall Time	t_{RSC}			20	ns	
SORQ Delay	t_{DRQ}	30		150	ns	$C_L = 100$ pF
$\overline{SOEN}$ Setup Time	t_{SOC}	50			ns	
$\overline{SOEN}$ Hold Time	t_{CSO}	10			ns	
SO Delay	t_{DCK}			150	ns	
SO Delay from SORQ	t_{DZRQ}	*				
SO Delay from SCK	t_{DZSC}	*				
SO Delay from $\overline{SOEN}$	t_{DZE}	*				
$\overline{SOEN}$ to SO Floating	t_{HZE}	*				
SCK to SO Floating	t_{HZSC}	*				
SORQ to SO Floating	t_{HZRQ}	*				
$\overline{SIEN}$, SI Setup Time	t_{DC}	50			ns	
$\overline{SIEN}$, SI Hold Time	t_{CD}	20			ns	
P_0, P_1 Delay	t_{DP}			300	ns	
RST Pulse Width	t_{RST}	4			ϕCY	
INT Pulse Width	t_{INT}	8			ϕCY	

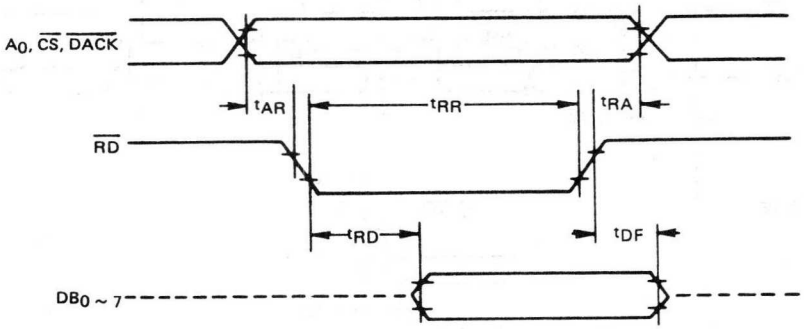
*To be specified

TIMING WAVEFORMS

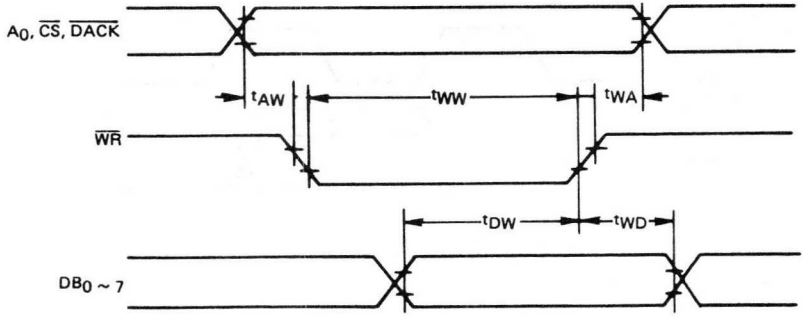
CLOCK



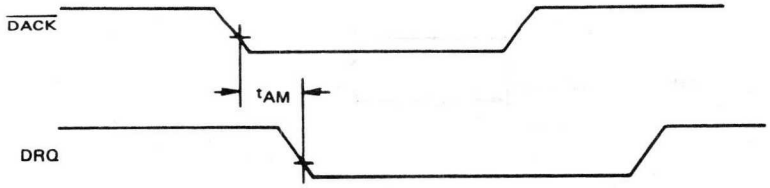
READ OPERATION



WRITE OPERATION

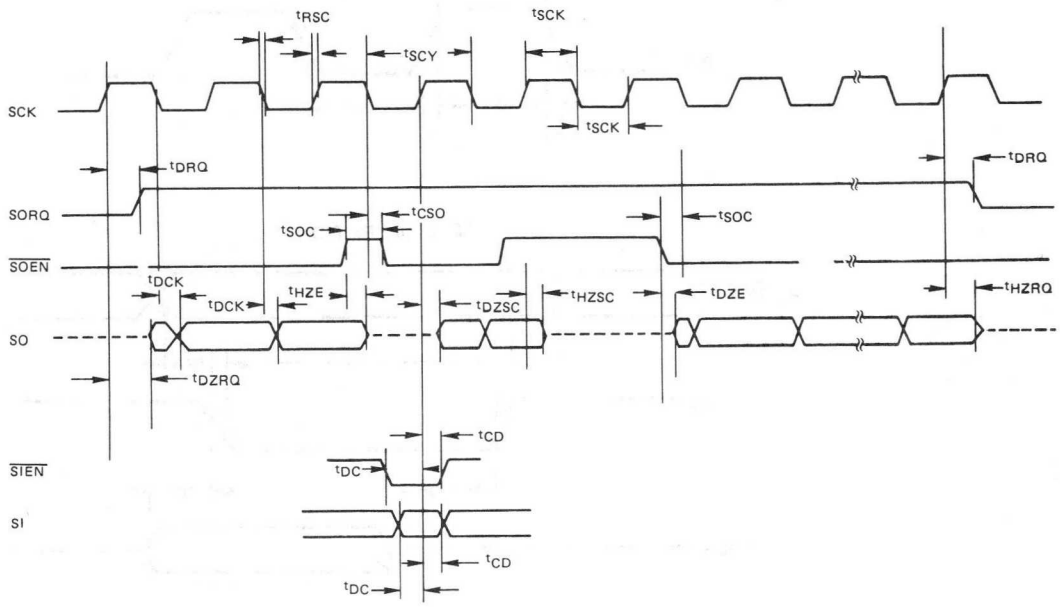


DMA OPERATION

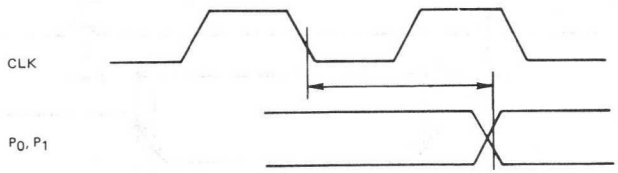


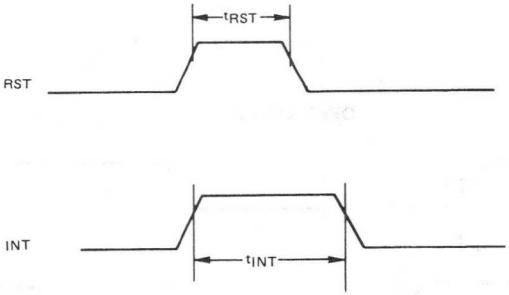
TIMING WAVEFORMS
(CON'T.)

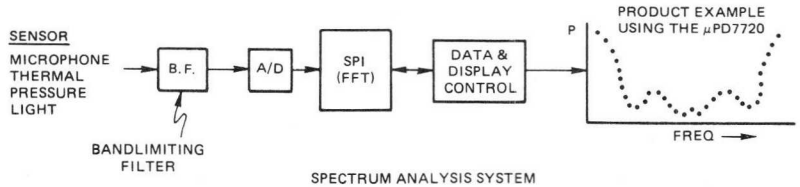
SERIAL TIMING



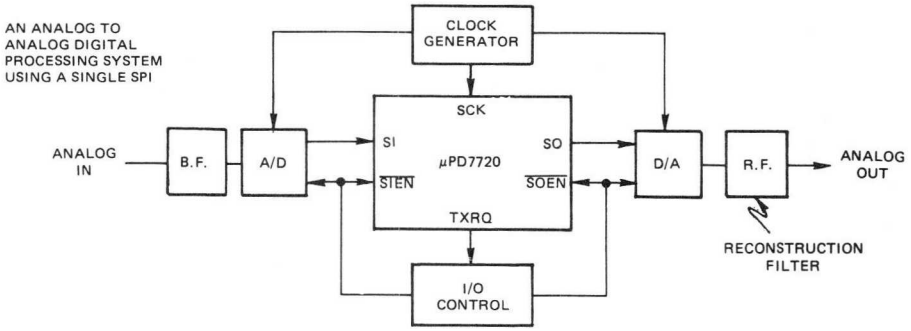
PORT OUTPUT

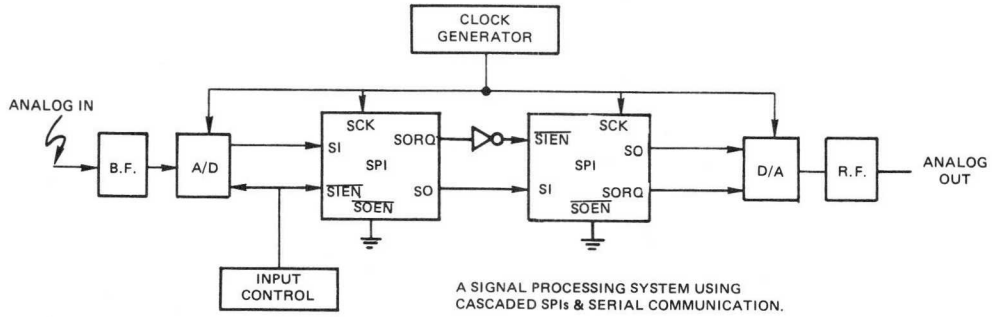




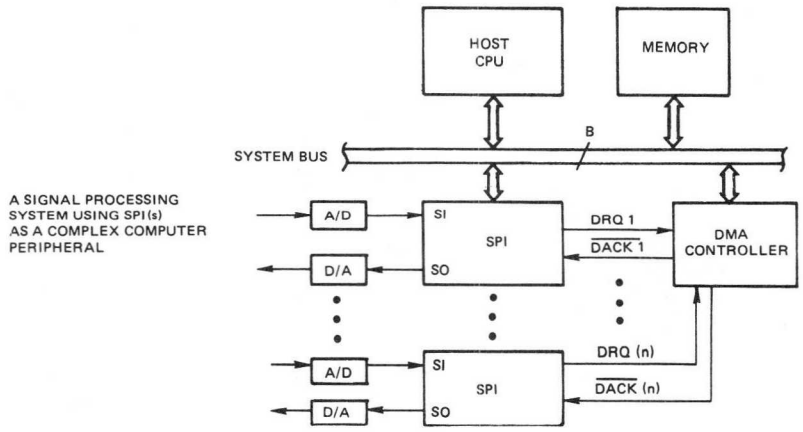


SPECTRUM ANALYSIS SYSTEM





A SIGNAL PROCESSING SYSTEM USING
CASCADED SPIs & SERIAL COMMUNICATION.



A SIGNAL PROCESSING
SYSTEM USING SPI(s)
AS A COMPLEX COMPUTER
PERIPHERAL

9

2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

μPD8155
μPD8155-2
μPD8156
μPD8156-2

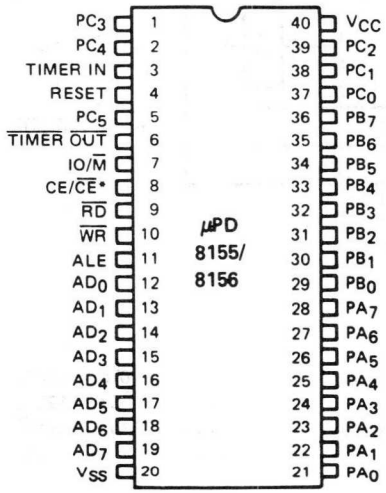
DESCRIPTION

The μPD8155 and μPD8156 are μPD8085A family components having 256 X 8 Static RAM, 3 programmable I/O ports and a programmable timer. They directly interface to the multiplexed μPD8085A bus with no external logic. The μPD8155 has an active low chip enable while the μPD8156 is active high.

FEATURES

- 256 X 8-Bit Static RAM
- Two Programmable 8-Bit I/O Ports
- One Programmable 6-Bit I/O Port
- Single Power Supplies: +5 Volt, ±10%
- Directly interfaces to the μPD8085A and μPD8085A-2
- Available in 40 Pin Plastic Packages

PIN CONFIGURATION



*μPD8155: $\overline{CE}$
μPD8156: CE

Rev/2

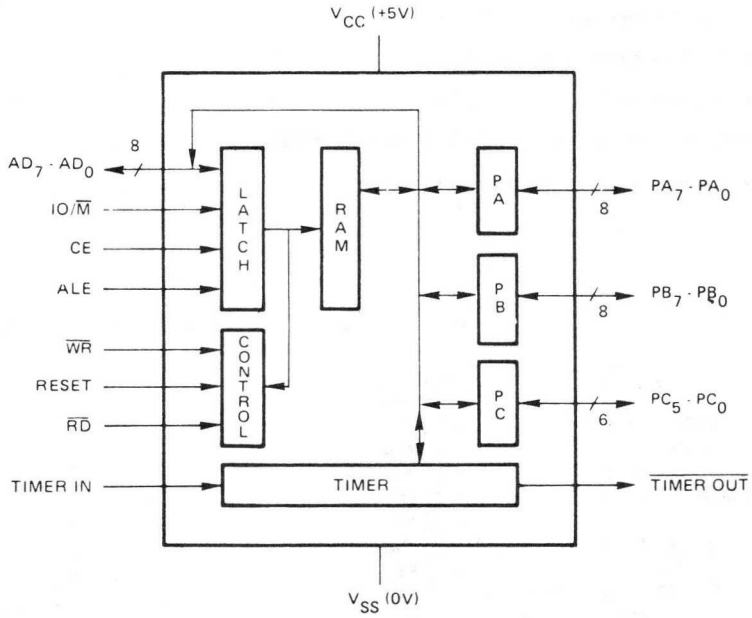
FUNCTIONAL DESCRIPTION

The μPD8155 and μPD8156 contain 2048 bits of Static RAM organized as 256 X 8. The 256 word memory location may be selected anywhere within the 64K memory space by using combinations of the upper 8 bits of address from the μPD8085A as a chip select.

The two general purpose 8-bit ports (PA and PB) may be programmed for input or output either in interrupt or status mode. The single 6-bit port (PC) may be used as control for PA and PB or general purpose input or output port. The μPD8155 and μPD8156 are programmed for their system personalities by writing into their Command/Status Registers (C/S) upon system initialization.

The timer is a single 14-bit down counter which is programmable for 4 modes of operation; see Timer Section.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Plastic Package)	-40°C to +125°C
Voltage on Any Pin	-0.3 to +7 Volts①
Power Dissipation	1.5 W

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 2, 5 39, 38, 37	PC_3, PC_4, PC_5 PC_2, PC_1, PC_0	Port C	Used as control for PA and PB or as a 6-bit general purpose port
3	TIMER IN	Timer Clock In	Clock input to the 14-bit binary down counter
4	RESET	Reset In	From μPD8085A system reset to set PA, PB, PC to the input mode
6	$\overline{\text{TIMER OUT}}$	Timer Counter Output	The output of the timer function
7	IO/$\overline{M}$	I/O or Memory Indicator	Selects whether operation to and from the chip is directed to the internal RAM or to I/O ports
8	CE/$\overline{CE}$	Chip Enable	Chip Enable Input. Active low for μPD8155 and active high for μPD8156
9	$\overline{RD}$	Read Strobe	Causes Data Read
10	$\overline{WR}$	Write Strobe	Causes Data Write
11	ALE	Address Low Enable	Latches low order address in when valid
12-19	$AD_0 - AD_7$	Low Address/Data	3-State address/data bus to interface directly to μPD8085A
20	V_{SS}	Ground	Ground Reference
21-28	$PA_0 - PA_7$	Port A	General Purpose I/O Port
29-36	$PB_0 - PB_7$	Port B	General Purpose I/O Port
40	V_{CC}	5 Volt Input	Power Supply

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 10\%$

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage		V_{IL}	-0.5		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{CC}+0.5	V	
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage		V_{OH}	2.4			V	I_{OH} = 400 μA
Input Leakage		I_{IL}			±10	μA	$V_{IN} = V_{CC}$ to 0V
Output Leakage Current		I_{LO}			±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CC} Supply Current		I_{CC}			180	mA	
Chip Enable Leakage	μPD8155	I_{IL} (CE)			+100	μA	$V_{IN} = V_{CC}$ to 0V
	μPD8156	I_{IL}(CE)			-100	μA	

9

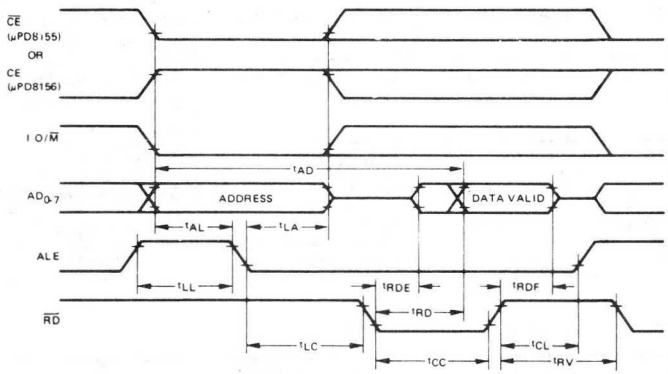
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = 5V ± 10%

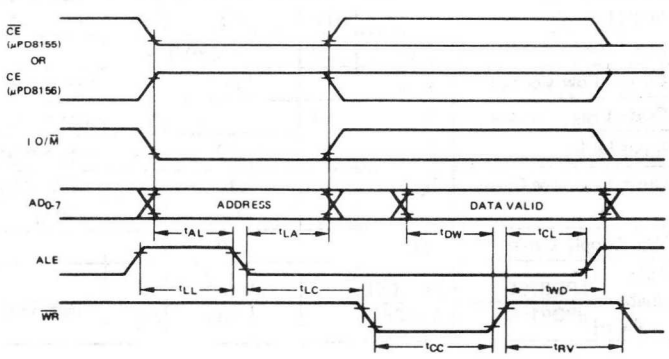
PARAMETER	SYMBOL	LIMITS 8155/8156 MIN	LIMITS 8155/8156 MAX	LIMITS 8155-2/8156-2 MIN	LIMITS 8155-2/8156-2 MAX	UNIT	TEST CONDITIONS
Address to Latch Set Up Time	t_{AL}	50		30		ns	
Address Hold Time after Latch	t_{LA}	80		30		ns	
Latch to READ/WRITE Control	t_{LC}	100		40		ns	
Valid Data Out Delay from READ Control	t_{RD}		170		140	ns	
Address Stable to Data Out Valid	t_{AD}		400		330	ns	
Latch Enable Width	t_{LL}	100		70		ns	
Data Bus Float After READ	t_{RDF}	0	100	0	80	ns	
READ/WRITE Control to Latch Enable	t_{CL}	20		10		ns	
READ/WRITE Control Width	t_{CC}	250		200		ns	
Data In to WRITE Set Up Time	t_{DW}	150		100		ns	
Data In Hold Time After WRITE	t_{WD}	0		0		ns	
Recovery Time Between Controls	t_{RV}	300		200		ns	150 pF Load
WRITE to Port Output	t_{WP}		400		300	ns	
Port Input Setup Time	t_{PR}	70		50		ns	
Port Input Hold Time	t_{RP}	50		10		ns	
Strobe to Buffer Full	t_{SBF}		400		300	ns	
Strobe Width	t_{SS}	200		150		ns	
READ to Buffer Empty	t_{RBE}		400		300	ns	
Strobe to INTR On	t_{SI}		400		300	ns	
READ to INTR Off	t_{RDI}		400		300	ns	
Port Setup Time to Strobe	t_{PSS}	50		0		ns	
Port Hold Time After Strobe	t_{PHS}	120		100		ns	
Strobe to Buffer Empty	t_{SBE}		400		300	ns	
WRITE to Buffer Full	t_{WBE}		400		300	ns	
WRITE to INTR Off	t_{WI}		400		300	ns	
TIMER-IN to TIMER-OUT Low	t_{TL}		400		300	ns	
TIMER-IN to TIMER-OUT High	t_{TH}		400		300	ns	
Data Bus Enable from READ Control	t_{RDE}	10		10		ns	

TIMING WAVEFORMS

READ CYCLE

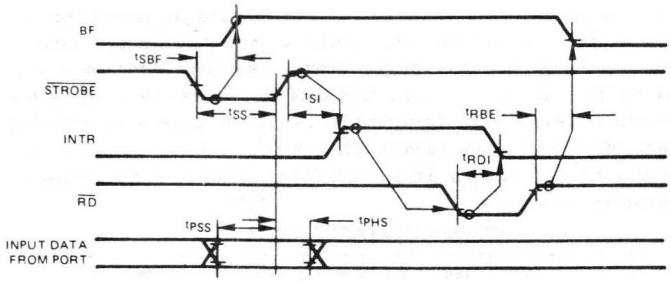


WRITE CYCLE

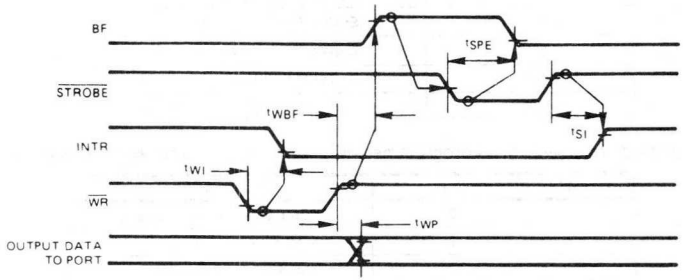


TIMING WAVEFORMS
(CONT.)

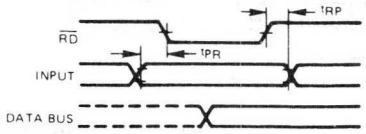
STROBED INPUT MODE



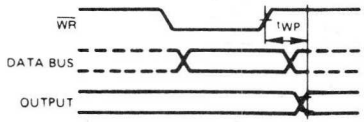
STROBED OUTPUT MODE



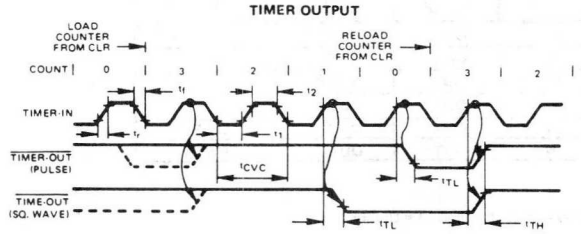
BASIC INPUT MODE



BASIC OUTPUT MODE



TIMER OUTPUT



COUNTDOWN FROM 3 TO 0

	μPD8155/8156	μPD8155-2/8156-2
tCYC	320 ns MIN.	200 ns MIN.
tRISE & tFALL	30 ns MAX.	30 ns MAX.
t1	80 ns MIN.	40 ns MIN.
t2	120 ns MIN.	70 ns MIN.
tTL	TIMER-IN to $\overline{\text{TIMER-OUT}}$ LOW (TO BE DEFINED).	
tTH	TIMER-IN to $\overline{\text{TIMER-OUT}}$ HIGH (TO BE DEFINED).	

9

COMMAND STATUS REGISTER

The Command Status Register is an 8-bit register which must be programmed before the μPD8155/8156 may perform any useful functions. Its purpose is to define the mode of operation for the three ports and the timer. Programming of the device may be accomplished by writing to I/O address XXXXX000 (X denotes don't care) with a specific bit pattern. Reading of the Command Status Register can be accomplished by performing an I/O read operation at address XXXXX000. The pattern returned will be a 7-bit status report of PA, PB and the Timer. The bit patterns for the Command Status Register are defined as follows:

COMMAND STATUS WRITE

TM2	TM1	IEB	IEA	PC_2	PC_1	PB	PA

where:

TM2-TM1	Define Timer Mode
IEB	Enable Port B Interrupt
IEA	Enable Port A Interrupt
PC_2-PC_1	Define Port C Mode
PB/PA	Define Port B/A as In or Out ①

The Timer mode of operation is programmed as follows during command status write:

TM2	TM1	TIMER MODE
0	0	Don't Affect Timer Operation
0	1	Stop Timer Counting
1	0	Stop Counting after TC
1	1	Start Timer Operation

Interrupt enable status is programmed as follows:

IEB/IEA	INTERRUPT ENABLE PORT B/A
0	No
1	Yes

Port C may be placed in four possible modes of operation as outlined below. The modes are selected during command status write as follows:

PC_2	PC_1	PORT C MODE
0	0	ALT 1
0	1	ALT 3
1	0	ALT 4
1	1	ALT 2

The function of each pin of port C in the four possible modes is outlined as follows:

PIN	ALT 1	ALT 2	ALT 3 ②	ALT 4 ②
PC0	IN	OUT	A INTR	A INTR
PC1	IN	OUT	A BF	A BF
PC2	IN	OUT	A $\overline{STB}$	A $\overline{STB}$
PC3	IN	OUT	OUT	B INTR
PC4	IN	OUT	OUT	B BF
PC5	IN	OUT	OUT	B $\overline{STB}$

Notes: ① PB/PA Sets Port B/A Mode: 0 = Input; 1 = Output

② In ALT 3 and ALT 4 mode the control signals are initialized as follows:

CONTROL	INPUT	OUTPUT
$\overline{STB}$ (Input Strobe)	Input Control	Input Control
INTR (Interrupt Request)	Low	High
BF (Buffer Full)	Low	Low

COMMAND STATUS REGISTER (CONT.)

COMMAND STATUS READ

	TI	INTE B	B BF	INTR B	INTE A	A BF	INTR A

Where the function of each bit is as follows:

TI	Defines a Timer Interrupt. Latched high at TC and reset after reading the CS register or starting a new count.
INTE B/A	Defines If Port B/A Interrupt is Enabled. High = enabled.
B/A BF	Defines If Port B/A Buffer is Full-Input Mode or Empty-Output Mode. High = active.
INTR B/A	Port B/A Interrupt Request. High = active.

The programming address summary for the status, ports, and timer are as follows:

I/O Address	Number of Bits	Function
XXXXX000	8	Command Status
XXXXX001	8	PA
XXXXX010	8	PB
XXXXX011	6	PC
XXXXX100	8	Timer-Low
XXXXX101	8	Timer-High

TIMER

The Internal Timer is a 14-bit binary down counter capable of operating in 4 modes. Its desired mode of operation is programmable at any time during operation. Any TTL clock meeting timer in requirements (See AC Characteristics) may be used as a time base and fed to the timer input. The timer output may be looped around and cause an interrupt or used as I/O control. The operational modes are defined as follows and programmed along with the 6 high bits of timer data.

M2	M1	Operation
0	0	High at Start, Low During Second Half of Count
0	1	Square Wave (Period = Count Length, Auto Reload at TC)
1	0	Single Pulse at TC
1	1	Single Pulse at TC with Auto Reload

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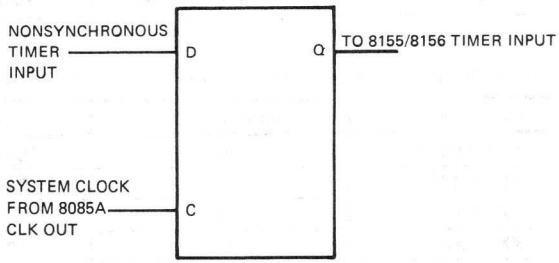
TIMER (CONT.)

Programming the timer requires two words to be written to the μPD8155/8156 at I/O address XXXXX100 and XXXXX101 for the low and high order bytes respectively. Valid count length must be between 2_H and $3FFF_H$. The bit assignments for the high and low programming words are as follows:

Word	Bit Pattern								I/O Address
High Byte	M_2	M_1	T13	T12	T11	T10	T9	T8	XXXXX101
Low Byte	T7	T6	T5	T4	T3	T2	T1	T0	XXXXX100

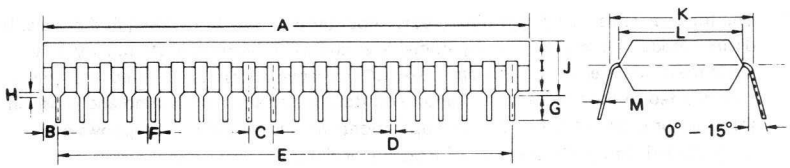
The control of the timer is performed by TM2 and TM1 of the Command Status Word.

Note that counting will be stopped by a hardware reset and a START command must be issued via the Command Status Register to begin counting. A new mode and/or count length can be loaded while counter is counting, but will not be used until a START command is issued.



When using the timer of the 8155/8156 care must be taken if the timer input is an external, nonsynchronous event. To sync this signal to the system clock the flip-flop shown should be used.

PACKAGE OUTLINE
μPD8155C
μPD8156C



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

EIGHT-BIT INPUT/OUTPUT PORT

DESCRIPTION

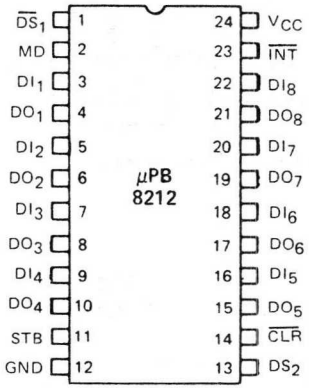
The μPB8212 input/output port consists of an 8-bit latch with three-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the control and generation of interrupts to the microprocessor.

The device is multimode in nature and can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

FEATURES

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current – 0.25 mA Max.
- Three State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8080A Processor
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count
- Available in 24-pin Plastic and Cerdip Packages

PIN CONFIGURATION

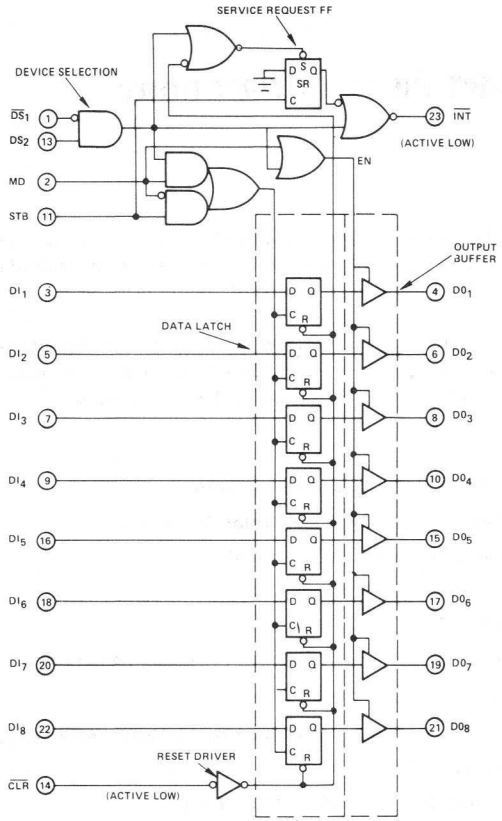


PIN NAMES

$DI_1 - DI_8$	Data In
$DO_1 - DO_8$	Data Out
$\overline{DS_1}$, DS_2	Device Select
MD	Mode
STB	Strobe
$\overline{INT}$	Interrupt (Active Low)
$\overline{CLR}$	Clear (Active Low)

9

BLOCK DIAGRAM



STB	MD	$(\overline{DS_1} \cdot DS_2)$	DATA OUT EQUALS
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

$\overline{CLR}$	$(\overline{DS_1} \cdot DS_2)$	STB	SR ②	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	0	0	③	③
1	↘	0	1	1
1	0	↘	0	0
1	1	0	1	0
1	1	↘	0	0

Notes: ① $\overline{CLR}$ resets data latch sets SR flip-flop. (No effect on output buffer)
② Internal SR flip-flop
③ Previous data remains

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	125 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current ACK, DS_2, CR, $DI_1 - DI_8$ Inputs	I_F		−0.14	−0.25	mA	$V_F = 0.45V$
Input Load Current MD Input	I_F		−0.25	−0.75	mA	$V_F = 0.45V$
Input Load Current $\overline{DS_1}$ Input	I_F		−0.26	−1.0	mA	$V_F = 0.45V$
Input Leakage Current ACK, DS, CR, $DI_1 - DI_8$ Inputs	I_R			10	μA	$V_R = 5.25V$
Input Leakage Current MD Input	I_R			30	μA	$V_R = 5.25V$
Input Leakage Current $\overline{DS_1}$ Input	I_R			40	μA	$V_R = 5.25V$
Input Forward Voltage Clamp	V_C		−0.85	−1.3	V	$I_C = -5$ mA
Input "Low" Voltage	V_{IL}			0.85	V	
Input "High" Voltage	V_{IH}	2.0			V	
Output "Low" Voltage	V_{OL}		0.26	0.45	V	$I_{OL} = 15$ mA
Output "High" Voltage	V_{OH}	3.65	4.0		V	$I_{OH} = -1$ mA
Short Circuit Output Current	I_{SC}	−15	−38	−75	mA	$V_O = 0V$
Output Leakage Current High Impedance State	I_O			20	μA	$V_O = 0.45V/5.25V$
Power Supply Current	I_{CC}		103	130	mA	

CAPACITANCE ①

$T_a = 25°C$; $V_{CC} = +5V$; $V_{BIAS} = 2.5V$; $f = 1$ MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		7	12	pF	$\overline{DS_1}$, MD
Input Capacitance	C_{IN}		4	9	pF	DS_2, CLR, STB, $DI_1 - DI_8$
Output Capacitance	C_{OUT}		6	12	pF	$DO_1 - DO_8$

Note: ① This parameter is periodically sampled and not 100% tested

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Pulse Width	t_{pw}	30			ns	Input Pulse Amplitude = 2.5V
Data To Output Delay	t_{pd}		20	30	ns	
Write Enable To Output Delay	t_{we}			40	ns	Input Rise and Fall Times = 5 ns
Data Setup Time	t_{set}	15			ns	
Data Hold Time	t_h	20			ns	Between 1V and 2V
Reset to Output Delay	t_r			40	ns	Measurement made at 1.5V with 15 mA and 30 pF Test Load
Set To Output Delay	t_s			30	ns	
Output Enable/Disable Time	t_e/t_d			45	ns	①
Clear To Output Delay	t_c			55	ns	②

Notes: ① $R_1 = 300\Omega/10K\Omega$; $R_2 = 600\Omega/1K\Omega$
② $R_1 = 300\Omega$; $R_2 = 600\Omega$

9

Data Latch

The 8 flip-flops that compose the data latch are of a "D" type design. The output (Q) of the flip-flop follows the data input (D) while the clock input (C) is high. Latching occurs when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$).
(Note: Clock (C) Overrides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to three-state, non-inverting output buffers. These buffers have a common control line (EN); enabling the buffer to transmit the data from the outputs of the data latch (Q) or disabling the buffer, forcing the output into a high impedance state (three-state).

This high-impedance state allows the designer to connect the μPB8212 directly to the microprocessor bi-directional data bus.

Control Logic

The μPB8212 has four control inputs: $\overline{DS}_1$, DS_2, MD and STB. These inputs are employed to control device selection, data latching, output buffer state and the service request flip-flop.

$\overline{DS}_1$, DS_2 (Device Select)

These two inputs are employed for device selection. When $\overline{DS}_1$ is low and DS_2 is high ($\overline{DS}_1 \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

Service Request Flip-Flop (SR)

The (SR) flip-flop is employed to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output (Q) of the (SR) flip-flop is connected to an inverting input of a "NOR" gate. The other input of the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS}_1 \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

MD (Mode)

This input is employed to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is in the output mode (high) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS}_1 \cdot DS_2$).

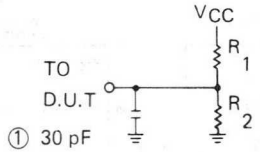
When MD is in the input mode (low) the output buffer state is determined by the device selection logic ($\overline{DS}_1 \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

STB is employed as the clock (C) to the data latch for the input mode (MD = 0) and to synchronously reset the service request flip-flop (SR).

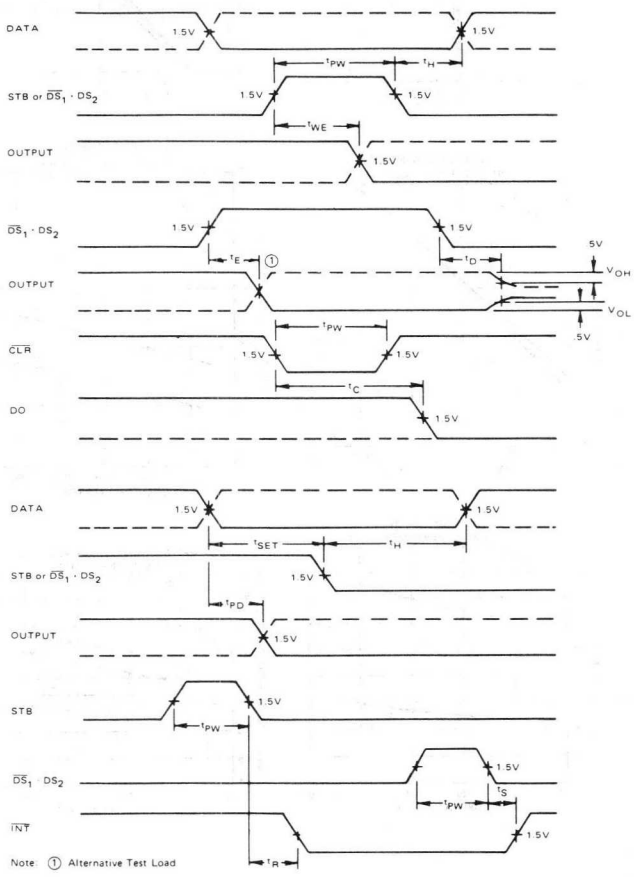
Note that the SR flip-flop triggers on the negative edge of STB which overrides $\overline{CLR}$.

TIMING WAVEFORMS



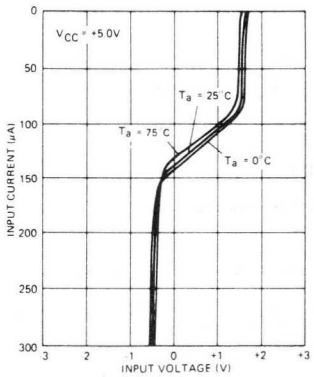
TEST CIRCUIT

Note: ① Including Jig and Probe Capacitance

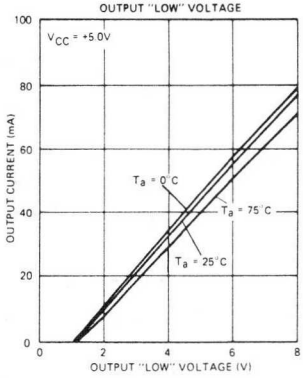


TYPICAL CHARACTERISTICS

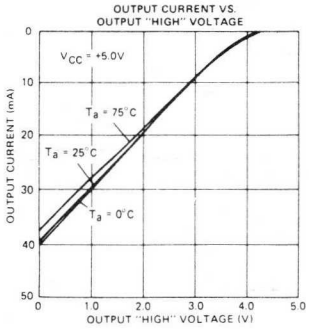
INPUT CURRENT VS. INPUT VOLTAGE



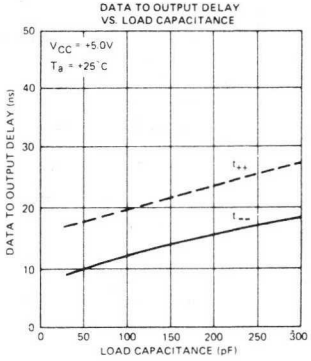
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



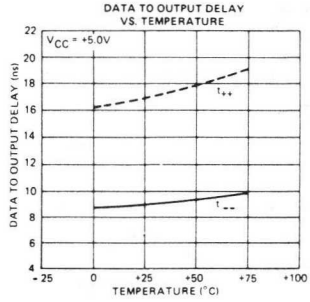
OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



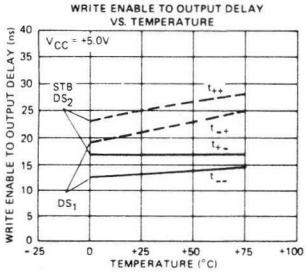
DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE



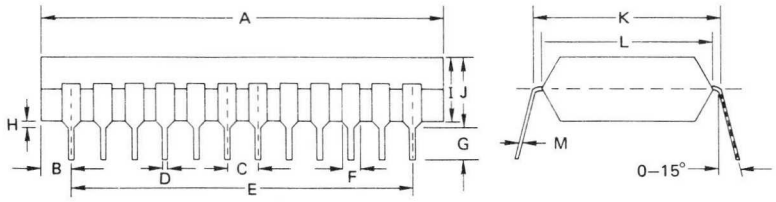
DATA TO OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE



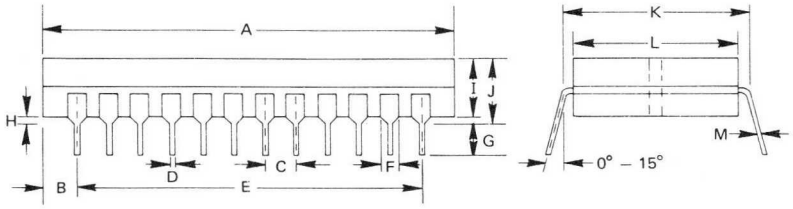
PACKAGE OUTLINE
μPB8212C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPB8212D'



(CERDIP)

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

PRIORITY INTERRUPT CONTROLLER

DESCRIPTION

The μPB8214 is an eight-level priority interrupt controller. Designed to simplify interrupt driven microcomputer systems, the μPB8214 requires a single +5V power supply and is packaged in a 24 pin plastic Dual-in-line package.

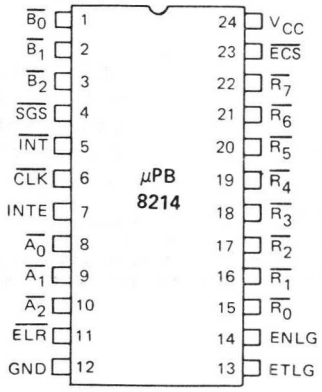
The μPB8214 accepts up to eight interrupts, determines which has the highest priority and then compares that priority with a software created current status register. If the incoming requires is of a higher priority than the interrupt currently being serviced, an interrupt request to the processor is generated. Vector information that identifies the interrupting device is also generated.

The interrupt structure of the microcomputer system can be expanded beyond eight interrupt levels by cascading μPB8214s. The μPB8214's interrupt and vector information outputs are open collector and control signals are provided to simplify expansion of the interrupt structure.

FEATURES

- Eight Priority Levels
- Current Status Register and Priority Comparator
- Easily Expanded Interrupt Structure
- Single +5 Volt Supply

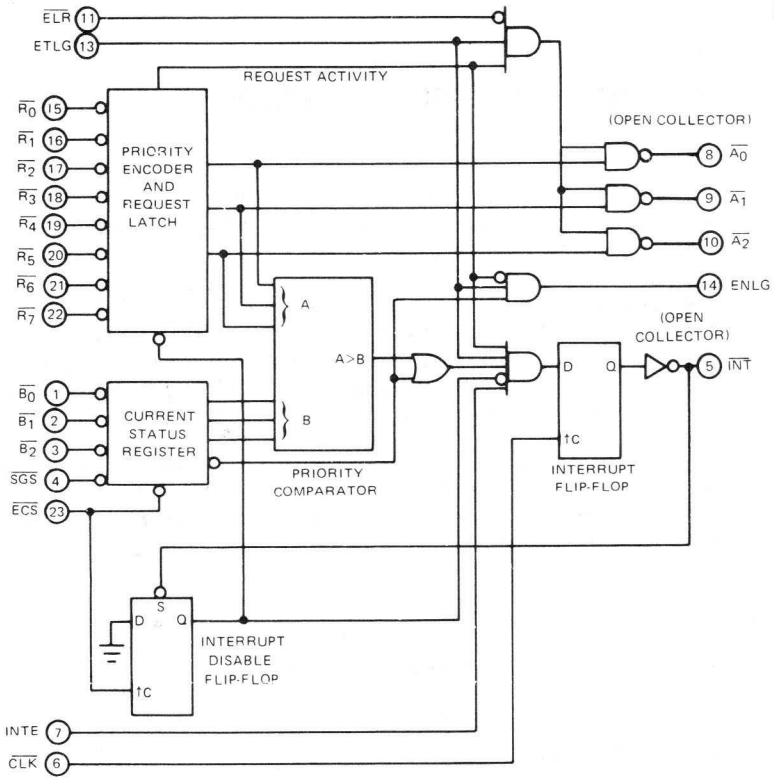
PIN CONFIGURATION



PIN NAMES

Inputs		
$\overline{R_0}$ $\overline{R_7}$	Request Levels ($\overline{R_7}$ Highest Priority)	
$\overline{B_0}$ $\overline{B_2}$	Current Status	
$\overline{SGS}$	Status Group Select	
$\overline{ECS}$	Enable Current Status	
INTE	Interrupt Enable	
$\overline{CLK}$	Clock (INT F-F)	
$\overline{ELR}$	Enable Level Read	
ETLG	Enable This Level Group	
Outputs		
$\overline{A_0}$ $\overline{A_2}$	Request Levels	Open
$\overline{INT}$	Interrupt (Act. Low)	Collector
ENLG	Enable Next Level Group	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
All Output and Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	100 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Clamp Voltage (all inputs)	V_C			-1.0	V	I_C= -5mA
Input Forward Current: ETLG input	I_F		-.15	-0.5	mA	V_F=0.45V
all other inputs			-.08	0.25	mA	
Input Reverse Current: ETLG input	I_R			80	μA	V_R=5.25V
all other inputs				40	μA	
Input LOW Voltage: all inputs	V_{IL}			0.8	V	V_{CC}=5.0V
Input HIGH Voltage: all inputs	V_{IH}	2.0			V	V_{CC}=5.0V
Power Supply Current	I_{CC}		90	130	mA	②
Output LOW Voltage: all outputs	V_{OL}		.3	.45	V	I_{OL}=10mA
Output HIGH Voltage: ENLG output	V_{OH}	2.4	3.0		V	I_{OH}= -1mA
Short Circuit Output Current: ENLG output	I_{OS}	-20	-35	-55	mA	V_{OS}=0V, V_{CC}=5.0V
Output Leakage Current: $\overline{INT}$ and $\overline{A_0}$–$\overline{A_2}$	I_{CEX}			100	μA	V_{CEX}=5.25V

CAPACITANCE ③

$T_a = 25°C$

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		5	10	pF	V_{BIAS}=2.5V
Output Capacitance	C_{OUT}		7	12	pF	V_{CC}=5V f=1mHz

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
$\overline{CLK}$ Cycle Time	t_{CY}	80	50		ns	Input pulse
$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	t_{PW}	25	15		ns	amplitude: 2.5 Volts
INTE Setup Time to $\overline{CLK}$	t_{ISS}	16	12		ns	
INTE Hold Time after $\overline{CLK}$	t_{ISH}	20	10		ns	
ETLG Setup Time to $\overline{CLK}$	t_{ETCS}④	25	12		ns	Input rise and fall
ETLG Hold Time After $\overline{CLK}$	t_{ETCH}④	20	10		ns	times: 5 ns between
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECCS}④	80	50		ns	1 and 2 Volts
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECCH}⑤	0			ns	
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECRS}⑤	110	70		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECRH}⑤	0				Output loading of
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECSS}④	75	70		ns	15 mA and 30 pF.
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECSH}④	0			ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{CLK}$	t_{DCS}④	70	50		ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time After $\overline{CLK}$	t_{DCH}④	0			ns	Speed measurements
$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{CLK}$	t_{RCS}⑤	90	55		ns	taken at the 1.5 Volts
$\overline{R_0}$–$\overline{R_7}$ Hold Time After $\overline{CLK}$	t_{RCH}⑤	0			ns	levels.
$\overline{INT}$ Setup Time to $\overline{CLK}$	t_{ICS}	55	35		ns	
$\overline{CLK}$ to $\overline{INT}$ Propagation Delay	t_{CI}		15	25	ns	
$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{INT}$	t_{RIS}⑥	10	0		ns	
$\overline{R_0}$–$\overline{R_7}$ Hold Time After $\overline{INT}$	t_{RIH}⑥	35	20		ns	
$\overline{R_0}$–$\overline{R_7}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{RA}		80	100	ns	
$\overline{ELR}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ELA}		40	55	ns	
$\overline{ECS}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ECA}		100	120	ns	
ETLG to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ETA}		35	70	ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{ECS}$	t_{DECS}⑥	15	10		ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time After $\overline{ECS}$	t_{DECH}⑥	15	10		ns	
$\overline{R_0}$–$\overline{R_7}$ to ENLG Propagation Delay	t_{REN}		45	70	ns	
ELTG to ENLG Propagation Delay	t_{ETEN}		20	25	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECRN}		85	90	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECSN}		35	55	ns	

Notes:
① Typical values are for T_a=25°C, V_{CC}=5.0V
② $\overline{B_0}$–$\overline{B_2}$, $\overline{SGS}$, $\overline{CLK}$, $\overline{R_0}$–$\overline{R_4}$ grounded, all other inputs and all outputs open.
③ This parameter is periodically sampled and not 100% tested.
④ Required for proper operation if INTE is enabled during next clock pulse.
⑤ These times are not required for proper operation but for desired change in interrupt flip-flop.
⑥ Required for new request or status to be properly loaded.

9

FUNCTIONAL DESCRIPTION

General

The μPB8214 is an LSI device designed to simplify the circuitry required to implement an interrupt driven microcomputer system. Up to eight interrupting devices can be connected to a μPB8214, which will assign priority to incoming interrupt requests and accept the highest. It will also compare the priority of the highest incoming request with the priority of the interrupt being serviced. If the serviced interrupt has a higher priority, the incoming request will not be accepted.

A system with more than eight interrupting devices can be implemented by interconnecting additional μPB8214s. In order to facilitate this expansion, control signals are provided for cascading the controllers so that there is a priority established among the controllers. In addition, the interrupt and vector information outputs are open collector.

Priority Encoder and Request Latch

The priority encoder portion of the μPB8214 accepts up to eight active low interrupt requests ($\overline{R_0}$–$\overline{R_7}$). The circuit assigns priority to the incoming requests, with $\overline{R_7}$ having the highest priority and $\overline{R_0}$ the lowest. If two or more requests occur simultaneously, the μPB8214 accepts the one having the highest priority. Once an incoming interrupt request is accepted, it is stored by the request latch and a three-bit code is output. As shown in the following table, the outputs, ($\overline{A_0}$–$\overline{A_2}$) are the complement of the request level (modulo 8) and directly correspond to the bit pattern required to generate the one byte RESTART (RST) instructions recognized by an 8080A. Simultaneously with the $\overline{A_0}$–$\overline{A_2}$ outputs, a system interrupt request ($\overline{INT}$) is output by the μPB8214. It should be noted that incoming interrupt requests that are *not* accepted are not latched and must remain as an input to the μPB8214 in order to be serviced.

FUNCTIONAL DESCRIPTION (CONT.)

Interrupt Control Circuitry

The μPB8214 contains two flip-flops and several gates which determine whether an accepted interrupt request to the μPB8214 will generate a system interrupt to the 8080A. A condition gate drives the D input of the interrupt flip-flop whenever an interrupt request has been completely accepted. This requires that: the ETLG (Enable This Level Group) and INTE (Interrupt Enable) inputs to the μPB8214 are high; the $\overline{ELR}$ input is low; the incoming request must be of a higher priority than the contents of the current status register; and the μPB8214 must have been enabled to accept interrupt requests by the clearing of the interrupt disable flip-flop.

Once the condition gate drives the D input of the interrupt flip-flop high, a system interrupt ($\overline{INT}$) to the 8080A is generated on the next rising edge of the $\overline{CLK}$ input to the μPB8214. This $\overline{CLK}$ input is typically connected to the $\phi 2$ (TTL) output of an 8224 so that 8080A set-up time specifications are met. When $\overline{INT}$ is generated, it sets the interrupt disable flip-flop so that no additional system interrupts will be generated until it is reset. It is reset by driving $\overline{ECS}$ (Enable Current Status) low, thereby writing into the current status register.

It should be noted that the open collector $\overline{INT}$ output from the μPB8214 is active for only one clock period and thus must be externally latched for inputting to the 8080A. Also, because the $\overline{INT}$ output is open collector, when μPB8214's are cascaded, an $\overline{INT}$ output from any one will set all of the interrupt disable flip-flops in the array. Each μPB8214's interrupt disable flip-flop must then be cleared individually in order to generate subsequent system interrupts.

FUNCTIONAL DESCRIPTION (CONT.)

RESTART GENERATION TABLE

PRIORITY REQUEST		RST	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
			1	1	$\overline{A_2}$	$\overline{A_1}$	$\overline{A_0}$	1	1	1
LOWEST	$\overline{R_0}$	7	1	1	1	1	1	1	1	1
	$\overline{R_1}$	6	1	1	1	1	0	1	1	1
	$\overline{R_2}$	5	1	1	1	0	1	1	1	1
	$\overline{R_3}$	4	1	1	1	0	0	1	1	1
	$\overline{R_4}$	3	1	1	0	1	1	1	1	1
	$\overline{R_5}$	2	1	1	0	1	0	1	1	1
	$\overline{R_6}$	1	1	1	0	0	1	1	1	1
HIGHEST	$\overline{R_7}$	0*	1	1	0	0	0	1	1	1

*CAUTION: RST 0 will vector the program counter to location 0 (zero) and invoke the same routine as the "RESET" input to 8080A.

Current Status Register

The current status register is designed to prevent an incoming interrupt request from overriding the servicing of an interrupt with higher priority. Via software, the priority level of the interrupt being serviced by the microprocessor is written into the current status register on $\overline{B_0}$–$\overline{B_2}$. The bit pattern written should be the complement of the interrupt level.

The interrupt level currently being serviced is written into the current status register by driving $\overline{ECS}$ (Enable Current Status) low. The μPB8214 will only accept interrupts with a higher priority than the value contained by the current status register. Note that the programmer is free to use the current status register for other than as above. Other levels may be written into it. The comparison may be completely disabled by driving $\overline{SGS}$ (Status Group Select) low when $\overline{ECS}$ is driven low. This will cause the μPB8214 to accept incoming interrupts only on the basis of their priority to each other.

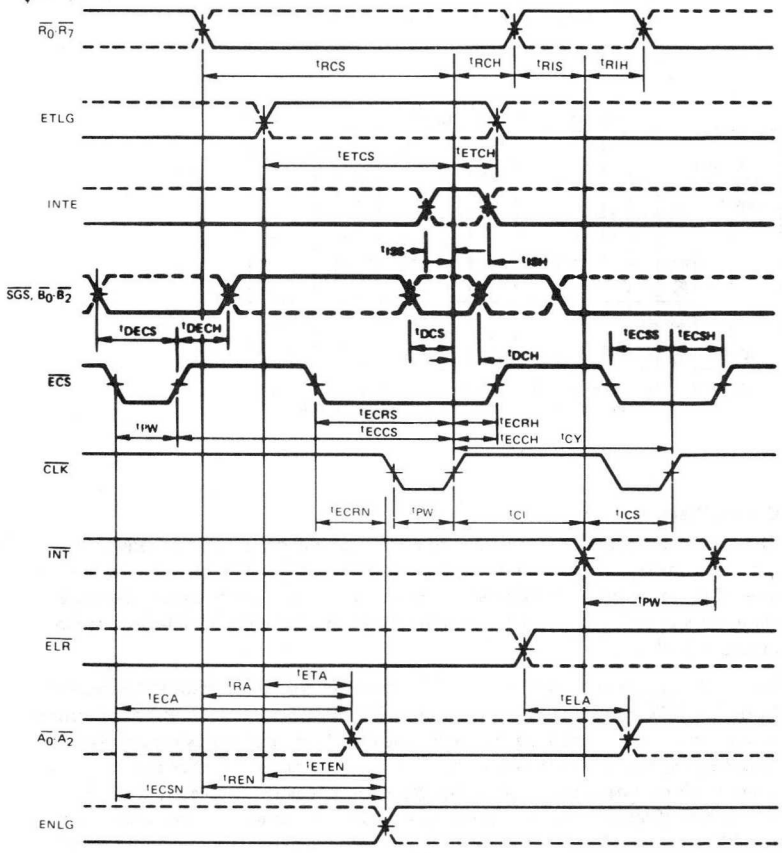
Priority Comparator

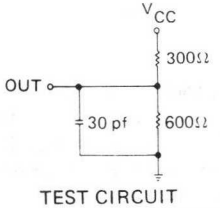
The priority comparator circuitry compares the level of the interrupt accepted by the priority encoder and request latch with the contents of the current status register. If the incoming request has a priority level higher than that of the current status register, the $\overline{INT}$ output is enabled. Note that this comparison can be disabled by loading the current status register with $\overline{SGS}$=0.

Expansion Control Signals

A microcomputer design may often require more than eight different interrupts. The μPB8214 is designed so that interrupt system expansion is easily performed via the use of three signals: ETLG (Enable This Level Group); ENLG (Enable Next Level Group); and $\overline{ELR}$ (Enable Level Read). A high input to ETLG indicates that the μPB8214 may accept an interrupt. In a typical system, the ENLG output from one μPB8214 is connected to the ETLG input of another μPB8214, etc. The ETLG of the μPB8214 with the highest priority is tied high. This configuration sets up priority among the cascaded μPB8214's. The ENLG output will be high for any device that does not have an interrupt pending, thereby allowing a device with lower priority to accept interrupts. The $\overline{ELR}$ input is basically a chip enable and allows hardware or software to selectively disable/enable individual μPB8214's. A low on the $\overline{ELR}$ input enables the device.

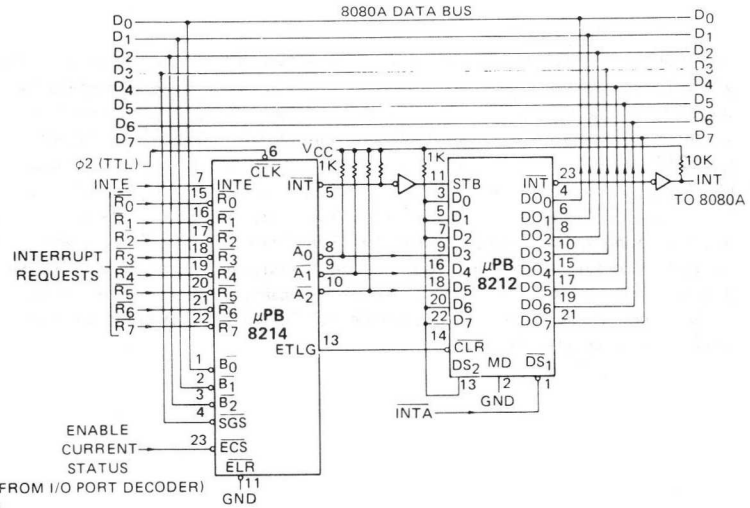
TIMING WAVEFORMS



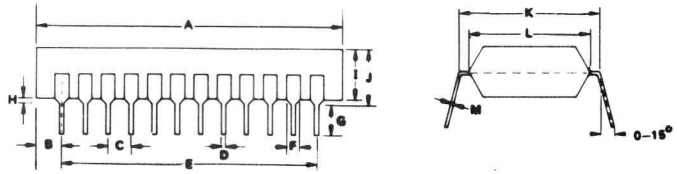


TEST CIRCUIT

TYPICAL μPB8214 CIRCUITRY



PACKAGE OUTLINE
μPB8214C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	33 MAX.	1.28
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	3.2 MIN.	0.125 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	0.25 ± 0.1	0.01 ± 0.004

9

NOTES

4 BIT PARALLEL BIDIRECTIONAL BUS DRIVER

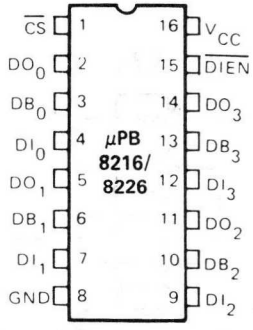
DESCRIPTION

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V (V_{OH}), and for high capacitance terminated bus structures, the DB outputs provide a high 55 mA (I_{OL}) capability.

FEATURES

- Data Bus Buffer Driver for μCOM-8 Microprocessor Family
- Low Input Load Current – 0.25 mA Maximum
- High Output Drive Capability for Driving System Data Bus
- 3.65V Output High Voltage for Direct Interface to μCOM-8 Microprocessor Family
- Three State Outputs
- Reduces System Package Count
- Available in 16 pin packages: Cerdip and Plastic

PIN CONFIGURATION



PIN NAMES

DB_0 DB_3	Data Bus Bi Directional
DI_0 DI_3	Data Input
DO_0 DO_3	Data Output
DIEN	Data in Enable Direction Control
CS	Chip Select

9

μPB8216/8226

FUNCTIONAL DESCRIPTION

Microprocessors like the μPD8080A are MOS devices and are generally capable of driving a single TTL load. This also applies to MOS memory devices. This type of drive is sufficient for small systems with a few components, but often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The μPD8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bi-Directional Driver

Each buffered line of the four bit driver consists of two separate buffers. They are three state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this is used to interface to the system side components such as memories, I/O, etc. Its interface is directly TTL compatible and it has high drive (55 mA). For maximum flexibility on the other side of the driver the inputs and outputs are separate. They can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080A Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080A processor is achieved with an adequate amount of noise immunity (650 mV worst case).

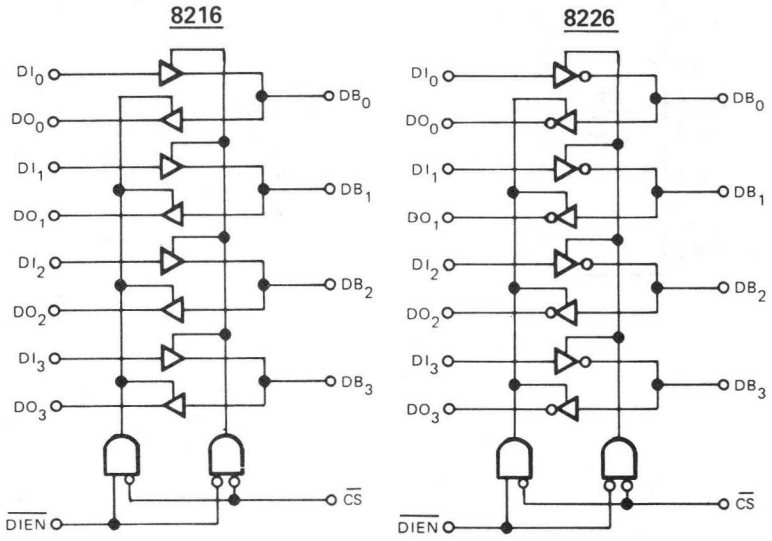
Control Gating $\overline{CS}$, $\overline{DIEN}$

The $\overline{CS}$ input is used for device selection. When $\overline{CS}$ is "high" the output drivers are all forced to their high-impedance state. When it is "low" the device is selected (enabled) and the data flow direction is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the data flow direction (see Block Diagrams for complete truth table). This directional control is accomplished by forcing one of the pair of buffers to its high impedance state. This allows the other to transmit its data. This is accomplished by a simple two gate circuit.

The μPB8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.

BLOCK DIAGRAMS



$\overline{DIEN}$	$\overline{CS}$	RESULT
0	0	DI → DB
1	0	DB → DO
0	1	High Impedance
1	1	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature (Cerdip) . . . . . −65°C to +150°C
(Plastic) . . . . . −65°C to +125°C
All Output and Supply Voltages . . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −1.3 to +5.5 Volts
Output Currents . . . . . 125 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ±5%

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current $\overline{DIEN}$, $\overline{CS}$		I_{F1}			−0.5	mA	V_F = 0.45
Input Load Current All Other Inputs		I_{F2}			−0.25	mA	V_F = 0.45
Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		I_{R1}			20	μA	V_R = 5.25V
Input Leakage Current DI Inputs		I_{R2}			10	μA	V_R = 5.25V
Input Forward Voltage Clamp		V_C			−1.0	V	I_C = −5 mA
Input "Low" Voltage		V_{IL}			0.95	V	
Input "High" Voltage		V_{IH}	2.0			V	
Output Leakage Current (3-State)	DO	I_O			20	μA	V_O = 0.45/5.25V
	DB	I_O			100		
Power Supply Current	8216	I_{CC}			130	mA	
	8226	I_{CC}			120	mA	
Output "Low" Voltage		V_{OL1}			0.48	V	DO Outputs I_{OL} = 15 mA DB Outputs I_{OL} = 25 mA
Output "Low" Voltage	8216	V_{OL2}			0.7	V	DB Outputs I_{OL} = 55 mA
	8226	V_{OL2}			0.7	V	DB Outputs I_{OH} = 50 mA
Output "High" Voltage		V_{OH1}	3.65			V	DO Outputs I_{OH} = −1 mA
Output "High" Voltage		V_{OH2}	2.4			V	DB Outputs I_{OH} = −10 mA
Output Short Circuit Current		I_{OS}	−15		−65	mA	DO Outputs V_O = 0V
		I_{OS}	−30		−120	mA	DB Outputs V_{CC} = 5.0V

Note: ① Typical values are for T_a = 25°C, V_{CC} = 5.0V.

CAPACITANCE ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			8	pF	V_{BIAS} = 2.5V V_{CC} = 5V T_a = 25°C f = 1 MHz
Output Capacitance	C_{OUT1}			10 ②	pF	
Output Capacitance	C_{OUT2}			18 ③	pF	

Notes: ① This parameter is periodically sampled and not 100% tested.
② DO Output.
③ DB Output.

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AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$

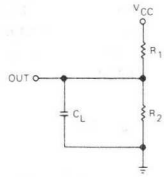
PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input to Output Delay DO Outputs		t_{PD1}			25	ns	C_L = 30 pF, R_1 = 300Ω, R_2 = 600Ω ④
Input to Output Delay	8216	t_{PD2}			30	ns	C_L = 300 pF, R_1 = 90Ω,
DB Outputs	8226	t_{PD2}			25	ns	R_2 = 180Ω 4
Output Enable Time	8216	t_E			65	ns	② ④
	8226	t_E			54	ns	
Output Disable Time		t_D			35	ns	③ ④

Notes: ① Typical values are for $T_a = 25°C$, $V_{CC} = 5.0V$

② DO Outputs, C_L = 30 pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ,
DB Outputs, C_L = 300 pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.

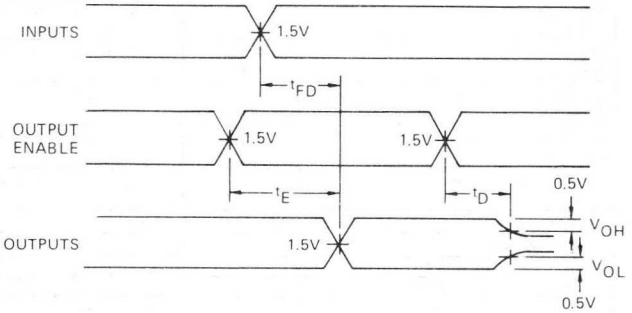
③ DO Outputs, C_L = 5 pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ,
DB Outputs, C_L = 5 pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.

④ Input pulse amplitude: 2.5V
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

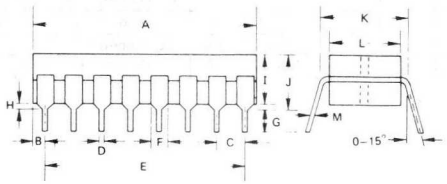


TEST CIRCUIT

TIMING WAVEFORMS

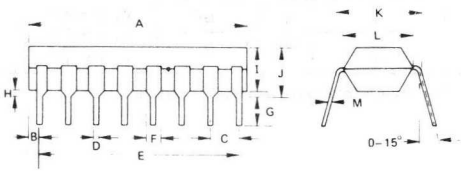


PACKAGE OUTLINE μPB8216C/D μPB8226C/D



Cerdip

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	$0.0098^{+0.0039}_{0.0019}$



Plastic

ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.05 MAX	0.16 MAX
J	4.55 MAX	0.18 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	0.01

CLOCK GENERATOR AND DRIVER FOR 8080A PROCESSORS

DESCRIPTION

The μPB8224 is a single chip clock generator and driver for 8080A processors. The clock frequency is determined by a user specified crystal and is capable of meeting the timing requirements of the entire 8080A family of processors. MOS and TTL level clock outputs are generated.

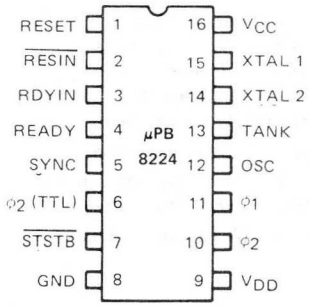
Additional logic circuitry of the μPB8224 provides signals for power-up reset, an advance status strobe and properly synchronizes the ready signal to the processor. This greatly reduces the number of chips needed for 8080A systems.

The μPB8224 is fabricated using NEC's Schottky bipolar process.

FEATURES

- Crystal Controlled Clocks
- Oscillator Output for External Timing
- MOS Level Clocks for 8080A Processor
- TTL Level Clock for DMA Activities
- Power-up Reset for 8080A Processor
- Ready Synchronization
- Advanced Status Strobe
- Reduces System Package Count
- Available in 16-pin Cerdip and Plastic Packages

PIN CONFIGURATION



PIN NAMES

RESIN	Reset Input
RESET	Reset Output
RDYIN	Ready Input
READY	Ready Output
SYNC	Sync Input
STSTB	Status STB Output
Φ1	Processor Clocks
Φ2	Processor Clocks
XTAL 1	Crystal Connections
XTAL 2	Crystal Connections
TANK	Used With Overtone Crystal
OSC	Oscillator Output
Φ2 (TTL)	Φ2 CLK (TTL Level)
VCC	+5V
VDD	+12V
GND	0V

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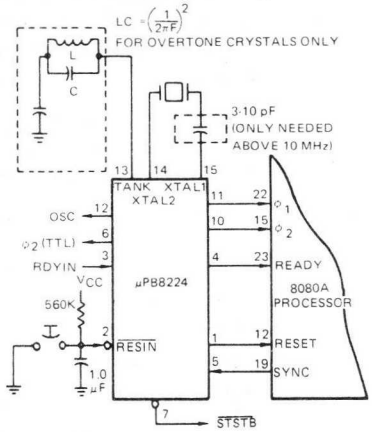
Clock Generator

The clock generator circuitry consists of a crystal controlled oscillator and a divide-by-nine counter. The crystal frequency is a function of the 8080A processor speed and is basically nine times the processor frequency, i.e.:

$$\text{Crystal frequency} = \frac{9}{t_{CY}}$$

where t_{CY} is the 8080A processor clock period.

A series resonant fundamental mode crystal is normally used and is connected across input pins XTAL1 and XTAL2. If an overtone mode crystal is used, an additional LC network, AC coupled to ground, must be connected to the TANK input of the μPB8224 as shown in the following figure.



The formula for the LC network is:

$$LC = \left(\frac{1}{2\pi F}\right)^2$$

where F is the desired frequency of oscillation.

The output of the oscillator is input to the divide-by-nine counter. It is also buffered and brought out on the OSC pin, allowing this stable, crystal controlled source to be used for derivation of other system timing signals. The divide-by-nine counter generates the two non-overlapping processor clocks, ϕ_1 and ϕ_2, which are buffered and at MOS levels, a TTL level ϕ_2 and internal timing signals.

The ϕ_1 and ϕ_2 high level outputs are generated in a 2-5-2 digital pattern, with ϕ_1 being high for two oscillator periods, ϕ_2 being high for five oscillator periods, and then neither being high for two oscillator periods. The TTL level ϕ_2,ϕ_2 (TTL), is normally used for DMA activities by gating the external device onto the 8080A bus once a Hold Acknowledge (HLDA) has been issued.

Additional Logic

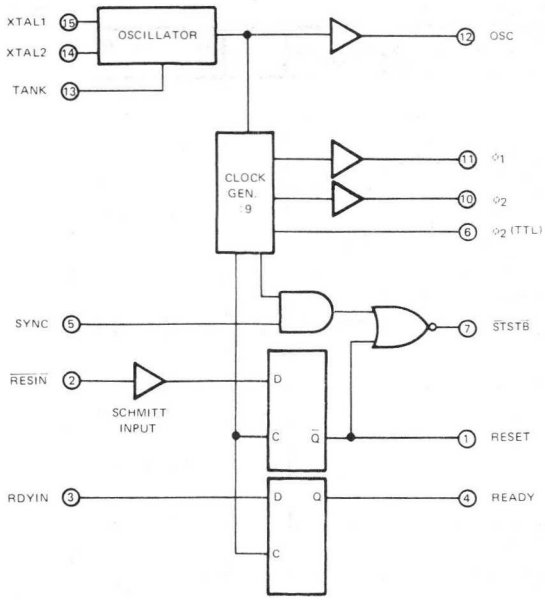
In addition to the clock generator circuitry, the μPB8224 contains additional logic to aid the system designer in the proper timing of several interface signals.

The $\overline{\text{STSTB}}$ signal indicates, at the earliest possible moment, when the status signals output from the 8080A processor are stable on the data bus. $\overline{\text{STSTB}}$ is designed to connect directly to the μPB8228 System Controller and automatically resets the μPB8228 during power-on Reset.

The $\overline{\text{RESIN}}$ input to the μPB8224 is used to automatically generate a RESET signal to the 8080A during power initialization. The slow rise of the power supply voltage in an external RC network is sensed by an internal Schmitt Trigger. The output of the Schmitt Trigger is gated to generate an 8080A compatible RESET. An active low manual switch may also be attached to the RC circuit for manual system reset.

The RDYIN input to the μPB8224 accepts an asynchronous "wait request" and generates a READY output to the 8080A that is fully synchronized to meet the 8080A timing requirements.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output Voltages (TTL)	−0.5 to +7 Volts
All Output Voltages (MOS)	−1.0 to +13.5 Volts
All Input Voltages	−1.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts
Supply Voltage V_{DD}	−0.5 to +13.5 Volts
Output Currents	100 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Current Loading	I_F			−0.25	mA	V_F = 0.45V
Input Leakage Current	I_R			10	μA	V_R = 5.25V
Input Forward Clamp Voltage	V_C			−1.0	V	I_C = −5 mA
Input "Low" Voltage	V_{IL}			0.8	V	V_{CC} = 5.0V
Input "High" Voltage	V_{IH}	2.6			V	Reset Input
		2.0				All Other Inputs
$\overline{RESIN}$ Input Hysteresis	V_{IH}-V_{IL}	0.25			V	V_{CC} = 5.0V
Output "Low" Voltage	V_{OL}			0.45	V	(Φ1, Φ2), Ready, Reset, $\overline{STSTB}$
						I_{OL} = 2.5 mA
				0.45	V	All Other Inputs
						I_{OL} = 15 mA
Output "High" Voltage	V_{OH}					
Φ1, Φ2		9.4			V	I_{OH} = −100 μA
READY, RESET		3.6			V	I_{OH} = −100 μA
All Other Outputs		2.4			V	I_{OH} = −1 mA
Output Short Circuit Current (All Low Voltage Outputs Only)	I_{SC} ①	−10		−60	mA	V_O = 0V; V_{CC} = 5.0V
Power Supply Current	I_{CC}			115	mA	
Power Supply Current	I_{DD}			15	mA	

Note: ① Caution, Φ1 and Φ2 output drivers do not have short circuit protection

CAPACITANCE①

T_a = 25°C; f = 1 MHz; V_{CC} = 5V; V_{DD} = 12V; V_{BIAS} = 2.5V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			8	pF	

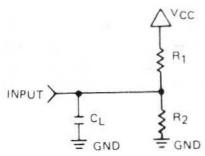
Note: ① This parameter is periodically sampled and not 100% tested.

T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

AC CHARACTERISTICS

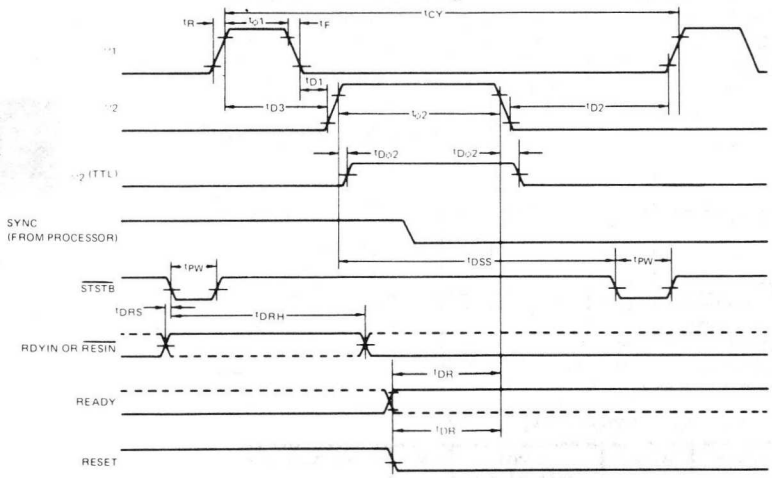
PARAMETER	SYMBOL	LIMITS ①			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
ϕ_1 Pulse Width	$t_{\phi 1}$	$\frac{2t_{CY}}{9}$ −20 ns			ns	C_L = 20 pF to 50 pF
ϕ_2 Pulse Width	$t_{\phi 2}$	$\frac{5t_{CY}}{9}$ −35 ns				
ϕ_1 to ϕ_2 Delay	t_{D1}	0				
ϕ_2 to ϕ_1 Delay	t_{D2}	$\frac{2t_{CY}}{9}$ −14 ns				
ϕ_1 to ϕ_2 Delay	t_{D3}	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ +20 ns		
ϕ_1 and ϕ_2 Rise Time	t_R			20		
ϕ_1 and ϕ_2 Fall Time	t_F			20		
ϕ_2 to ϕ_2 (TTL) Delay	$t_{D\phi 2}$	−5		+15	ns	ϕ_2 TTL, CL = 30 pF R_1 = 300Ω R_2 = 600Ω
ϕ_2 to $\overline{STSTB}$ Delay	t_{DSS}	$\frac{6t_{CY}}{9}$ −30 ns		$\frac{6t_{CY}}{9}$	ns	$\overline{STSTB}$, CL = 15 pF R_1 = 2K R_2 = 4K
$\overline{STSTB}$ Pulse Width	t_{PW}	$\frac{t_{CY}}{9}$ −15 ns			ns	
RDYIN Setup Time to $\overline{STSTB}$	t_{DRS}	50 ns − $\frac{4t_{CY}}{9}$				
RDYIN Hold Time After $\overline{STSB}$	t_{DRH}	$\frac{4t_{CY}}{9}$				
READY or RESET to ϕ_2 Delay	t_{DR}	$\frac{4t_{CY}}{9}$ −25 ns			ns	Ready and Reset CL = 10 pF R_1 = 2K R_2 = 4K
Crystal Frequency	f_{CLK}		$\frac{9}{t_{CY}}$		MHz	
Maximum Oscillating Frequency	f_{MAX}			27	MHz	

Note: ① t_{CY} represents the processor clock period



TEST CIRCUIT

TIMING WAVEFORMS



Voltage Measurement Points: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V.
All other signals measured at 1.5V.

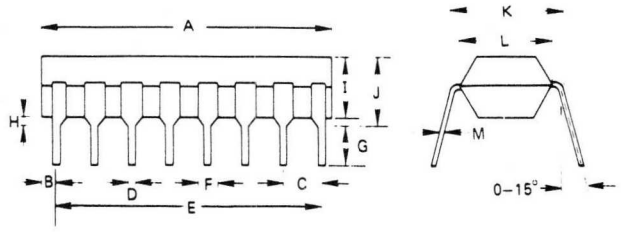
CRYSTAL REQUIREMENTS

Tolerance	0.005% at 0°C–70°C
Resonance	Series (Fundamental) ①
Load Capacitance	20-35 pF
Equivalent Resistance	75-20 ohms
Power Dissipation (Min)	4 mW

Note: ① With tank circuit use 3rd overtone mode.

PACKAGE OUTLINE

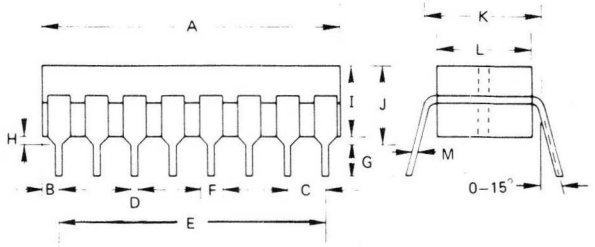
μPB8224C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.05 MAX	0.16 MAX
J	4.55 MAX	0.18 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

μPB8224D



(CERDIP)

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.8	0.27
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

9

8080A SYSTEM CONTROLLER AND BUS DRIVER

DESCRIPTION

The μPB8228/8238 is a single chip controller and bus driver for 8080A based systems. All the required interface signals necessary to connect RAM, ROM and I/O components to a μPD8080A are generated.

The μPB8228/8238 provides a bi-directional three-state bus driver for high TTL fan-out and isolation of the processor data bus from the system data bus for increased noise immunity.

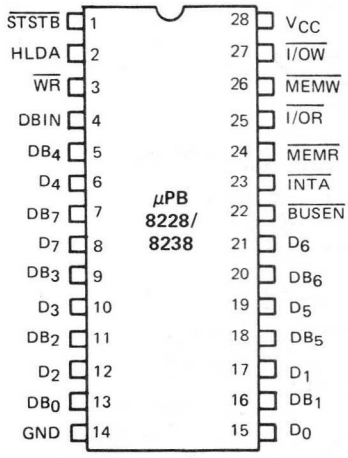
The system controller portion of the μPB8228/8238 consists of a status latch for definition of processor machine cycles and a gating array to decode this information for direct interface to system components. The controller can enable gating of a multi-byte interrupt onto the data bus or can automatically insert a RESTART 7 onto the data bus without any additional components.

Two devices are provided: the μPB8228 for small systems without tight write timing constraints and the μPB8238 for larger systems.

FEATURES

- System Controller for 8080A Systems
- Bi-Directional Data Bus for Processor Isolation
- 3.60V Output High Voltage for Direct Interface to 8080A Processor
- Three State Outputs on System Data Bus
- Enables Use of Multi-Byte Interrupt Instructions
- Generates RST 7 Interrupt Instruction
- μPB8228 for Small Memory Systems
- μPB8238 for Large Memory Systems
- Reduces System Package Count
- Schottky Bipolar Technology

PIN CONFIGURATION



NC: No Connection

PIN NAMES

$D_7 - D_0$	Data Bus (Processor Side)
$DB_7 - DB_0$	Data Bus (System Side)
$\overline{I/OR}$	I/O Read
$\overline{I/OW}$	I/O Write
$\overline{MEMR}$	Memory Read
$\overline{MEMW}$	Memory Write
DBIN	DBIN (From Processor)
$\overline{INTA}$	Interrupt Acknowledge
HLDA	HLDA (From Processor)
$\overline{WR}$	WR (From Processor)
$\overline{BUSEN}$	Bus Enable Input
$\overline{STSTB}$	Status Strobe (From μPB8224)
V_{CC}	+5V
GND	0 Volts

9

Rev/1

FUNCTIONAL DESCRIPTION

Bi-Directional Bus Driver

The eight bit, bi-directional bus driver provides buffering between the processor data bus and the system data bus. On the processor side, the μPB8228/8238 exceeds the minimum input voltage requirements (3.0V) of the μPD8080A. On the system side, the driver is capable of adequate drive current (10 mA) for connection of a large number of memory and I/O devices to the bus. Signal flow in the bus driver is controlled by the gating array and its outputs can be forced into a high impedance state by use of the $\overline{\text{BUSEN}}$ input.

Status Latch

The Status Latch in the μPB8228/8238 stores the status information placed on the data bus by the 8080A at the beginning of each machine cycle. The information is latched when $\overline{\text{STSTB}}$ goes low and is then decoded by the gating array for the generation of control signals.

Gating Array

The Gating Array generates "active low" control signals for direct interfacing to system components by gating the contents of the status latch with control signals from the 8080A.

$\overline{\text{MEM/R}}$, $\overline{\text{I/OR}}$ and $\overline{\text{INTA}}$ are generated by gating the DBIN signal from the processor with the contents of the status latch. $\overline{\text{I/OR}}$ is used to enable an I/O input onto the system data bus. $\overline{\text{MEM/R}}$ is used to enable a memory input.

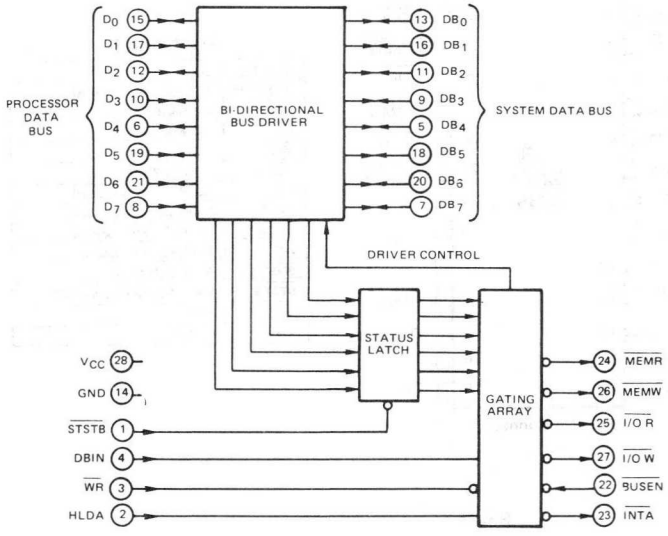
$\overline{\text{INTA}}$ is normally used to gate an interrupt instruction onto the system data bus. When used with the μPD8080A processor, the μPB8228/8238 will decode an interrupt acknowledge status word during all three machine cycles for a multi-byte interrupt instruction. For 8080A type processors that do not generate an interrupt acknowledge status word during the second and third machine cycles of a multi-byte interrupt instruction, the μPB8228/8238 will internally generate an $\overline{\text{INTA}}$ pulse for those machine cycles.

The μPB8228/8238 also provides the designer the ability to place a single interrupt instruction onto the bus without adding additional components. By connecting the +12 volt supply to the $\overline{\text{INTA}}$ output (pin 23) of the μPB8228/8238 through a 1 K ohm series resistor, RESTART 7 will be gated onto the processor data bus when DBIN is active during an interrupt acknowledge machine cycle.

$\overline{\text{MEM/W}}$ and $\overline{\text{I/OW}}$ are generated by gating the $\overline{\text{WR}}$ signal from the processor with the contents of the status latch. $\overline{\text{I/OW}}$ indicates that an output port write is about to occur. $\overline{\text{MEM/W}}$ indicates that a memory write will occur.

The data bus output buffers and control signal buffers can be asynchronously forced into a high impedance state by placing a high on the $\overline{\text{BUSEN}}$ pin of the μPB8228/8238. Normal operation is performed with $\overline{\text{BUSEN}}$ low.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.5 to 5.5 Volts
Output Currents	100 mA

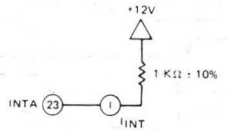
COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Clamp Voltage, All Inputs	V_C			−1.0	V	V_{CC} = 4.75V; I_{CC} = −5 mA
Input Load Current, $\overline{STSTB}$	I_F			500	μA	V_{CC} = 5.25V V_F = 0.45V
D_2 and D_6				750	μA	
D_0, D_1, D_4, D_5, and D_7				250	μA	
All Other Inputs				250	μA	
Input Leakage Current, $\overline{STSTB}$	I_R			100	μA	V_{CC} = 5.25V V_R = 5.0V
DB_0 through DB_7				20	μA	
All Other Inputs				100	μA	
Input Threshold Voltage, All Inputs	V_{TH}	0.8		2.0	V	V_{CC} = 5V
Power Supply Current	I_{CC}			190	mA	V_{CC} = 5.25V
Output Low Voltage, D_0 through D_7	V_{OL}			0.45	V	V_{CC} = 4.75V; I_{OL} = 2 mA
All Other Outputs				0.48	V	I_{OL} = 10 mA
Output High Voltage, D_0 through D_7	V_{OH}	3.6			V	V_{CC} = 4.75V; I_{OH} = −10 μA
All Other Outputs		2.4			V	I_{OH} = −1 mA
Short Circuit Current, All Outputs	I_{OS}	15		90	mA	V_{CC} = 5V
Off State Output Current, All Control Outputs	$I_{O(off)}$			100	μA	V_{CC} = 5.25V; V_O = 5.0V
				−100	μA	V_O = 0.45V
INTA Current	I_{INT}			5	mA	(See Figure below)



INTA TEST CIRCUIT

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			12	pF	V_{BIAS} = 2.5V,
Output Capacitance Control Signals	C_{OUT}			15	pF	V_{CC} = 5.0V,
I/O Capacitance (D or DB)	$C_{I/O}$			15	pF	f = 1 MHz

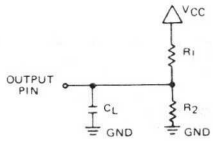
NOTE: This parameter is periodically sampled and not 100% tested.

AC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

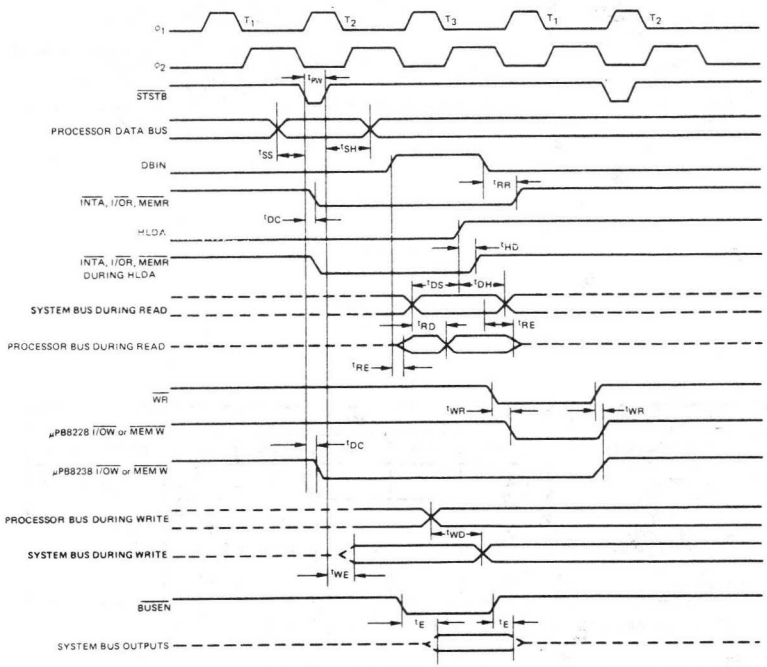
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Width of Status Strobe	t_{PW}	22			ns	
Setup Time, Status Inputs D_0-D_7	t_{SS}	8			ns	
Hold Time, Status Inputs D_0-D_7	t_{SH}	5			ns	
Delay from $\overline{STSTB}$ to any Control Signal	t_{DC}	20		60	ns	C_L = 100 pF
Delay from DBIN to Control Outputs	t_{RR}			30	ns	C_L = 100 pF
Delay from DBIN to Enable/ Disable 8080A Bus	t_{RE}			45	ns	C_L = 25 pF
Delay from System Bus to 8080A Bus during Read	t_{RD}			30	ns	C_L = 25 pF
Delay from $\overline{WR}$ to Control Outputs	t_{WR}	5		45	ns	C_L = 100 pF
Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$	t_{WE}			30	ns	C_L = 100 pF
Delay from 8080A Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	t_{WD}	5		40	ns	C_L = 100 pF
Delay from $\overline{System\ Bus\ Enable}$ to System Bus DB_0-DB_7	t_E			30	ns	C_L = 100 pF
HLDA to Read Status Outputs	t_{HD}			25	ns	
Setup Time, System Bus Inputs to HLDA	t_{DS}	10			ns	
Hold Time, System Bus Inputs to HLDA	t_{DH}	20			ns	C_L = 100 pF

For D_0-D_7: R_1 = 4 KΩ, R_2 = ∞Ω, C_L = 25 pF. For all other outputs: R_1 = 500Ω, R_2 = 1 KΩ, C_L = 100 pF.



TEST CIRCUIT

TIMING WAVEFORMS

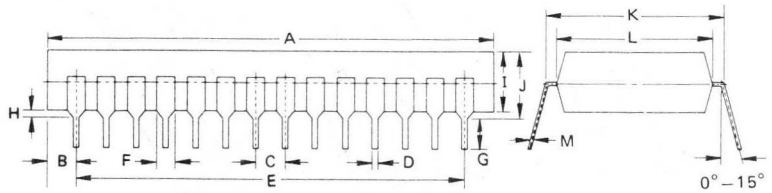


VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

STATUS WORD CHART

DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH	MEMORY READ	MEMORY WRITE	STACK READ	STACK WRITE	INPUT READ	OUTPUT WRITE	INTERRUPT ACKNOWLEDGE (M_1)	INT. ACK. (M_2, M_3)	HALT ACKNOWLEDGE	
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	
D_0	INTA	0	0	0	0	0	0	0	1	0	1	
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1	
D_2	STACK	0	0	0	1	1	0	0	0	0	0	
D_3	HLTA	0	0	0	0	0	0	0	0	1	1	
D_4	OUT	0	0	0	0	0	0	1	0	0	0	μPD8080A OUTPUT
D_5	M_1	1	0	0	0	0	0	0	1	0	1	
D_6	INP	0	0	0	0	0	1	0	0	0	0	
D_7	MEMR	1	1	0	1	0	0	0	0	1	0	
24	$\overline{MEMR}$	0	0	1	0	1	1	1	1	1	1	
26	$\overline{MEMW}$	1	1	0	1	0	1	1	1	1	1	μPB8228/8238 OUTPUT
25	$\overline{I/OR}$	1	1	1	1	1	0	1	1	1	1	
27	$\overline{I/OW}$	1	1	1	1	1	1	0	1	1	1	
23	$\overline{INTA}$	1	1	1	1	1	1	1	0	0	1	
PIN NO.		SIGNAL STATUS										
		μPB8228/8238 CONTROL SIGNALS										

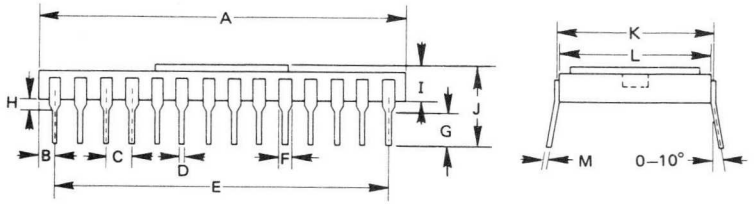
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PACKAGE OUTLINE
μPB8228C
μPB8238C

(Plastic)

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$



μPB8228D
μPB8238D

(Ceramic)

ITEM	MILLIMETERS	INCHES
A	36.2 MAX.	1.43
B	1.59 MAX.	0.06
C	2.54	0.1
D	0.46 ± 0.05	0.02 ± 0.004
E	33.02	1.3
F	1.02	0.04
G	3.2 MIN.	0.13
H	1.0	0.04
I	3.5	0.14
J	4.5	0.18
K	15.24	0.6
L	14.93	0.59
M	0.25 ± 0.05	0.01 ± 0.002

INPUT/OUTPUT EXPANDER FOR μPD8048/8748/8035

DESCRIPTION

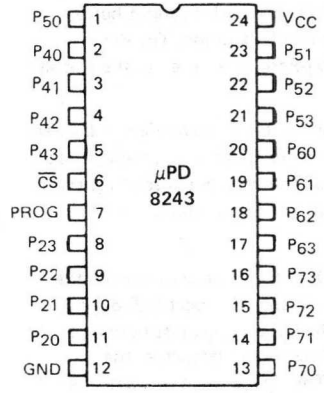
The μPD8243 input/output expander is directly compatible with the μPD8048 family of single-chip microcomputers. Using NMOS technology the μPD8243 provides high drive capabilities while requiring only a single +5V supply voltage.

The μPD8243 interfaces to the μPD8048 family through a 4-bit I/O port and offers four 4-bit bi-directional static I/O ports. The ease of expansion allows for multiple μPD8243's to be added using the bus port.

The bi-directional I/O ports of the μPD8243 act as an extension of the I/O capabilities of the μPD8048 microcomputer family. They are accessible with their own ANL, MOV, and ORL instructions.

FEATURES

- Four 4-Bit I/O Ports
- Fully Compatible with μPD8048 Microcomputer Family
- High Output Drive
- NMOS Technology
- Single +5V Supply
- Direct Extension of Resident μPD8048 I/O Ports
- Logical AND and OR Directly to Ports
- Compatible with Industry Standard 8243
- Available in a 24-Pin Plastic Package



FUNCTIONAL DESCRIPTION

General Operation

The I/O capabilities of the μPD8048/8748/8035 can be enhanced in four 4-bit I/O port increments using one or more μPD8243's. These additional I/O lines are addressed as ports 4-7. The following lists the operations which can be performed on ports 4-7.

- Logical AND Accumulator to Port.
- Logical OR Accumulator to Port.
- Transfer Port to Accumulator.
- Transfer Accumulator to Port.

Port 2 (P_{20}-P_{23}) forms the 4-bit bus through which the μPD8243 communicates with the host processor. The PROG output from the μPD8048/8748/8035 provides the necessary timing to the μPD8243. There are two 4-bit nibbles involved in each data transfer. The first nibble contains the op-code and port address followed by the second nibble containing the 4-bit data. Multiple μPD8243's can be used for additional I/O. The output lines from the μPD8048/8748/8035 can be used to form the chip selects for the additional μPD8243's.

Power On Initialization

Applying power to the μPD8243 sets ports 4-7 to the tri-state mode and port 2 to the input mode. The state of the PROG pin at power on may be either high or low. The PROG pin must make a high-to-low transition in order to exit from the power on mode. The power on sequence is initiated any time V_{CC} drops below 1V. The table below shows how the 4-bit nibbles on Port 2 correspond to the μPD8243 operations.

Port Address			Op-Code		
P_{21}	P_{20}	Address Code	P_{23}	P_{22}	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

For example an 0010 appearing on P_{20}-P_{23}, respectively, would result in a Write to Port 4.

Read Mode

There is one Read mode in the μPD8243. A falling edge on the PROG pin latches the op-code and port address from input Port 2. The port address and Read operation are then decoded causing the appropriate outputs to be tri-stated and the input buffers switched on. The rising edge of PROG terminates the Read operation. The Port (4,5,6, or 7) that was selected by the Port address (P_{21}-P_{20}) is returned to the tri-state mode, and Port 2 is switched to the input mode.

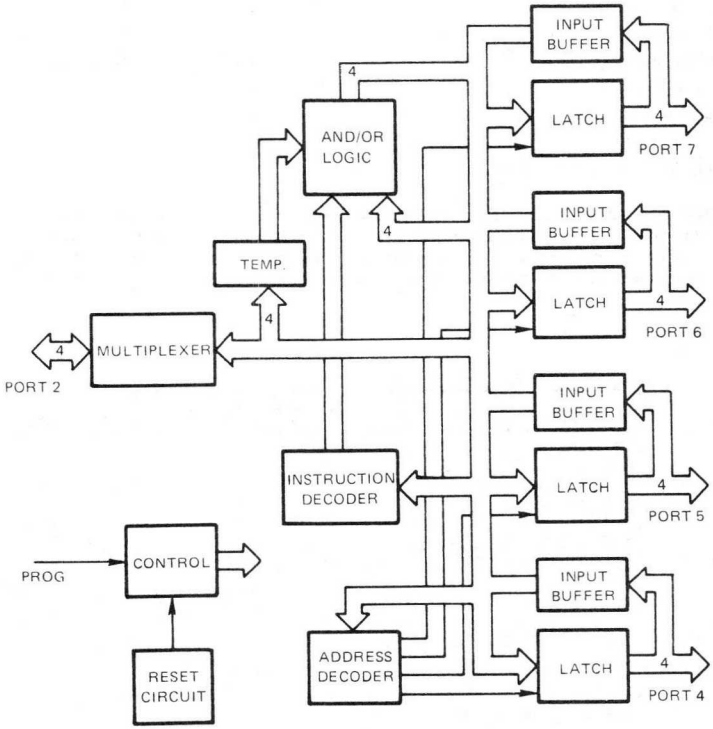
Generally, in the read mode, a port will be an input and in the write mode it will be an output. If during program operation, the μPD8243's modes are changed, the first read pulse immediately following a write should be ignored. The subsequent read signals are valid. Reading a port will then force that port to a high impedance state.

Write Modes

There are three write modes in the μPD8243. The MOVD P_p,A instruction from the μPD8048/8748/8035 writes the new data directly to the specified port (4,5,6, or 7). The old data previously latched at that port is lost. The ORLD Pp,A instruction performs a logical OR between the new data and the data currently latched at the selected port. The result is then latched at that port. The final write mode uses the ANLD Pp,A instruction. It performs a logical AND between the new data and the data currently latched at the specified port. The result is latched at that port.

The data remains latched at the selected port following the logical manipulation until new data is written to that port.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
2-5 1, 21-23 17-20 13-16	P_{40}-P_{43} P_{50}-P_{53} P_{60}-P_{63} P_{70}-P_{73}	The four 4-bit static bi-directional I/O ports. They are programmable into the following modes: input mode (during a Read operation); low impedance latched output mode (after a Write operation); and the tri-state mode (following a Read operation). Data appearing on I/O lines P_{20}-P_{23} can be written directly. That data can also be logically ANDed or ORed with the previous data on those lines.
6	$\overline{CS}$	Chip Select input (active-low). When the μPD8343 is deselected ($\overline{CS}$ = 1), output or internal status changes are inhibited.
7	PROG	Clock input pin. The control and address information are present on port lines P_{20}-P_{23} when PROG makes a high-to-low transition. Data is present on port lines P_{20}-P_{23} when PROG makes a low-to-high transition.
8-11	P_{20}-P_{23}	P_{20}-P_{23} form a 4-bit bi-directional port. Refer to PROG function for contents of P_{20}-P_{23} at the rising and falling edges of PROG. Data from a selected port is present on P_{20}-P_{23} prior to the rising edge of PROG if during a Read operation.
12	GND	The μPD8041/8741 ground potential.
24	V_{CC}	+5 volt supply.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	-65°C to +150°C
Storage Temperature (Plastic Package)	-65°C to +125°C
Voltage on Any Pin	- 0.5 to +7 Volts ①
Power Dissipation	1 W

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage (Ports 4-7)	V_{OL1}			0.45	V	I_{OL} = 5 mA ①
Output Low Voltage (Port 7)	V_{OL2}			1	V	I_{OL} = 20 mA
Output Low Voltage (Port 2)	V_{OL3}			0.45	V	I_{OL} = 0.6 mA
Output High Voltage (Ports 4-7)	V_{OH1}	2.4			V	I_{OH} = 240 μA
Output High Voltage (Port 2)	V_{OH2}	2.4			V	I_{OH} = 100 μA
Sum of All I_{OL} From 16 Outputs	I_{OL}			100	mA	5 mA Each Pin
Input Leakage Current (Ports 4-7)	I_{IL1}	-10		20	μA	V_{IN} = V_{CC} to 0V
Input Leakage Current (Port 2, $\overline{CS}$, PROG)	I_{IL2}	-10		10	μA	V_{IN} = V_{CC} to 0V
V_{CC} Supply Current	I_{CC}		10	20	mA	

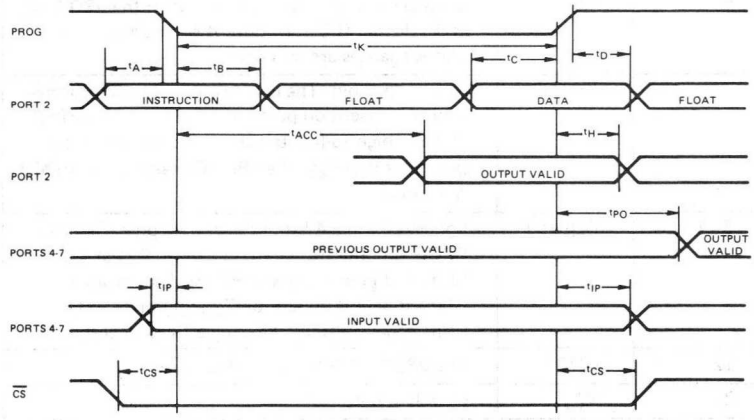
Note: ① Refer to graph of additional sink current drive.

AC CHARACTERISTICS

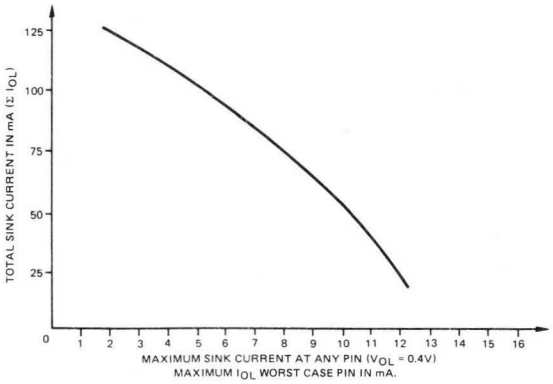
T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Code Valid Before PROG	t_A	100			ns	80 pF Load
Code Valid After PROG	t_B	60			ns	20 pF Load
Data Valid Before PROG	t_C	200			ns	80 pF Load
Data Valid After PROG	t_D	20			ns	20 pF Load
Port 2 Floating After PROG	t_H	0		150	ns	20 pF Load
PROG Negative Pulse Width	t_K	900			ns	
Ports 4-7 Valid After PROG	t_{PO}			700	ns	100 pF Load
Ports 4-7 Valid Before/After PROG	t_{LP1}	100			ns	
Port 2 Valid After PROG	t_{ACC}			750	ns	80 pF Load
$\overline{CS}$ Valid Before/After PROG	$t_{\overline{CS}}$	50			ns	

TIMING WAVEFORMS

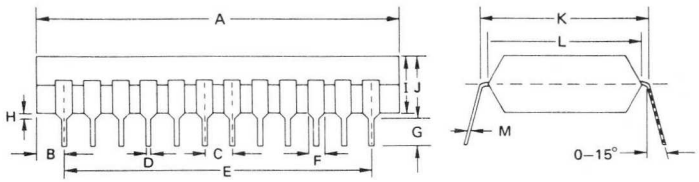


CURRENT SINKING CAPABILITY ①



Note: ① This curve plots the guaranteed worst case current sinking capability of any I/O port line versus the total sink current of all pins. The μPD8243 is capable of sinking 5 mA (for V_{OL} = 0.4V) through each of the 16 I/O lines simultaneously. The current sinking curve shows how the individual I/O line drive increases if all the I/O lines are not fully loaded.

PACKAGE OUTLINES μPD8243C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

9

NEC
μPD8251
μPD8251A

PROGRAMMABLE COMMUNICATION INTERFACES

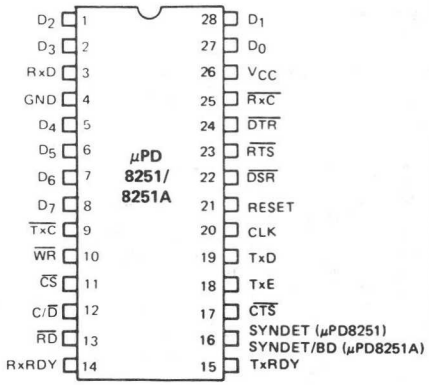
DESCRIPTION

The μPD8251 and μPD8251A Universal Synchronous/Asynchronous Receiver/Transmitters (USARTs) are designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the 8080A or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals such as TxE and SYNDET, is available to the processor at any time.

FEATURES

- Asynchronous or Synchronous Operation
  - Asynchronous:
    - Five 8-Bit Characters
    - Clock Rate – 1, 16 or 64 x Baud Rate
    - Break Character Generation
    - Select 1, 1-1/2, or 2 Stop Bits
    - False Start Bit Detector
    - Automatic Break Detect and Handling (μPD8251A)
  - Synchronous:
    - Five 8-Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
- Baud Rate (1X Mode) – DC to 56K Baud (μPD8251)
  – DC to 64K Baud (μPD8251A)
- Full Duplex, Double Buffered Transmitter and Receiver
- Parity, Overrun and Framing Flags
- Fully Compatible with 8080A/8085/μPD780 (Z80™)
- All Inputs and Outputs are TTL Compatible
- Single +5 Volt Supply, ±10%
- Separate Device Receive and Transmit TTL Clocks
- 28 Pin Plastic DIP Package
- N-Channel MOS Technology

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock (TTL)
TxD	Transmitter Data
RxC	Receiver Clock (TTL)
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
SYNDET/BD	Sync Detect/Break Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

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TM: Z80 is a registered trademark of Zilog.

Rev/4

μPD8251/8251A

FUNCTIONAL DESCRIPTION

The μPD8251 and μPD8251A Universal Synchronous/Asynchronous Receiver/Transmitters are designed specifically for 8080 microcomputer systems but work with most 8-bit processors. Operation of the μPD8251 and μPD8251A, like other I/O devices in the 8080 family, are programmed by system software for maximum flexibility.

In the receive mode, the μPD8251 or μPD8251A converts incoming serial format data into parallel data and makes certain format checks. In the transmit mode, it formats parallel data into serial form. The device also supplies or removes characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

μPD8251A FEATURES AND ENHANCEMENTS

The μPD8251A is an advanced design of the industry standard 8251 USART. It operates with a wide range of microprocessors, including the 8080, 8085, and μPD780 (Z80™). The additional features and enhancements of the μPD8251A over the μPD8251 are listed below.

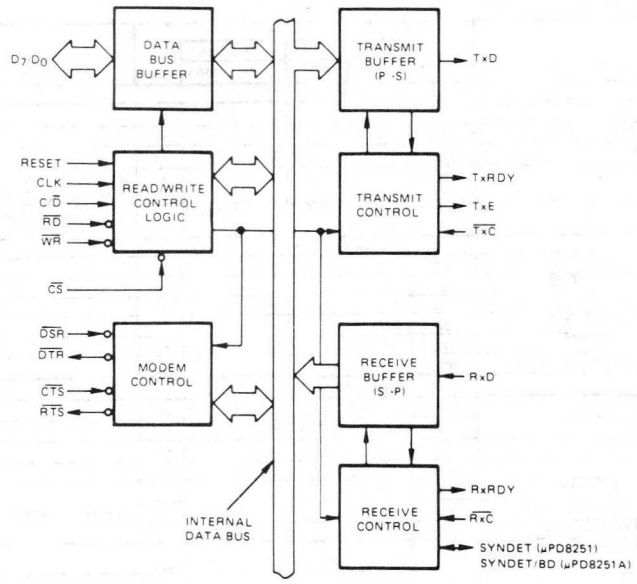
1. The data paths are double-buffered with separate I/O registers for control, status, Data In and Data Out. This feature simplifies control programming and minimizes processor overhead.
2. The Receiver detects and handles "break" automatically in asynchronous operations, which relieves the processor of this task.
3. The Receiver is prevented from starting when in "break" state by a refined Rx initialization. This also prevents a disconnected USART from causing unwanted interrupts.
4. When a transmission is concluded the TxD line will always return to the marking state unless SBRK is programmed.
5. The Tx Disable command is prevented from halting transmission by the Tx Enable Logic enhancement, until all data previously written has been transmitted. The same logic also prevents the transmitter from turning off in the middle of a word.
6. Internal Sync Detect is disabled when External Sync Detect is programmed. An External Sync Detect Status is provided through a flip-flop which clears itself upon a status read.
7. The possibility of a false sync detect is minimized by:
   - ensuring that if a double sync character is programmed, the characters be contiguously detected.
   - clearing the Rx register to all Logic 1s (V_{OH}) whenever the Enter Hunt command is issued in Sync mode.
8. The $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device as long as the μPD8251A is not selected.
9. The μPD8251A Status can be read at any time, however, the status update will be inhibited during status read.
10. The μPD8251A has enhanced AC and DC characteristics and is free from extraneous glitches, providing higher speed and improved operating margins.
11. Baud rate from DC to 64K.

BASIC OPERATION

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	μPD8251/μPD8251A → Data Bus
0	1	0	0	Data Bus → μPD8251/μPD8251A
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

TM: Z80 is a registered trademark of Zilog.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages	-0.5 to +7 Volts
All Input Voltages	-0.5 to +7 Volts
Supply Voltages	-0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 10%; GND = 0V.

PARAMETER	SYMBOL	LIMITS μPD8251 MIN	μPD8251 TYP	μPD8251 MAX	μPD8251A MIN	μPD8251A MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	0.5	0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	2.0	V_{CC}	V	
Output Low Voltage	V_{OL}			0.45		0.45	V	μPD8251: I_{OL} = 1.7 mA μPD8251A: I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			2.4		V	μPD8251: I_{OH} = -100 μA μPD8251A: I_{OH} = -400 μA
Data Bus Leakage	I_{DL}			-50		-10	μA	V_{OUT} = 0.45V
				10		10		V_{OUT} = V_{CC}
Input Load Current	I_{IL}			10		10	μA	At 5.5V
Power Supply Current	I_{CC}		45	80		100	mA	μPD8251A: All Outputs = Logic 1

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

AC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 10%; GND = 0V

PARAMETER	SYMBOL	LIMITS μPD8251 MIN	LIMITS μPD8251 MAX	LIMITS μPD8215A MIN	LIMITS μPD8215A MAX	UNIT	TEST CONDITIONS
READ							
Address Stable before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	t_{AR}	50		0		ns	
Address Hold Time for $\overline{READ}$ ($\overline{CS}$, $\overline{CD}$)	t_{RA}	5		0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	430		250		ns	
Data Delay from $\overline{READ}$	t_{RD}		350		200	ns	μPD8251: C_L = 100 pF μPD8251A: C_L = 150 pF
$\overline{READ}$ to Data Floating	t_{DF}	25	200	10	100	ns	μPD8251 C_L = 100 pF C_L = 15 pF
WRITE							
Address Stable before $\overline{WRITE}$	t_{AW}	20		0		ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20		0		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400		250		ns	
Data Set-Up Time for $\overline{WRITE}$	t_{DW}	200		150		ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40		0		ns	
Recovery Time Between WRITES ②	t_{RV}	6		6		t_{CY}	
OTHER TIMING							
Clock Period ③	t_{CY}	0.420	1.35	0.32	1.35	μs	
Clock Pulse Width High	$t_{\Phi W}$	220	0.7t_{CY}	120	t_{CY}-90	ns	
Clock Pulse Width Low	$t_{\Phi W}$			90		ns	
Clock Rise and Fall Time	$t_{R,tF}$	0	50	5	20	ns	
TxD Delay from Falling Edge of TxC	t_{DTx}		1		1	μs	
Rx Data Set-Up Time to Sampling Pulse	t_{SRx}	2		2		μs	μPD8251: C_L = 100 pF
Rx Data Hold Time to Sampling Pulse	t_{HRx}	2		2		μs	
Transmitter Input Clock Frequency 1X Baud Rate 16X Baud Rate 64X Baud Rate	f_{Tx}	DC DC DC	56 520 520		64 310 615	kHz kHz kHz	
Transmitter Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{TPW}	12 1		12 1		t_{CY} t_{CY}	
Transmitter Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{TPD}	15 3		15 3		t_{CY} t_{CY}	
Receiver Input Clock Frequency 1X Baud Rate 16X Baud Rate 64X Baud Rate	f_{Rx}	DC DC DC	56 520 520		64 310 615	kHz kHz kHz	
Receiver Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{RPW}	12 1		12 1		t_{CY} t_{CY}	
Receiver Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{RPD}	15 3		15 3		t_{CY} t_{CY}	
TxRDY Delay from Center of Data Bit	t_{Tx}		16		8	t_{CY}	μPD8251: C_L = 50 pF
RxRDY Delay from Center of Data Bit	t_{RX}		20		24	t_{CY}	
Internal SYNDET Delay from Center of Data Bit	t_{IS}		25		24	t_{CY}	
External SYNDET Set-Up Time before Falling Edge of $\overline{RxC}$	t_{ES}		16		16	t_{CY}	
TxEMPTY Delay from Center of Data Bit	t_{TxE}		16		20	t_{CY}	μPD8251: C_L = 50 pF
Control Delay from Rising Edge of WRITE (TxE, DTR, $\overline{RTS}$)	t_{WC}		16		8	t_{CY}	
Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)	t_{CR}		16		20	t_{CY}	

Notes: ① AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.

② This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.

③ The TxC and RxC frequencies have the following limitations with respect to CLK.
For 1X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
For 16X and 64X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$

④ Reset Pulse Width = 6 t_{CY} minimum.

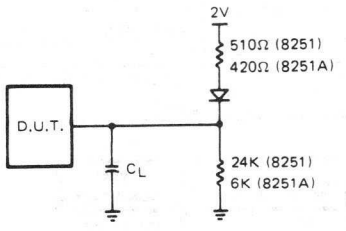
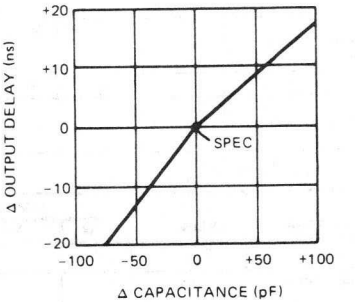
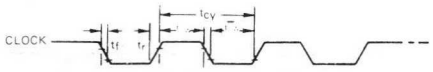


Figure 1. TEST LOAD CIRCUIT

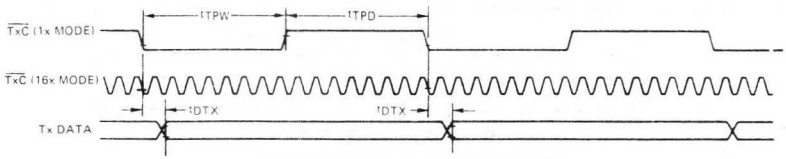


Typical Δ Output Delay Versus Δ Capacitance (pF)

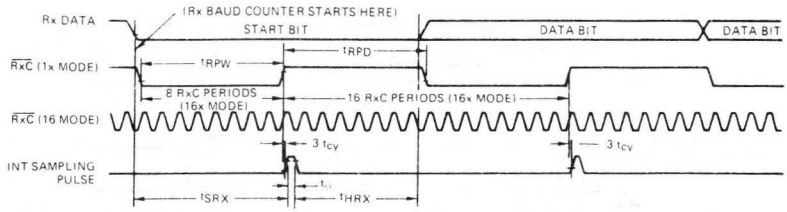
TIMING WAVEFORM



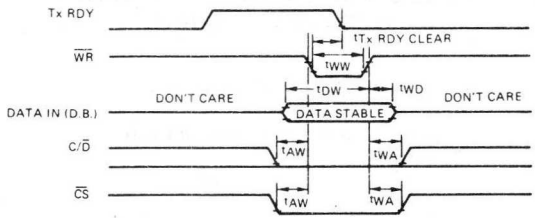
SYSTEM CLOCK INPUT



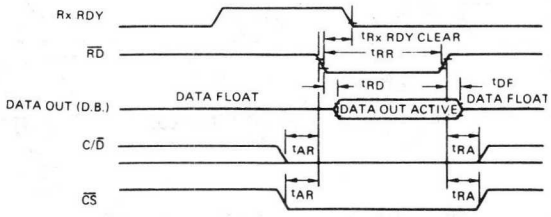
TRANSMITTER CLOCK AND DATA



RECEIVER CLOCK AND DATA



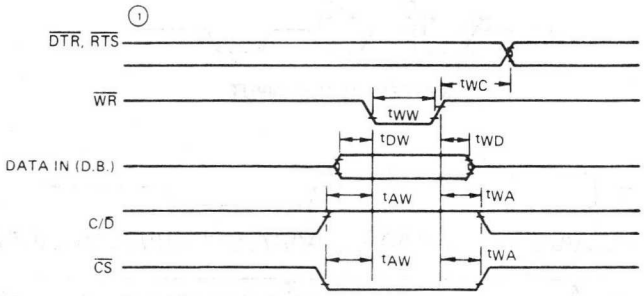
WRITE DATA CYCLE (PROCESSOR → USART)



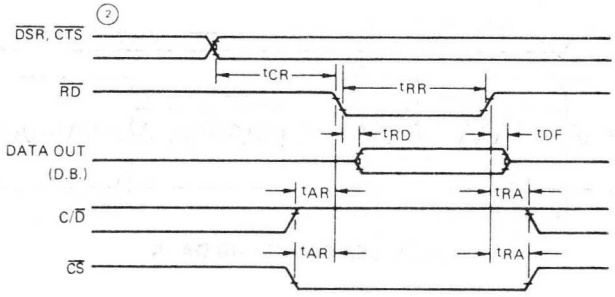
READ DATA CYCLE (PROCESSOR ← USART)

9

TIMING WAVEFORM
(CONT.)



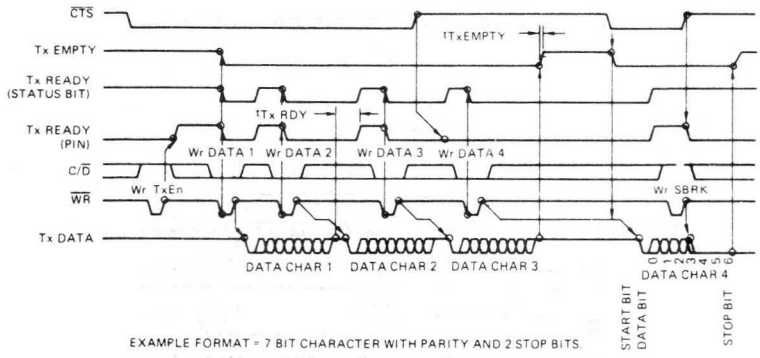
WRITE CONTROL OR OUTPUT PORT CYCLE
(PROCESSOR → USART)



READ CONTROL OR INPUT PORT CYCLE
(PROCESSOR ← USART)

NOTES: ① T_{WC} Includes the response timing of a control byte.

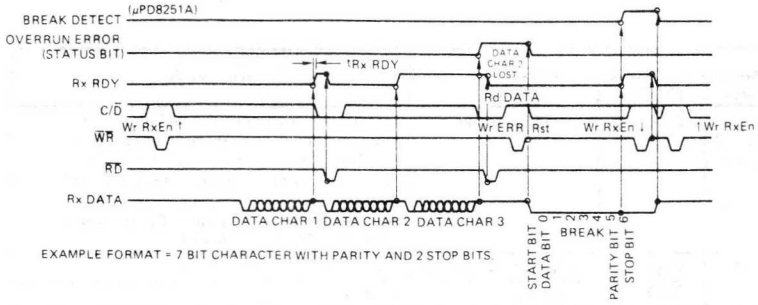
② T_{CR} Includes the effect of CTS on the TxENBL circuitry



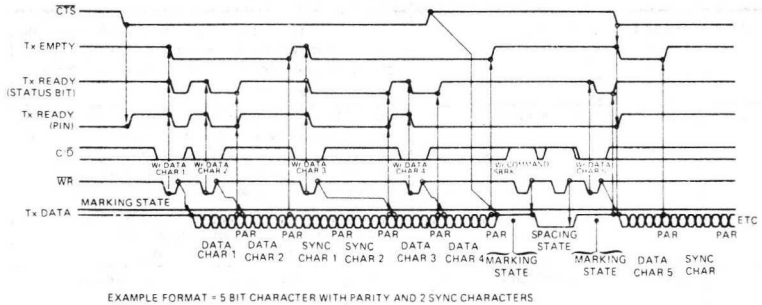
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY AND 2 STOP BITS.

TRANSMITTER CONTROL AND FLAG TIMING
(ASYNC MODE)

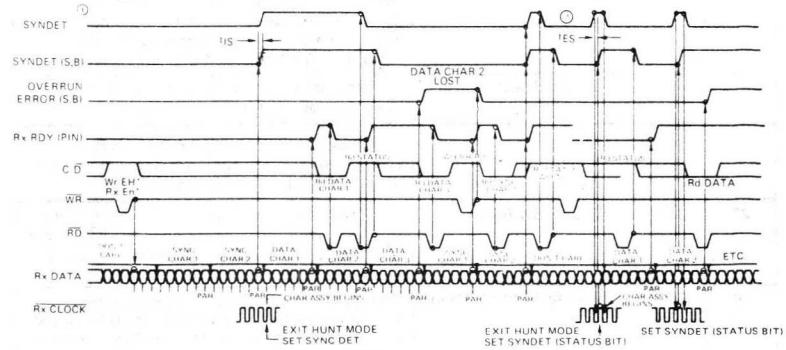
TIMING WAVEFORM
(CONT.)



RECEIVER CONTROL AND FLAG TIMING (ASYNC MODE)



TRANSMITTER CONTROL AND FLAG TIMING (SYNC MODE)



RECEIVER CONTROL AND FLAG TIMING (SYNC MODE)

Notes: ① Internal sync, 2 sync characters, 5 bits, with parity.
② External sync, 5 bits, with parity.

9

PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1, 2, 27, 28 5 – 8	$D_7 - D_0$	Data Bus Buffer	An 8-bit, 3-state bi-directional buffer used to interface the USART to the processor data bus. Data is transmitted or received by the buffer in response to input/output or Read/ Write instructions from the processor. The Data Bus Buffer also transfers Control words, Command words, and Status.
26	V_{CC}	V_{CC} Supply Voltage	+5 volt supply
4	GND	Ground	Ground
Read/Write Control Logic			This logic block accepts inputs from the processor Control Bus and generates control signals for overall USART operation. The Mode Instruction and Command Instruction registers that store the control formats for device functional definition are located in the Read/ Write Control Logic.
21	RESET	Reset	A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is 6 t_{CY}.
20	CLK	Clock Pulse	The CLK input provides for internal device timing and is usually connected to the Phase 2 (TTL) output of the μPB8224 Clock Generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be at least 30 times the Receiver or Transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.
10	$\overline{WR}$	Write Data	A "zero" on this input instructs the USART to accept the data or control word which the processor is writing out on the data bus.
13	$\overline{RD}$	Read Data	A "zero" on this input instructs the USART to place the data or status information onto the Data Bus for the processor to read.
12	$C/\overline{D}$	Control/Data	The Control/Data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the USART to accept or provide either a data character, control word or status information via the Data Bus. 0 = Data; 1 = Control.
11	$\overline{CS}$	Chip Select	A "zero" on this input enables the USART to read from or write to the processor.
Modem Control			The μPD8251 and μPD8251A have a set of control inputs and outputs which may be used to simplify the interface to a Modem.
22	$\overline{DSR}$	Data Set Ready	The Data Set Ready input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
24	$\overline{DTR}$	Data Terminal Ready	The Data Terminal Ready output can be controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
23	$\overline{RTS}$	Request to Send	The Request to Send output can be controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
17	$\overline{CTS}$	Clear to Send	A "zero" on the Clear to Send input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one).

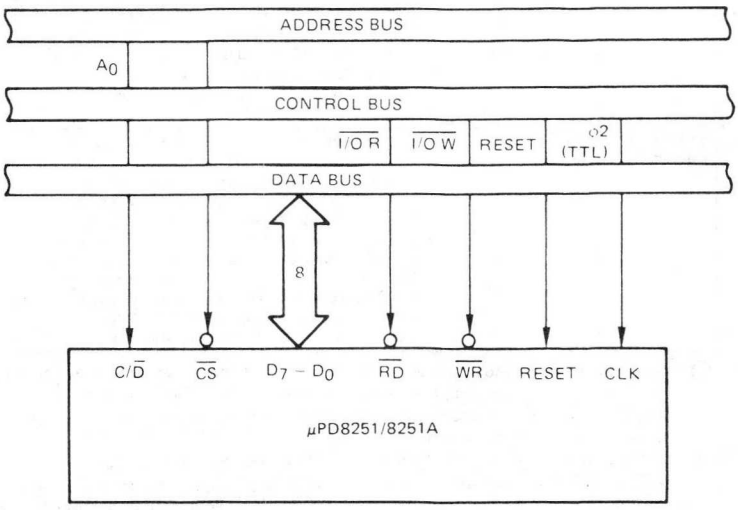
TRANSMIT BUFFER

The Transmit Buffer receives parallel data from the Data Bus Buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD pin.

PIN IDENTIFICATION (CONT.)

PIN			FUNCTION
NO.	SYMBOL	NAME	
Transmit Control Logic			The Transmit Control Logic accepts and outputs all external and internal signals necessary for serial data transmission.
15	TxRDY	Transmitter Ready	Transmitter Ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information for polled operation. Loading a character from the processor automatically resets TxRDY, on the leading edge.
18	TxE	Transmitter Empty	The Transmitter Empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a Sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.
9	$\overline{TxC}$	Transmitter Clock	The Transmitter Clock controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1x, 16x, or 64x the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
19	TxD	Transmitter Data	The Transmit Control Logic outputs the composite serial data stream on this pin.

μPD8251 AND μPD8251A INTERFACE TO 8080 STANDARD SYSTEM BUS



RECEIVE BUFFER

The Receive Buffer accepts serial data input at the $\overline{RxD}$ pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require less than eight bits, the μPD8251 and μPD8251A set the extra bits to "zero."

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Receiver Control Logic			This block manages all activities related to incoming data.
14	RxRDY	Receiver Ready	The Receiver Ready output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For Polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
25	$\overline{RxC}$	Receiver Clock	The Receiver Clock determines the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1.16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1x, 16x or 64x or Synchronous operation at 1x the Baud Rate. Unlike $\overline{TxC}$, data is sampled by the μPD8251 and μPD8251A on the rising edge of $\overline{RxC}$. ①
3	RxD	Receiver Data	A composite serial data stream is received by the Receiver Control Logic on this pin.
16	SYNDET (μPD8251)	Sync Detect	The SYNC Detect pin is only used in the Synchronous mode. The μPD8251 may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal Sync mode, the SYNDET output will go to a "one" when the μPD8251 has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251 to start assembling data character on the next falling edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the μPD8251 is in SYNC.
16	SYNDET/BD (μPD8251A)	Sync Detect/ Break Detect	The SYNDET/BD pin is used in both Synchronous and Asynchronous modes. When in SYNC mode the features for the SYNDET pin described above apply. When in Asynchronous mode, the Break Detect output will go high when an all zero word of the programmed length is received. This word consists of: start bit, data bit, parity bit and one stop bit. Reset only occurs when Rx data returns to a logic one state or upon chip reset. The state of Break Detect can be read as a status bit.

Note: ① Since the μPD8251 and μPD8251A will frequently be handling both the reception and transmission for a given link, the Receive and Transmit Baud Rates will be same. $\overline{RxC}$ and $\overline{TxC}$ then require the same frequency and may be tied together and connected to a single clock source or Baud Rate Generator.

Examples:

If the Baud Rate equals 110 (Async):
$\overline{RxC}$ or $\overline{TxC}$ equals 110 Hz (1x)
$\overline{RxC}$ or $\overline{TxC}$ equals 1.76 KHz (16x)
$\overline{RxC}$ or $\overline{TxC}$ equals 7.04 KHz (64x)

If the Baud Rate equals 300:
$\overline{RxC}$ or $\overline{TxC}$ equals 300 Hz (1x) A or S
$\overline{RxC}$ or $\overline{TxC}$ equals 4800 Hz (16x) A only
$\overline{RxC}$ or $\overline{TxC}$ equals 19.2 KHz (64x) A only

OPERATIONAL DESCRIPTION

A set of control words must be sent to the μPD8251 and μPD8251A to define the desired mode and communications format. The control words will specify the BAUD rate factor (1x, 16x, 64x), character length (5 to 8), number of STOP bits (1, 1-1/2, 2) Asynchronous or Synchronous mode, SYNDET (IN or OUT), parity, etc.

After receiving the control words, the μPD8251 and μPD8251A are ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251 and μPD8251A may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note: The μPD8251 and μPD8251A may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251 and μPD8251A cannot transmit until the TxEN (Transmitter Enable) bit has been set by a Command Instruction and until the $\overline{\text{CTS}}$ (Clear to Send) input is a "zero". TxD is held in the "marking" state after Reset awaiting new control words.

USART PROGRAMMING

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A RESET (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D}$ = 1) followed by a software reset command instruction (40 Hex) can be used to initialize the μPD8251 and μPD8251A.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

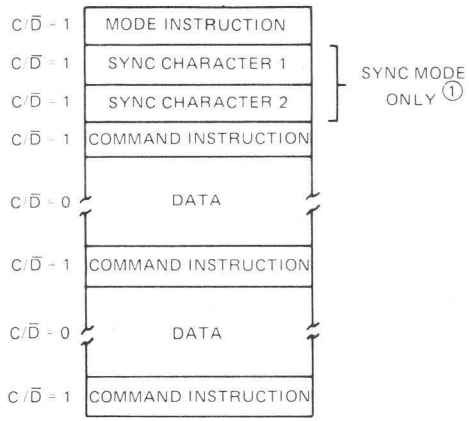
MODE INSTRUCTION

This control word specifies the general characteristics of the interface regarding the Synchronous or Asynchronous mode, BAUD rate factor, character length, parity, and number of stop bits. Once the Mode Instruction has been received, SYNC characters or Command Instructions may be inserted depending on the Mode Instruction content.

COMMAND INSTRUCTION

This control word will be interpreted as a SYNC character definition if immediately preceded by a Mode Instruction which specified a Synchronous format. After the SYNC character(s) are specified or after an Asynchronous Mode Instruction, all subsequent control words will be interpreted as an update to the Command Instruction. Command Instruction updates may occur at any time during the data block. To modify the Mode Instruction, a bit may be set in the Command Instruction which causes an internal Reset which allows a new Mode Instruction to be accepted.

TYPICAL DATA BLOCK



NOTE (1) The second SYNC character is skipped if MODE instruction has programmed the μPD8251 and μPD8251A to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the μPD8251 and μPD8251A to ASYNC mode.

MODE INSTRUCTION DEFINITION

The μPD8251 and μPD8251A can operate in either Asynchronous or Synchronous communication modes. Understanding how the Mode Instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components (one asynchronous and the other synchronous) which share the same support circuits and package. Although the format definition can be changed at will or "on the fly", the two modes will be explained separately for clarity.

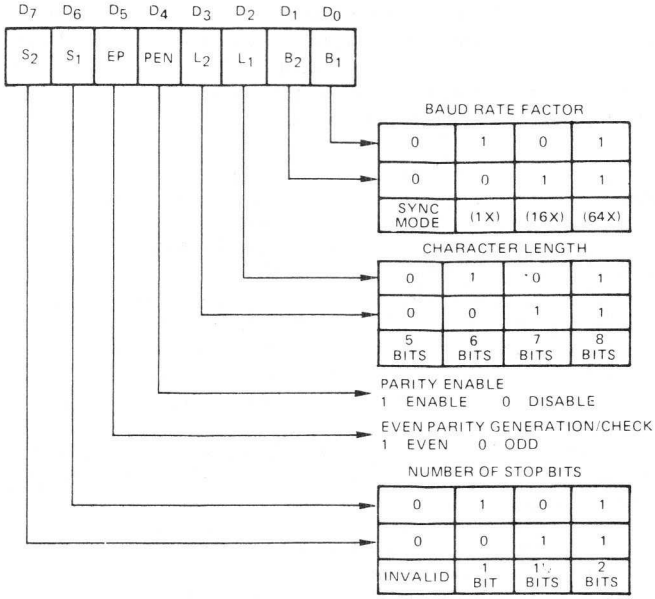
ASYNCHRONOUS TRANSMISSION

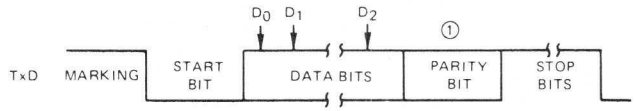
When a data character is written into the μPD8251 and μPD8251A, the USART automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bit(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at $\overline{TxC}$, $\overline{TxC}/16$ or $\overline{TxC}/64$, as defined by the Mode Instruction.

If no data characters have been loaded into the μPD8251 and μPD8251A, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

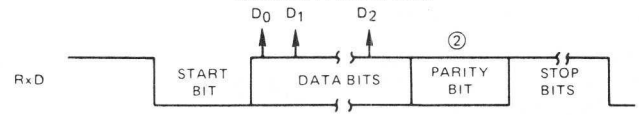
ASYNCHRONOUS RECEIVE

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a START bit and a new character. The START bit is checked by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid STOP bit, the input character is loaded into the parallel Data Bus Buffer of the μPD8251 and μPD8251A and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

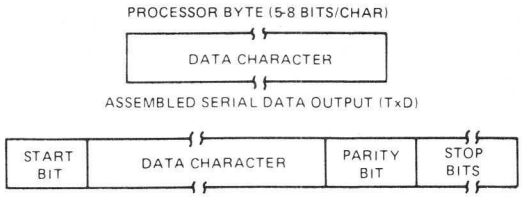




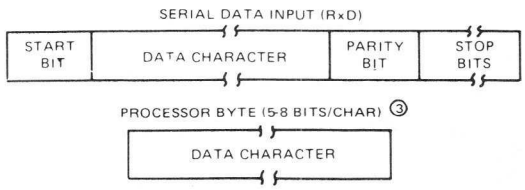
TRANSMITTER OUTPUT



RECEIVER INPUT



TRANSMISSION FORMAT



RECEIVE FORMAT

Notes: ① Generated by μPD8251/8251A
② Does not appear on the Data Bus.
③ If character length is defined as 5, 6, or 7 bits, the unused bits are set to "zero."

SYNCHRONOUS TRANSMISSION

As in Asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251 and μPD8251A receive the first character (usually a SYNC character) from the processor. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

Once transmission has started, Synchronous Mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251 and μPD8251A Transmit Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251 and μPD8251A become empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

SYNCHRONOUS RECEIVE

In Synchronous Receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the Enter HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

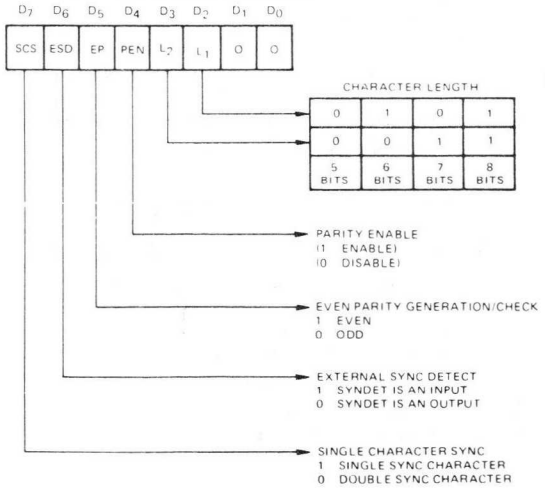
Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the Receive Buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251 and μPD8251A leave the HUNT mode and are in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

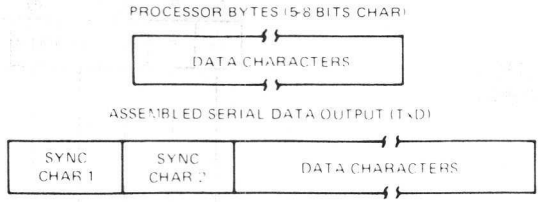
Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. If not in HUNT, parity will continue to be checked even if the receiver is not enabled. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost.

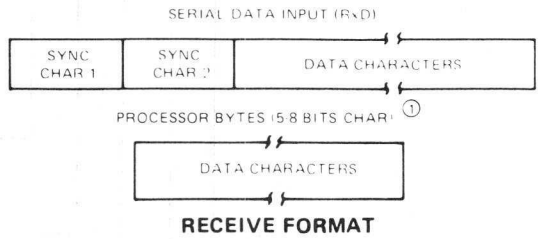
MODE INSTRUCTION FORMAT SYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

Note ① If character length is defined as 5, 6 or 7 bits, the unused bits are set to "zero."

COMMAND INSTRUCTION FORMAT

After the functional definition of the μPD8251 and μPD8251A has been specified by the Mode Instruction and the SYNC character(s) have been entered (if in SYNC mode), the USART is ready to receive Command Instructions and begin communication. A Command Instruction is used to control the specific operation of the format selected by the Mode Instruction. Enable Transmit, Enable Receive, Error Reset and Modem Controls are controlled by the Command Instruction.

After the Mode Instruction and the SYNC character(s) (as needed) are loaded, all subsequent "control writes" ($C/\overline{D} = 1$) will load or overwrite the Command Instruction register. A Reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251 and μPD8251A to interpret the next "control write", which must immediately follow the reset, as a Mode Instruction.

STATUS READ FORMAT

It is frequently necessary for the processor to examine the status of an active interface device to determine if errors have occurred or if there are other conditions which require a response from the processor. The μPD8251 and μPD8251A have features which allow the processor to read the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device Status Information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251 and μPD8251A to be used in both Polled and interrupt driven environments. Status update can have a maximum delay of 16 clock periods in the μPD8251 and 28 clock periods in the μPD8251A.

PARITY ERROR

When a parity error is detected, the PE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. PE being set does not inhibit USART operation.

OVERRUN ERROR

If the processor fails to read a data character before the one following is available, the OE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

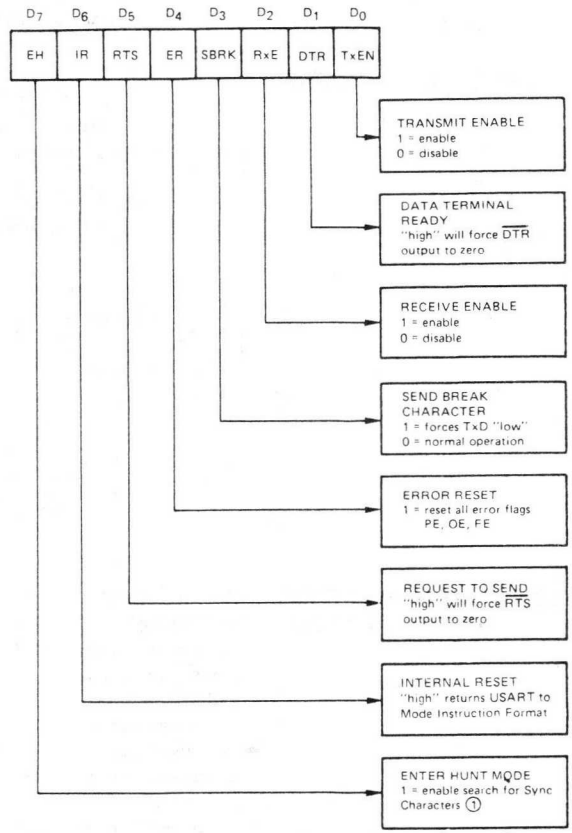
FRAMING ERROR ①

If a valid STOP bit is not detected at the end of a character, the FE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. FE being set does not inhibit USART operation.

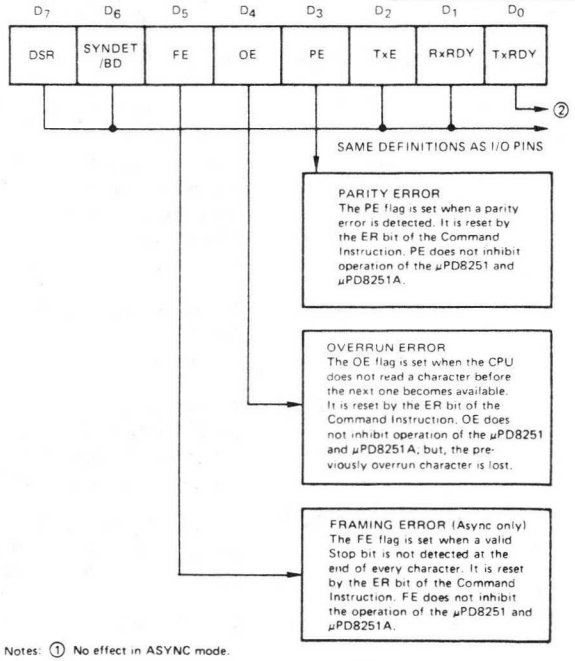
Note: ① ASYNC mode only.

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COMMAND INSTRUCTION FORMAT



STATUS READ FORMAT



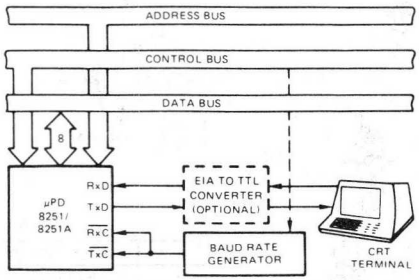
Notes: ① No effect in ASYNC mode.

② TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

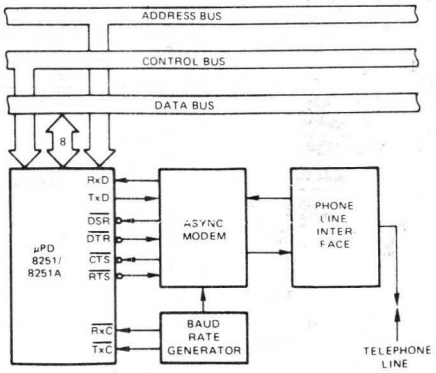
TxRDY status bit = DB Buffer Empty

TxRDY (pin 15) = DB Buffer Empty • $\overline{CTS}$ • TxEn

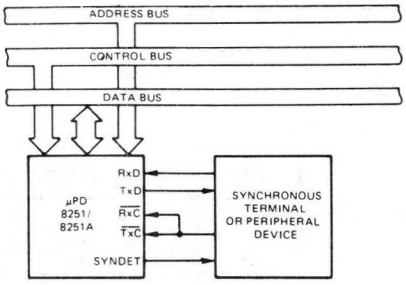
APPLICATION OF THE μPD8251 AND μPD8251A



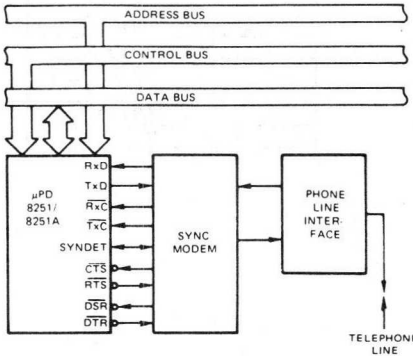
ASYNCHRONOUS SERIAL INTERFACE TO CRT TERMINAL, DC to 9600 BAUD



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES

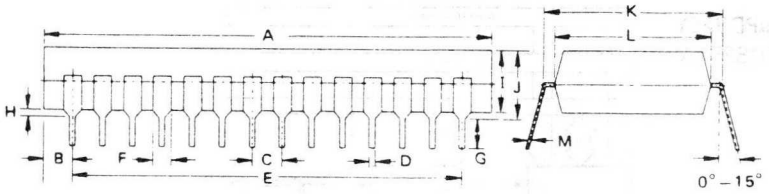


SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES

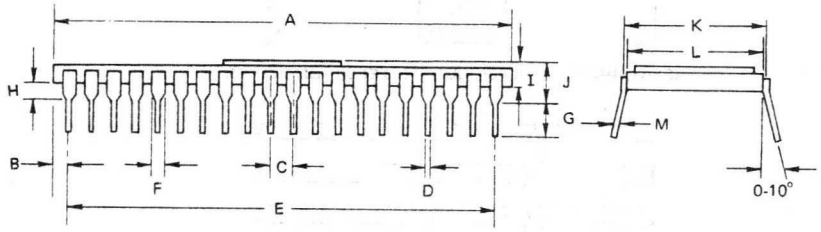
PACKAGE OUTLINES
μPD8251C
μPD8251AC



Plastic

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$

μPD8251D
μPD8251AD



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.03 MAX.
B	1.62 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.0019

PROGRAMMABLE INTERVAL TIMER

DESCRIPTION

The NEC μPD8253-5 contains three independent, programmable, multi-modal 16-bit counter/timers. It is designed as a general purpose device, fully compatible with the 8080 family. The μPD8253-5 interfaces directly to the busses of the processor as an array of I/O ports.

The μPD8253-5 can generate accurate time delays under the control of system software. The three independent 16-bit counters can be clocked at rates from DC to 4 MHz. The system software controls the loading and starting of the counters to provide accurate multiple time delays. The counter output flags the processor at the completion of the time-out cycles.

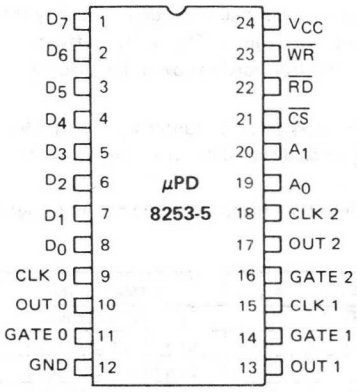
System overhead is greatly improved by relieving the software from the maintenance of timing loops. Some other common uses for the μPD8253-5 in microprocessor based systems are:

- Programmable Baud Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller
- NEC Now Supplies μPD8253-5 to all μPD8253 Requirements

FEATURES

- Three Independent 16-Bit Counters
- Clock Rate: DC to 4 MHz
- Count Binary or BCD
- Single +5 Volt Supply, ±10%
- 24 Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8-Bit)
CLK N	Counter Clock Inputs
GATE N	Counter Gate Inputs
OUT N	Counter Outputs
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Command or Data
$\overline{CS}$	Chip Select
A_0, A_1	Counter Select
V_{CC}	+5 Volts
GND	Ground

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Rev/4

FUNCTIONAL DESCRIPTION

Data Bus Buffer

The 3-state, 8-bit, bi-directional Data Bus Buffer interfaces the μPD8253-5 to the 8080AF/8085A microprocessor system. It will transmit or receive data in accordance with the INput or OUTput instructions executed by the processor. There are three basic functions of the Data Bus Buffer.

1. Program the modes of the μPD8253-5.
2. Load the count registers.
3. Read the count values.

Read/Write Logic

The Read/Write Logic controls the overall operation of the μPD8253-5 and is governed by inputs received from the processor system bus.

Control Word Register

Two bits from the address bus of the processor, A_0 and A_1, select the Control Word Register when both are at a logic "1" (active-high logic). When selected, the Control Word Register stores data from the Data Bus Buffer in a register. This data is then used to control:

1. The operational MODE of the counters.
2. The selection of BCD or Binary counting.
3. The loading of the count registers.

$\overline{RD}$ (Read)

This active-low signal instructs the μPD8253-5 to transmit the selected counter value to the processor.

$\overline{WR}$ (Write)

This active-low signal instructs the μPD8253-5 to receive MODE information or counter input data from the processor.

A_1, A_0

The A_1 and A_0 inputs are normally connected to the address bus of the processor. They control the one-of-three counter selection and address the control word register to select one of the six operational MODES.

$\overline{CS}$ (Chip Select)

The μPD8253-5 is enabled when an active-low signal is applied to this input. Reading or writing from this device is inhibited when the chip is disabled. The counter operation, however, is not affected.

Counters #0, #1, #2

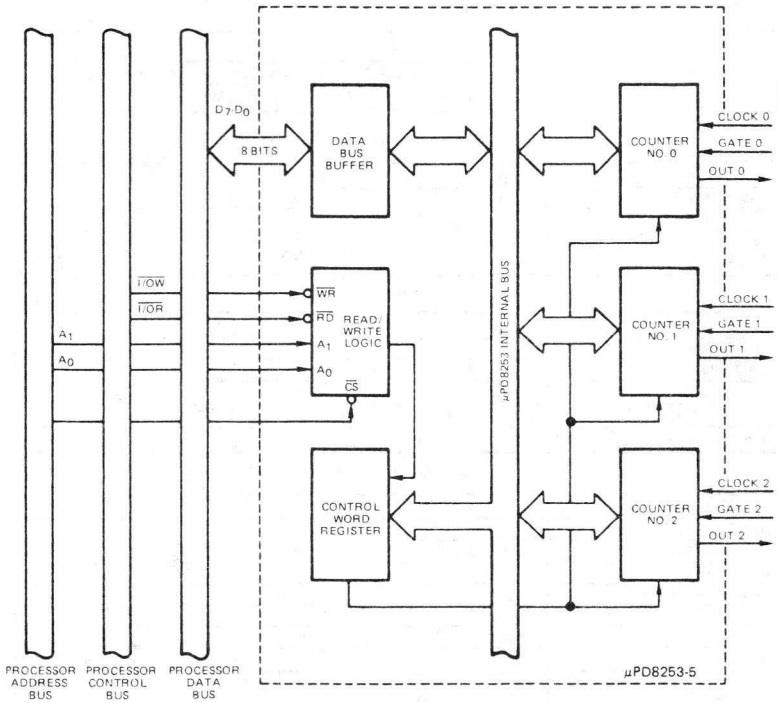
The three identical, 16-bit down counters are functionally independent allowing for separate MODE configuration and counting operation. They function as Binary or BCD counters with their gate, input and output line configuration determined by the operational MODE data stored in the Control Word Register. The system software overhead time can be reduced by allowing the control word to govern the loading of the count data.

The programmer, with READ operations, has access to each counter's contents. The μPD8253-5 contains the commands and logic to read each counter's contents while still counting without disturbing its operation.

The following is a table showing how the counters are manipulated by the input signals to the Read/Write Logic.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	FUNCTION
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation, 3-State
1	X	X	X	X	Disable, 3-State
0	1	1	X	X	No-Operation, 3-State

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
Voltage on Any Pin	−0.5 to +7 Volts (1)

Note: (1) With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device realiability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}+0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Input Load Current	I_{IL}			±10	μA	V_{IN} = V_{CC} to 0 V
Output Float Leakage Current	I_{OFL}			±10	μA	V_{OUT} = V_{CC} to 0 V
V_{CC} Supply Current	I_{CC}			140	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
Input/Output Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

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μPD8253-5

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%; GND = 0V

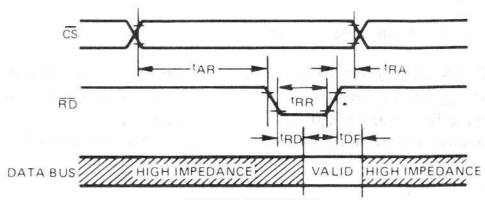
AC CHARACTERISTICS ①

PARAMETER	SYMBOL	② LIMITS μPD8253 MIN	TYP	MAX	② LIMITS μPD8253-5 MIN	TYP	MAX	UNIT	TEST CONDITIONS
READ									
Address Stable Before $\overline{READ}$	t_{AR}	50			0			ns	
Address Hold Time for $\overline{READ}$	t_{RA}	5			0			ns	
$\overline{READ}$ Pulse Width	t_{RR}	400			250			ns	
Data Delay from $\overline{READ}$	t_{RD}			300			170	ns	CL = 150 pF
$\overline{READ}$ to Data Floating	t_{DF}	25		125	25		100	ns	CL = 100 pF
WRITE									
Address Stable Before $\overline{WRITE}$	t_{AW}	20			0			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20			0			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400			250			ns	
Data Set Up Time for $\overline{WRITE}$	t_{DW}	200			150			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40			0			ns	
Recovery Time Between $\overline{WRITES}$	t_{RV}	1			1			μs	
CLOCK AND GATE TIMING									
Clock Period	t_{CLK}	300		DC	250		DC	ns	
High Pulse Width	t_{PWH}	200			160			ns	
Low Pulse Width	t_{PWL}	100			90			ns	
Gate Pulse Width High	t_{GW}	150			150			ns	
Gate Set Up Time to Clock ↑	t_{GS}	100			100			ns	
Gate Hold Time After Clock ↑	t_{GH}	50			50			ns	
Low Gate Width	t_{GL}	100			100			ns	
Output Delay from Clock ↓	t_{OD}			300			300	ns	CL = 100 pF
Output Delay from Gate	t_{ODG}			300			300	ns	CL = 100 pF

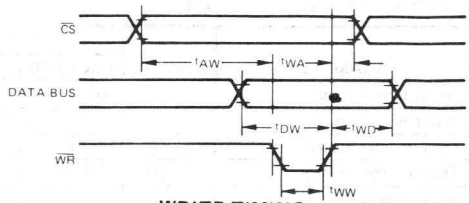
Notes: ① AC Timing Measured at V_{OH} = 2.2V; V_{OL} = 0.8V.

② Data for comparison only, NEC supplies μPD8253-5 only.

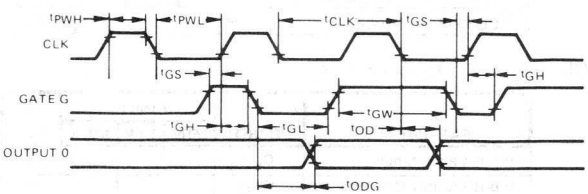
TIMING WAVEFORMS



READ TIMING



WRITE TIMING



CLOCK AND GATE TIMING

PROGRAMMING THE μPD8253-5

The programmer can select any of the six operational MODES for the counters using system software. Individual counter programming is accomplished by loading the CONTROL WORD REGISTER with the appropriate control word data (A_0, A_1 = 11).

CONTROL WORD FORMAT

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

SC – Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Invalid

RL – Read/Load

RL1	RL0	
0	0	Counter Latching Operation
1	0	Read/Load Most Significant Byte Only
0	1	Read/Load Least Significant Byte Only
1	1	Read/Load Least Significant Byte First, Then Most Significant Byte

BCD

0	Binary Counter, 16-Bits
1	BCD Counter, 4-Decades

M-Mode

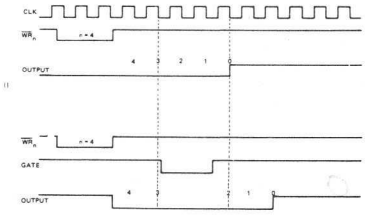
M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

OPERATIONAL MODES ①

Each of the three counters can be individually programmed with different operating MODES by appropriately formatted Control Words. The following is a summary of the MODE operations.

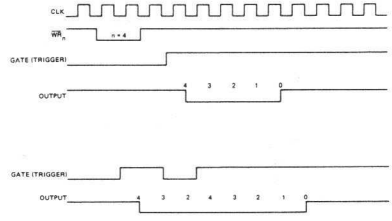
Mode 0: Interrupt on Terminal Count

The initial MODE set operation forces the OUTPUT low. When the specified counter is loaded with the count value, it will begin counting. The OUTPUT will remain low until the terminal count sets it high. It will remain in the high state until the trailing edge of the second $\overline{WR}$ pulse loads in COUNT data. If data is loaded during the counting process, the first $\overline{WR}$ stops the count. Counting starts with the new count data triggered by the falling clock edge after the second $\overline{WR}$. If a GATE pulse is asserted while counting, the count is terminated for the duration of GATE. The falling edge of CLK following the removal of GATE restarts counting from the terminated point.



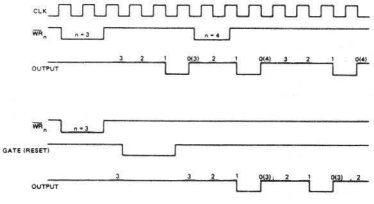
Mode 1: Programmable One-Shot

The OUTPUT is set low by the falling edge of CLOCK following the trailing edge of GATE. The OUTPUT is set high again at the terminal count. The output pulse is not affected if new count data is loaded while the OUTPUT is low. The new data will be loaded on the rising edge of the next trigger pulse. The assertion of a trigger pulse while OUTPUT is low, resets and retriggers the One-Shot. The OUTPUT will remain low for the full count value after the rising edge of TRIGGER.



Mode 2: Rate Generator

The RATE GENERATOR is a variable modulus counter. The OUTPUT goes low for one full CLOCK period as shown in following timing diagram. The count data sets the time between OUTPUT pulses. If the count register is reloaded between output pulses the present period will not be affected. The subsequent period will reflect the new value. The OUTPUT will remain high for the duration of the asserted GATE input. Normal operation resumes on the falling CLOCK edge following the rising edge of GATE.



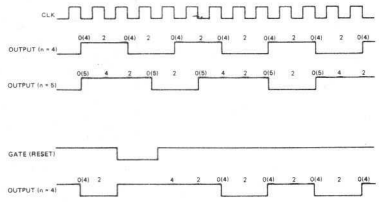
Note: ① All internal counter events occur at the falling edge of the associated clock in all modes of operation.

OPERATIONAL MODES (Cont.) ①

Mode 3: Square Wave Generator

MODE 3 resembles MODE 2 except the OUTPUT will be high for half of the count and low for the other half (for even values of data). For odd values of count data the OUTPUT will be high one clock cycle longer than when it is low (High Period → $\frac{N+1}{2}$ clock cycles; Low Period → $\frac{N-1}{2}$ clock periods, where N is the decimal value of count data). If the count register is reloaded with a new value during counting, the new value will be reflected immediately after the output transition of the current count.

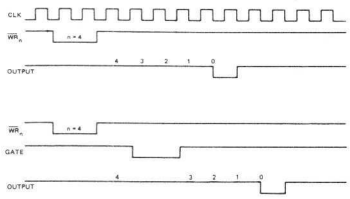
The OUTPUT will be held in the high state while GATE is asserted. Counting will start from the full count data after the GATE has been removed.



Mode 4: Software Triggered Strobe

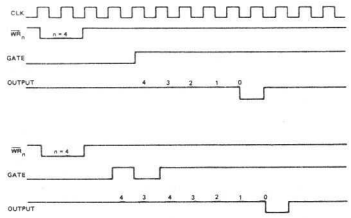
The OUTPUT goes high when MODE 4 is set, and counting begins after the second byte of data has been loaded. When the terminal count is reached, the OUTPUT will pulse low for one clock period. Changes in count data are reflected in the OUTPUT as soon as the new data has been loaded into the count registers. During the loading of new data, the OUTPUT is held high and counting is inhibited.

The OUTPUT is held high for the duration of GATE. The counters are reset and counting begins from the full data value after GATE is removed.



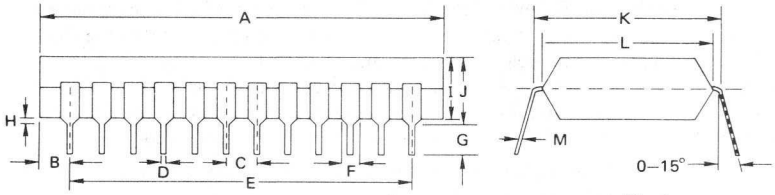
Mode 5: Hardware Triggered Strobe

Loading MODE 5 sets OUTPUT high. Counting begins when count data is loaded and GATE goes high. After terminal count is reached, the OUTPUT will pulse low for one clock period. Subsequent trigger pulses will restart the counting sequence with the OUTPUT pulsing low on terminal count following the last rising edge of the trigger input (Reference bottom half of timing diagram).



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PACKAGE OUTLINE
μPD8253C
μPD8253-5C



Plastic

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

PROGRAMMABLE PERIPHERAL INTERFACES

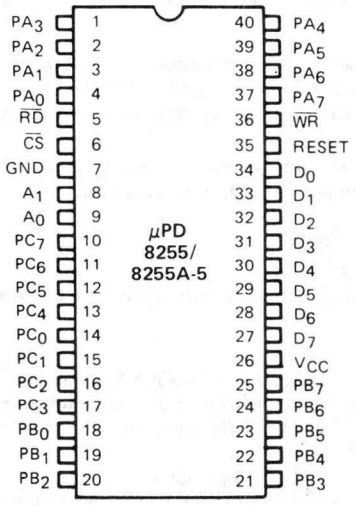
DESCRIPTION

The μPD8255 and μPD8255A-5 are general purpose programmable INPUT/OUTPUT devices designed for use with the 8080A/8085A microprocessors. Twenty-four (24) I/O lines may be programmed in two groups of twelve (group I and group II) and used in three modes of operation. In the Basic mode, (MODE 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In the Strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The Bidirectional Bus mode, (MODE 2), uses the 8 lines of Port A for a bidirectional bus, and five lines from Port C for bus control signals. The μPD8255 and μPD8255A-5 are packaged in 40 pin plastic dual-in-line packages.

FEATURES

- Fully Compatible with the 8080A/8085 Microprocessor Families
- All Inputs and Outputs TTL Compatible
- 24 Programmable I/O Pins
- Direct Bit SET/RESET Eases Control Application Interfaces
- 8 – 2 mA Darlington Drive Outputs for Printers and Displays (μPD8255)
- 8 – 4 mA Darlington Drive Outputs for Printers and Displays (μPD8255A-5)
- LSI Drastically Reduces System Package Count
- Standard 40 Pin Dual-In-Line Plastic and Ceramic Packages

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

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μPD8255/8255A-5

FUNCTIONAL DESCRIPTION

General

The μPD8255 and μPD8255A-5 Programmable Peripheral Interfaces (PPI) are designed for use in 8080A/8085A microprocessor systems. Peripheral equipment can be effectively and efficiently interfaced to the 8080A/8085A data and control busses with the μPD8255 and μPD8255A-5. The μPD8255 and μPD8255A-5 are functionally configured to be programmed by system software to avoid external logic for peripheral interfaces.

Data Bus Buffer

The 3-state, bidirectional, eight bit Data Bus Buffer (D_0-D_7) of the μPD8255 and μPD8255A-5 can be directly interfaced to the processor's system Data Bus (D_0-D_7). The Data Bus Buffer is controlled by execution of IN and OUT instructions by the processor. Control Words and Status information are also transmitted via the Data Bus Buffer.

Read/Write and Control Logic

This block manages all of the internal and external transfers of Data, Control and Status. Through this block, the processor Address and Control busses can control the peripheral interfaces.

Chip Select, $\overline{CS}$, pin 6

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 for communication with the 8080A/8085A.

Read, $\overline{RD}$, pin 5

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 to send Data or Status to the processor via the Data Bus Buffer.

Write, $\overline{WR}$, pin 36

A Logic Low, V_{IL}, on this input enables the Data Bus Buffer to receive Data or Control Words from the processor.

Port Select 0, A_0, pin 9
Port Select 1, A_1, pin 8

These two inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of three ports on the Control Word Register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor Address Bus.

Reset, pin 35

A Logic High, V_{IH}, on this input clears the Control Register and sets ports A, B, and C to the input mode. The input latches in ports A, B, and C are not cleared.

Group I and Group II Controls

Through an OUT instruction in System Software from the processor, a control word is transmitted to the μPD8255 and μPD8255A-5. Information such as "MODE," "Bit SET," and "Bit RESET" is used to initialize the functional configuration of each I/O port.

Each group (I and II) accepts "commands" from the Read/Write Control Logic and "control words" from the internal data bus and in turn controls its associated I/O ports.

Group I – Port A and upper Port C (PC_7-PC_4)
Group II – Port B and lower Port C (PC_3-PC_0)

While the Control Word Register can be written into, the contents cannot be read back to the processor.

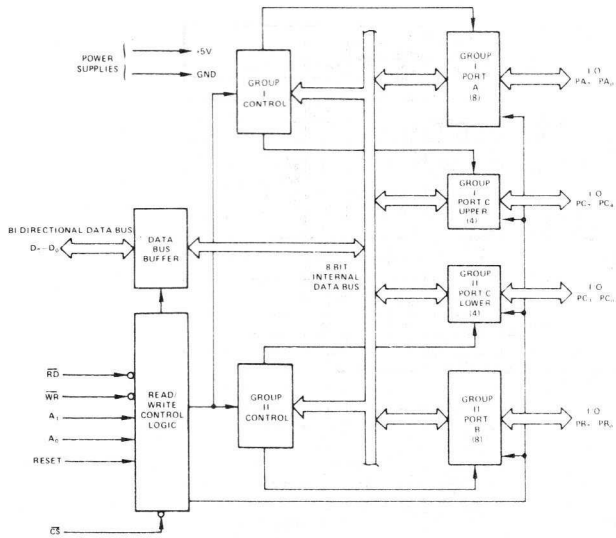
Ports A, B, and C

The three 8-bit I/O ports (A, B, and C) in the μPD8255 and μPD8255A-5 can all be configured to meet a wide variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255 and μPD8255A-5 is further enhanced by special features unique to each of the ports.

Port A = An 8-bit data output latch/buffer and data input latch.
Port B = An 8-bit data input/output latch/buffer and an 8-bit data input buffer.
Port C = An 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4-bit control and status ports for use with Ports A and B.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages ①	-0.5 to +7 Volts
All Input Voltages ①	-0.5 to +7 Volts
Supply Voltages ①	-0.5 to +7 Volts

Note: ① With respect to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS μPD8255 MIN	μPD8255 TYP	μPD8255 MAX	μPD8255A-5 MIN	μPD8255A-5 TYP	μPD8255A-5 MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	V_{SS}-0.5		0.8	-0.5		0.8	V	
Input High Voltage	V_{IH}	2		V_{CC}	2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4			0.45	V	②
Output High Voltage	V_{OH}	2.4			2.4			V	③
Darlington Drive Current	I_{OH} ①	1	2	4	-1		-4	mA	V_{OH} = 1.5V, R_{EXT} = 750Ω
Power Supply Current	I_{CC}		40	120			120	mA	V_{CC} = +5V, Output Open
Input Leakage Current	I_{LIH}			10			10	μA	V_{IN} = V_{CC}
Input Leakage Current	I_{LIL}			-10			-10	μA	V_{IN} = 0.4V
Output Leakage Current	I_{LOH}			10			±10	μA	V_{OUT} = V_{CC}, $\overline{CS}$ = 2.0V
Output Leakage Current	I_{LOL}			-10			-10	μA	V_{OUT} = 0.4V, $\overline{CS}$ = 2.0V

Notes: ① Any set of eight (8) outputs from either Port A, B, or C can source 2 mA into 1.5V for μPD8255, or 4 mA into 1.5V for μPD8255A-5.

② For μPD8255: I_{OL} = 1.7 mA
For μPD8255A-5: I_{OL} = 2.5 mA for DB Port; 1.7 mA for Peripheral Ports.

③ For μPD8255: I_{OH} = -100 μA for DB Port; 50 μs for Peripheral Ports.
For μPD8255A-5: I_{OH} = -400 μA for dB Port; -200 μs for Peripheral Ports.

CAPACITANCE

T_a = 25°C; V_{CC} = V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

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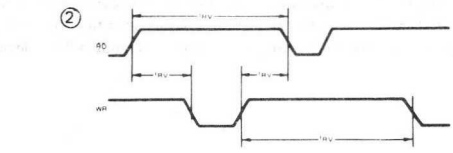
AC CHARACTERISTICS

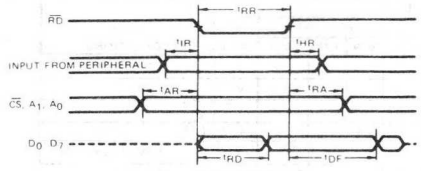
T_a = 0°C to +70°C; V_{CC} = +5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS μPD8255 MIN	LIMITS μPD8255 MAX	LIMITS μPD8255A-5 MIN	LIMITS μPD8255A-5 MAX	UNIT	TEST CONDITIONS
READ							
Address Stable Before $\overline{READ}$	t_{AR}	50		0		ns	
Address Stable After $\overline{READ}$	t_{RA}	0		0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	405		300		ns	
Data Valid From $\overline{READ}$	t_{RD}		295		200	ns	8255: C_L = 100 pF 8255A-5: C_L = 150 pF
Data Float After $\overline{READ}$	t_{DF}	10	150	10	100	ns ns	C_L = 100 pF C_L = 15 pF
Time Between $\overline{READ}$s and/or $\overline{WRITE}$s	t_{RV}	850		850		ns	②
WRITE							
Address Stable Before $\overline{WRITE}$	t_{AW}	20		0		ns	
Address Stable After $\overline{WRITE}$	t_{WA}	20		20		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400		300		ns	
Data Valid To $\overline{WRITE}$ (L.E.)	t_{DW}	10		100		ns	
Data Valid After $\overline{WRITE}$	t_{WD}	35		30		ns	
OTHER TIMING							
$\overline{WR}$ = 0 To Output	t_{WB}		500		350	ns	8255: C_L = 50 pF 8255A-5: C_L = 150 pF
Peripheral Data Before $\overline{RD}$	t_{IR}	0		0		ns	
Peripheral Data After $\overline{RD}$	t_{HR}	50		0		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	500		300		ns	
$\overline{STB}$ Pulse Width	t_{ST}	350		500		ns	
Per. Data Before T.E. Of $\overline{STB}$	t_{PS}	60		0		ns	
Per. Data After T.E. Of $\overline{STB}$	t_{PH}	150		180		ns	
$\overline{ACK}$ = 0 To Output	t_{AD}		400		300	ns	8255: C_L = 50 pF 8255A-5: C_L = 150 pF
$\overline{ACK}$ = 0 To Output Float	t_{KD}	20	300	20	250	ns	8255 { C_L = 50 pF C_L = 15 pF
$\overline{WR}$ = 1 To $\overline{OBF}$ = 0	t_{WOB}		300		650	ns	8255: C_L = 50 pF 8255A-5: C_L = 150 pF
$\overline{ACK}$ = 0 To $\overline{OBF}$ = 1	t_{AOB}		450		350	ns	
$\overline{STB}$ = 0 To IBF = 1	t_{SIB}		450		300	ns	
$\overline{RD}$ = 1 To IBF = 0	t_{RIB}		360		300	ns	
$\overline{RD}$ = 0 To INTR = 0	t_{RIT}		450		400	ns	
$\overline{STB}$ = 1 To INTR = 1	t_{SIT}		400		300	ns	
$\overline{ACK}$ = 1 To INTR = 1	t_{AIT}		400		350	ns	
$\overline{WR}$ = 0 To INTR = 0	t_{WIT}		850		850	ns	

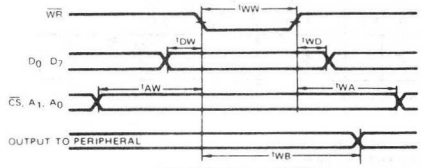
Notes: ① Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.

TIMING WAVEFORMS
MODE 0

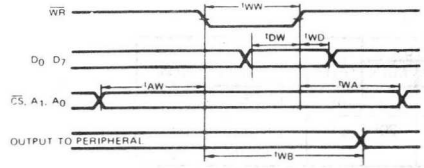




BASIC INPUT



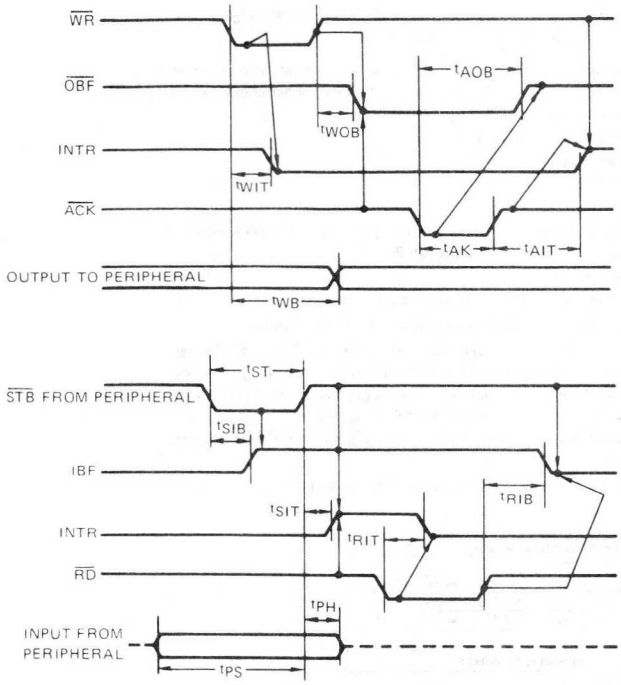
BASIC OUTPUT – μPD8255



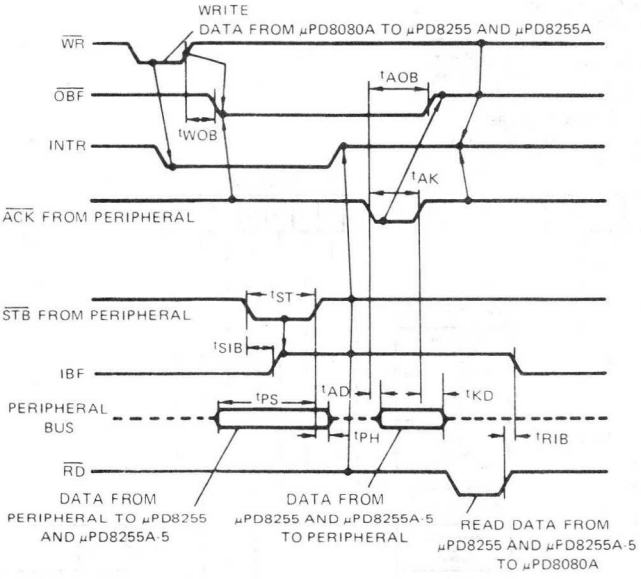
BASIC OUTPUT – μPD8255A-5

TIMING WAVEFORMS (CONT.)

MODE 1



MODE 2



Note: ① Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · MASK · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · MASK · $\overline{ACK}$ · $\overline{WR}$)

② When the μPD8255A-5 is set to Mode 1 or 2, $\overline{OBF}$ is reset to be high (logic 1).

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μPD8255/8255A-5

MODES

The μPD8255 and μPD8255A-5 can be operated in modes (0, 1 or 2) which are selected by appropriate control words and are detailed below.

MODE 0

- MODE 0 provides for basic Input and Output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed.

  16 different configurations in MODE 0

  Two 8-bit ports and two 4-bit ports

  Inputs are not latched

  Outputs are latched

MODE 1

MODE 1 provides for Strobed Input and Output operations with data transferred through Port A or B and handshaking through Port C.

Two I/O Groups (I and II)

Both groups contain an 8-bit data port and a 4-bit control/data port

Both 8-bit data ports can be either Latched Input or Latched Output

MODE 2

MODE 2 provides for Strobed bidirectional operation using PA_{0-7} as the bidirectional latched data bus. PC_{3-7} is used for interrupts and "handshaking" bus flow controls similar to Mode 1. Note that PB_{0-7} and PC_{0-2} may be defined as Mode 0 or 1, input or output in conjunction with Port A in Mode 2.

An 8-bit latched bidirectional bus port (PA_{0-7}) and a 5-bit control port (PC_{3-7})

Both inputs and outputs are latched

An additional 8-bit input or output port with a 3-bit control port

BASIC OPERATION

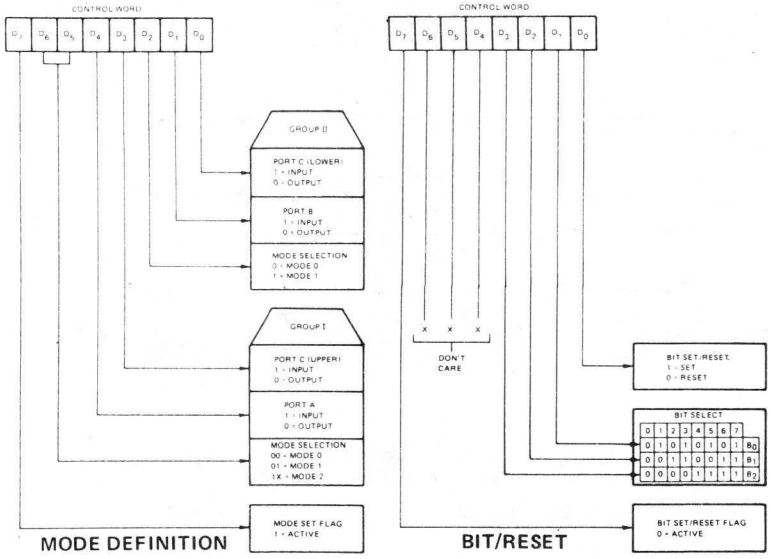
INPUT OPERATION (READ)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

OUTPUT OPERATION (WRITE)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

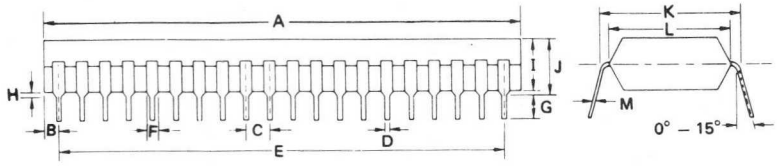
DISABLE FUNCTION					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

NOTES: ① X means "DO NOT CARE."
② All conditions not listed are illegal and should be avoided.

FORMATS

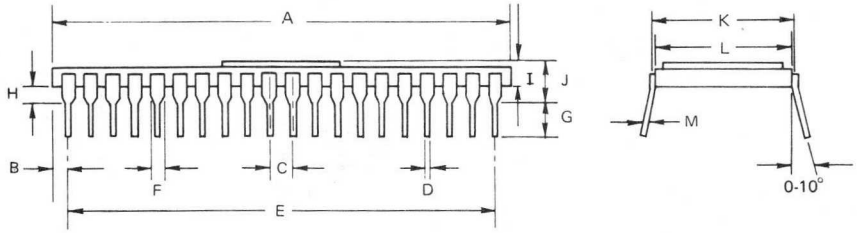


PACKAGE OUTLINE
μPD8255C
μPD8255AC/D-5



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{0.05}$	$0.010^{+0.004}_{0.002}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.03 MAX.
B	1.62 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.0019

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NOTES

PROGRAMMABLE DMA CONTROLLER

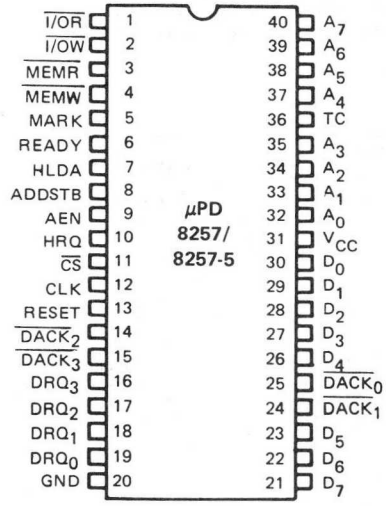
DESCRIPTION

The μPD8257-5 is a programmable four-channel Direct Memory Access (DMA) controller. It is designed to simplify high speed transfers between peripheral devices and memories. Upon a peripheral request, the μPD8257-5 generates a sequential memory address, thus allowing the peripheral to read or write data directly to or from memory. Peripheral requests are prioritized within the μPD8257-5 so that the system bus may be acquired by the generation of a single HOLD command to the 8080A. DMA cycle counts are maintained for each of the four channels, and a control signal notifies the peripheral when the preprogrammed member of DMA cycles has occurred. Output control signals are also provided which allow simplified sectored data transfers and expansion to other μPD8257-5 devices for systems requiring more than four DMA channels.

FEATURES

- NEC Now Supplies μPD8257-5 to μPD8257 Requirements
- Four Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Automatic Load Mode
- Single TTL Clock
- Single +5V Supply ±10%
- Expandable
- 40 Pin Plastic Dual-In-Line Package

PIN CONFIGURATION

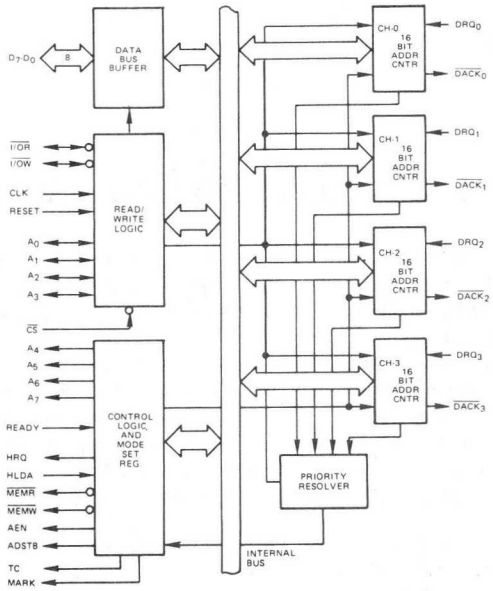


PIN NAMES

D_7-D_0	Data Bus
A_7-A_0	Address Bus
$\overline{I/OR}$	I/O Read
$\overline{I/OW}$	I/O Write
$\overline{MEMR}$	Memory Read
$\overline{MEMW}$	Memory Write
CLK	Clock Input
RESET	Reset Input
READY	Ready
HRQ	Hold Request (to 8080A)
HLDA	Hold Acknowledge (from 8080A)
AEN	Address Enable
ADSTB	Address Strobe
TC	Terminal Count
MARK	Modulo 128 Mark
DRQ_3-DRQ_0	DMA Request Input
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA Acknowledge Out
$\overline{CS}$	Chip Select
V_{CC}	+5 Volts
GND	Ground

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5 to +7 Volts ①
Power Dissipation	1 Watt

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a = 25°C$

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$ GND = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		0.8	Volts	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	Volts	
Output Low Voltage	V_{OL}			0.45	Volts	I_{OL} = 1.7 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	Volts	I_{OH} = −150 μA for AB, DB and AEN I_{OH} = −80 μA for others
HRQ Output High Voltage	V_{HH}	3.3		V_{CC}	Volts	I_{OH} = −80 μA
V_{CC} Current Drain	I_{CC}			120	mA	
Input Leakage	I_{IL}			10	μA	$V_{IN} = V_{CC}$
Output Leakage During Float	I_{OFL}			10	μA	V_{OUT} ①

Note: ① $V_{CC} > V_{OUT} >$ GND + 0.45V

CAPACITANCE

$T_a = 25°C$; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

AC CHARACTERISTICS PERIPHERAL (SLAVE) MODE

BUS PARAMETERS

T_a = 0°C to 70°C; V_{CC} = 5V ± 10%; GND = 0V ①

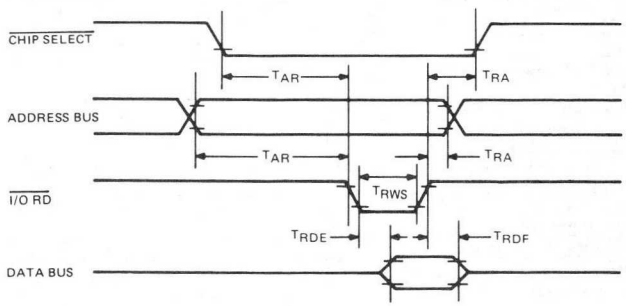
PARAMETER	SYMBOL	② LIMITS μPD8257 MIN	TYP	MAX	μPD8257-5 MIN	TYP	MAX	UNIT	TEST CONDITIONS
READ									
Adr or $\overline{CS}$↓ Setup to $\overline{Rd}$↓	T_{AR}	0			0			ns	
Adr or $\overline{CS}$↑ Hold from $\overline{Rd}$↑	T_{RA}	0			0			ns	
Data Access from $\overline{Rd}$↓	T_{RDE}	0		300	0		170	ns	C_L = 100 pF
DB→Float Delay from $\overline{Rd}$↑	T_{RDF}	20		150	20		100	ns ns	C_L = 100 pF C_L = 15 pF
$\overline{Rd}$ Width	T_{RW}	250			250			ns	
WRITE									
$\overline{CS}$↓ Setup to $\overline{Wr}$↓	T_{CW}	300			300			ns	
$\overline{CS}$↑ Hold from $\overline{Wr}$↑	T_{WC}	20			20			ns	
Adr Setup to $\overline{Wr}$↓	T_{AW}	20			20			ns	
Adr Hold from $\overline{Wr}$↑	T_{WA}	0			0			ns	
Data Setup to $\overline{Wr}$↓	T_{DW}	200			200			ns	
Data Hold from $\overline{Wr}$↑	T_{WD}	0			0			ns	
Wr Width	T_{WWS}	200			200			ns	
OTHER TIMING									
Reset Pulse Width	T_{RSTW}	300			300			ns	
Power Supply ↑(V_{CC}) Setup to Reset↓	T_{RSTD}	500			500			μs	
Signal Rise Time	T_r			20			20	ns	
Signal Fall Time	T_f			20			20	ns	
Reset to First $\overline{IOWR}$	T_{RSTS}	2			2			t_{CY}	

Note: ① All timing measurements are made at the following reference voltages unless specified otherwise: Input "1" at 2.0V, "0" at 0.8V, Output "1" at 2.0V, "0" at 0.8V.

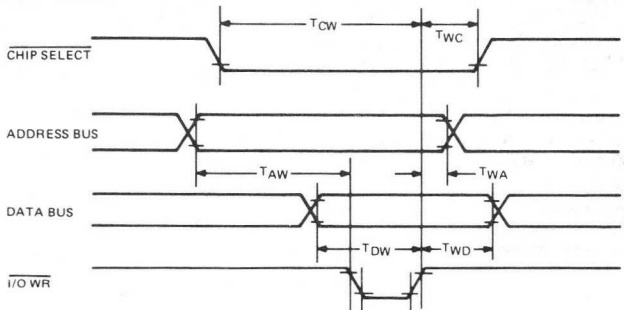
② Data for comparison only.

TIMING WAVEFORMS PERIPHERAL (SLAVE) MODE

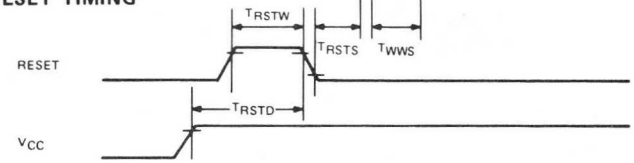
READ TIMING



WRITE TIMING



RESET TIMING



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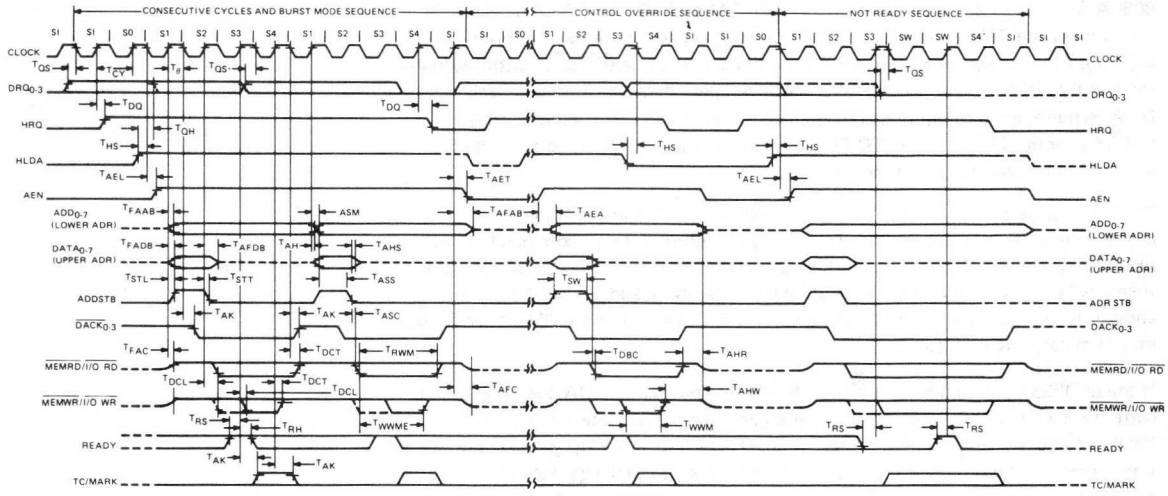
AC CHARACTERISTICS
DMA (MASTER) MODE

T_a = 0°C to 70°C; V_{CC} = +5V ± 10%; GND = 0V

PARAMETER	SYMBOL	LIMITS				UNIT	TEST CONDITIONS
		(8) μPD8257		μPD8257-5			
		MIN	MAX	MIN	MAX		
Cycle Time (Period)	T_{CY}	0.320	4	0.250	4	μs	
Clock Active (High)	T_θ	120	.8T_{CY}	30	.8T_{CY}	ns	
DRQ↑ Setup to θ↓ (SI, S4)	T_{QS}	120		120			
DRQ↓ Hold from HLDA↑	T_{QH}	0		0			④
HRQ↑ or ↓Delay from θ↑ (SI, S4) (measured at 2.0V)	T_{DQ}		160		160	ns	①
HRQ↑ or ↓ Delay from θ↑ (SI, S4) (measured at 3.3V)	T_{DQ1}		250		250	ns	③
HLDA↑ or ↓Setup to θ↓ (SI, S4)	T_{HS}	100		100		ns	
AEN↑ Delay from θ↓ (S1)	T_{AEL}		300		250	ns	①
AEN↓ Delay from θ↑ (SI)	T_{AET}		200		200	ns	①
Adr (AB) (Active) Delay from AEN↑ (S1)	T_{AEA}	20		20		ns	④
Adr (AB) (Active) Delay from θ↑ (S1)	T_{FAAB}		250		250	ns	②
Adr (AB) (Float) Delay from θ↑ (SI)	T_{AFAB}		150		150	ns	②
Adr (AB) (Stable) Delay from θ↑ (S1)	T_{ASM}		250		250	ns	②
Adr (AB) (Stable) Hold from θ↑ (S1)	T_{AH}	T_{ASM}−50		T_{ASM}−50			②
Adr (AB) (Valid) Hold from $\overline{Rd}$↑ (S1, SI)	T_{AHR}	60		60		ns	④
Adr (AB) (Valid) Hold from $\overline{Wr}$↑ (S1, SI)	T_{AHW}	300		300		ns	④
Adr (DB) (Active) Delay from θ↑ (S1)	T_{FADB}		300		250	ns	②
Adr (DB) (Float) Delay from θ↑ (S2)	T_{AFDB}	T_{STT}+20	250	T_{STT}+20	170	ns	②
Adr (DB) Setup to Adr Stb↓ (S1-S2)	T_{ASS}	100		100		ns	④
Adr (DB) (Valid) Hold from Adr Stb↓ (S2)	T_{AHS}	50		50		ns	④
Adr Stb↑ Delay from θ↑ (S1)	T_{STL}		200		200	ns	①
Adr Stb↓ Delay from θ↑ (S2)	T_{STT}		140		140	ns	①
Adr Stb Width (S1-S2)	T_{SW}	T_{CY}−100		T_{CY}−100		ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr Stb↓ (S2)	T_{ASC}	70		70		ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr (DB) (Float) (S2)	T_{DBC}	20		20		ns	④
DACK↑ or ↓Delay from θ↓ (S2, S1) and TC/Mark ↑ Delay from θ↑ (S3) and TC/Mark ↓ Delay from θ↑ (S4)	T_{AK}		250		250	ns	① ⑤
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from θ↑ (S2) and $\overline{Wr}$↓ Delay from θ↑ (S3)	T_{DCL}		200		200	ns	② ⑥
$\overline{Rd}$↑ Delay from θ↓ (S1, SI) and $\overline{Wr}$↑ Delay from θ↑ (S4)	T_{DCT}		200		200	ns	② ⑦
$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑ (S1)	T_{FAC}		300		250	ns	②
$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑ (SI)	T_{AFC}		150		150	ns	②
$\overline{Rd}$ Width (S2-S1 or SI)	T_{RWM}	$2T_{CY}$+ T_θ−50		$2T_{CY}$+ T_θ−50		ns	④
$\overline{Wr}$ Width (S3-S4)	T_{WWM}	T_{CY}−50		T_{CY}−50		ns	④
$\overline{Wr}$ (Ext) Width (S2-S4)	T_{WWME}	$2T_{CY}$−50		$2T_{CY}$−50		ns	④
READY Set Up Time to θ↑ (S3, Sw)	T_{RS}	30		30		ns	
READY Hold Time from θ↑ (S3, Sw)	T_{RH}	20		20		ns	

Notes: ① Load = 1 TTL
② Load = 1 TTL + 50 pF
③ Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V
④ Tracking Specification
⑤ ΔT_{AK} <50 ns
⑥ ΔT_{DGL} <50 ns
⑦ ΔT_{DCT} <50 ns
⑧ Data for comparison only

TIMING WAVEFORMS
DMA (MASTER) MODE



FUNCTIONAL DESCRIPTION

The μPD8257-5 is a programmable, Direct Memory Address (DMA) device. When used with an 8212 I/O port device, it provides a complete four-channel DMA controller for use in 8080A/8085A based systems. Once initialized by an 8080A/8085A CPU, the μPD8257-5 will block transfer up to 16,364 bytes of data between memory and a peripheral device without any attention from the CPU, and it will do this on all 4-DMA channels. After receiving a DMA transfer request from a peripheral, the following sequence of events occurs within the μPD8257-5.

- It acquires control of the system bus (placing 8080A/8085A in hold mode).
- Resolves priority conflicts if multiple DMA requests are made.
- A 16-bit memory address word is generated with the aid of an 8212 in the following manner:

  The μPD8257-5 outputs the least significant eight bits (A_0-A_7) which go directly onto the address bus.

  The μPD8257-5 outputs the most significant eight bits (A_8-A_{15}) onto the data bus where they are latched into an 8212 and then sent to the high order bits on the address bus.
- The appropriate memory and I/O read/write control signals are generated allowing the peripheral to receive or deposit a data byte directly from or to the appropriate memory location.

Block transfer of data (e.g., a sector of data on a floppy disk) either to or from a peripheral may be accomplished as long as the peripheral maintains its DMA Request (DRQ_n). The μPD8257-5 retains control of the system bus as long as DRQ_n remains high or until the Terminal Count (TC) is reached. When the Terminal Count occurs, TC goes high, informing the CPU that the operation is complete.

There are three different modes of operation:

- DMA read, which causes data to be transferred from memory to a peripheral;
- DMA write, which causes data to be transferred from a peripheral to memory; and
- DMA verify, which does not actually involve the transfer of data.

The DMA read and write modes are the normal operating conditions for the μPD8257-5. The DMA verify mode responds in the same manner as read/write except no memory or I/O read/write control signals are generated, thus preventing the transfer of data. The peripheral gains control of the system bus and obtains DMA Acknowledgements for its requests, thus allowing it to access each byte of a data block for check purposes or accumulation of a CRC (Cyclic Redundancy Code) checkword. In some applications it is necessary for a block of DMA read or write cycles to be followed by a block of DMA verify cycles to allow the peripheral to verify its newly acquired data.

DMA OPERATION

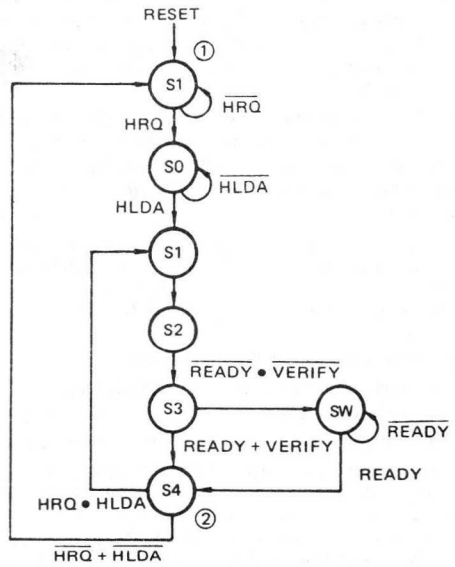
Internally the μPD8257-5 contains six different states (S0, S1, S2, S3, S4 and SW). The duration of each state is determined by the input clock. In the idle state, (S1), no DMA operation is being executed. A DMA cycle is started upon receipt of one or more DMA Requests (DRQ_n), then the μPD8257-5 enters the S0 state. During state S0 a Hold Request (HRQ) is sent to the 8080A/8085A and the μPD8257-5 waits in S0 until the 8080A/8085A issues a Hold Acknowledge (HLDA) back. During S0, DMA Requests are sampled and DMA priority is resolved (based upon either the fixed or priority scheme). After receipt of HLDA, the DMA Acknowledge line ($\overline{DACK}_n$) with the highest priority is driven low, selecting that particular peripheral for the DMA cycle. The DMA Request line (DRQ_n) must remain high until either a DMA Acknowledge ($\overline{DACK}_n$) or both $\overline{DACK}_n$ and TC (Terminal Count) occur, indicating the end of a block or sector transfer (burst model).

The DMA cycle consists of four internal states; S1, S2, S3 and S4. If the access time of the memory or I/O device is not fast enough to return a Ready command to the μPD8257-5 after it reaches state S3, then a Wait state is initiated (SW). One or more than one Wait state occurs until a Ready signal is received, and the μPD8257-5 is allowed to go into state S4. Either the extended write option or the DMA Verify mode may eliminate any Wait state.

If the μPD8257-5 should lose control of the system bus (i.e., HLDA goes low) then the current DMA cycle is completed, the device goes into the S1 state, and no more DMA cycles occur until the bus is reacquired. Ready setup time (t_{RS}), write setup time (t_{DW}), read data access time (t_{RD}) and HLDA setup time (t_{QS}) should all be carefully observed during the handshaking mode between the μPD8257-5 and the 8080A/8085A.

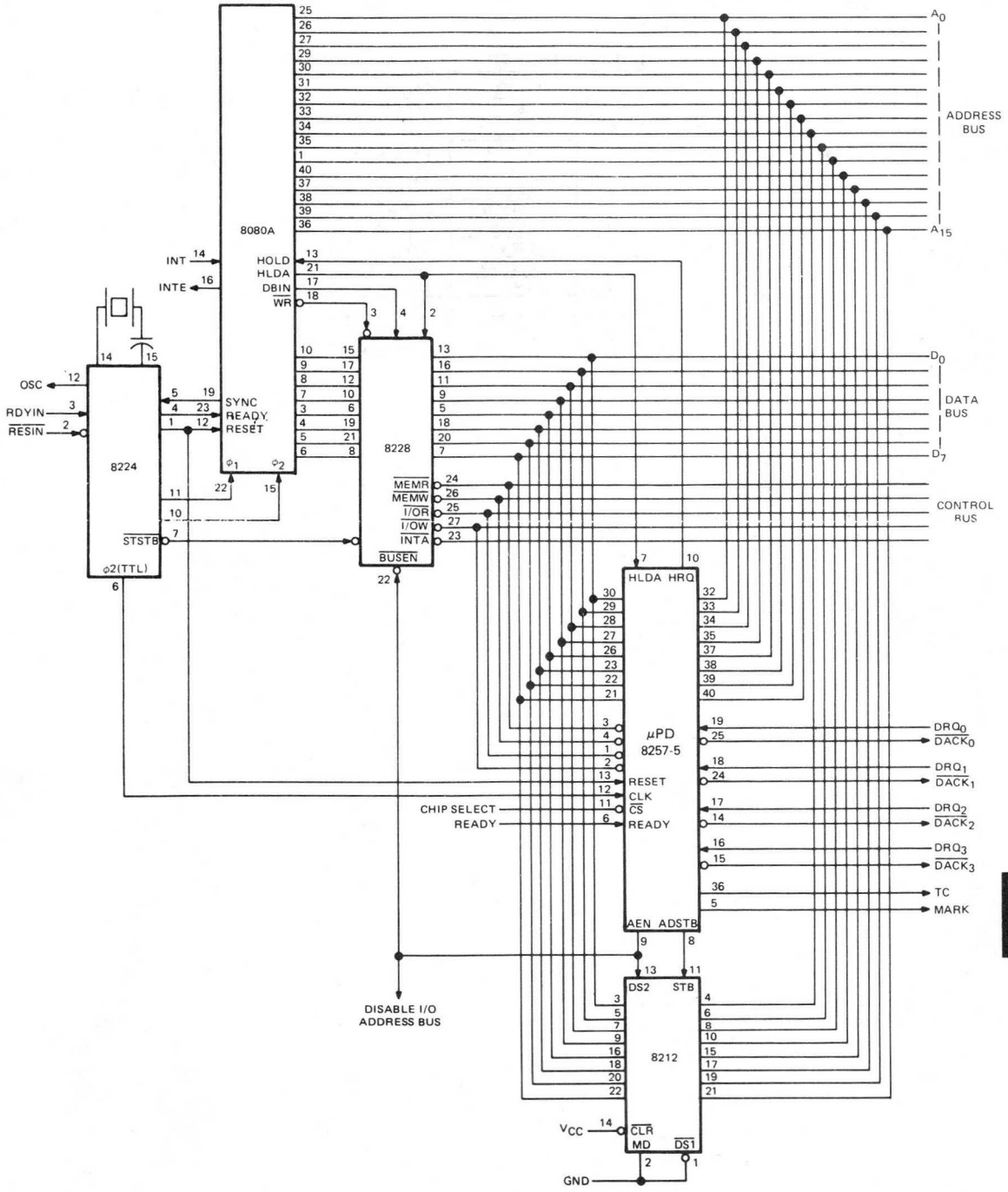
During DMA write cycles, the I/O Read ($\overline{I/O\ R}$) output is generated at the beginning of state S2 and the Memory Write ($\overline{MEMW}$) output is generated at the beginning of S3. During DMA read cycles, the Memory Read ($\overline{MEMR}$) output is generated at the beginning of state S2 and the I/O Write ($\overline{I/O\ W}$) goes low at the beginning of state S3. No Read or Write control signals are generated during DMA verify cycles.

DMA OPERATION STATE DIAGRAM

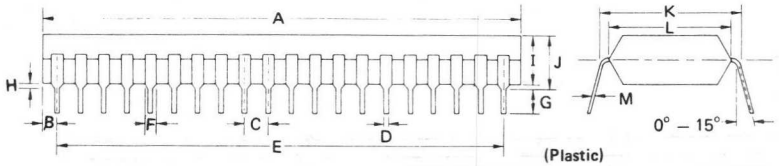


Notes: ① HRQ is set if DRQ_n is active.
② HRQ is reset if DRQ_n is not active.

TYPICAL μPD8257-5
SYSTEM INTERFACE SCHEMATIC



PACKAGE OUTLINE
μPD8257C
μPD8257C-5



(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

PROGRAMMABLE INTERRUPT CONTROLLER

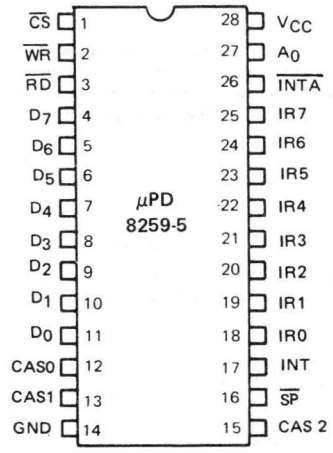
DESCRIPTION

The NEC μPD8259-5 is a programmable interrupt controller directly compatible with the 8080A/8085A/μPD780(Z80™). It can service eight levels of interrupts and contains on-chip logic to expand interrupt capabilities up to sixty-four levels with the addition of other μPD8259-5's. The user is offered a selection of priority algorithms to tailor the priority processing to meet his systems requirements. These algorithms can be dynamically modified during operation, expanding the versatility of the microprocessor system.

FEATURES

- NEC now Supplies μPD8259-5 to μPD8259 Requirements
- Eight Level Priority Controller
- Programmable Base Vector Address
- Expandable to 64 Levels
- Programmable Interrupt Modes (Algorithms)
- Individual Request Mask Capability
- Single +5V Supply ±10% (No Clocks)
- Full Compatibility with 8080A
- μPD8259-5 Compatible with 8085A Speeds
- Available in 28 Pin Plastic and Ceramic Packages

PIN CONFIGURATION



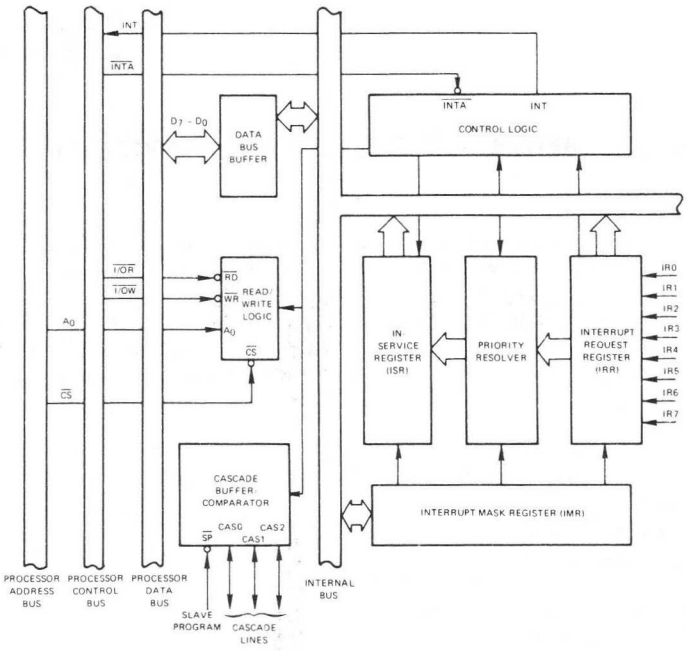
PIN NAMES

$D_7 - D_0$	Data Bus (Bi-Directional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Command Select Address
CAS2 – CAS0	Cascade Lines
$\overline{SP}$	Slave Program Input
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0 – IR7	Interrupt Request Inputs
$\overline{CS}$	Chip Select

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TM: Z80 is a registered trademark of Zilog, Inc.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
Voltage on Any Pin	−0.5 to +7 Volts (1)
Power Dissipation	1W

Note: (1) With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5V	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Interrupt Output-High Voltage	V_{OH-INT}	2.4			V	I_{OH} = −400 μA
		3.5			V	I_{OH} = −50 μA
Input Leakage Current for IR_{0-7}	I_{IL} (IR_{0-7})			−300	μA	V_{IN} = 0V
				10	μA	V_{IN} = V_{CC}
Input Leakage Current for other Inputs	I_{IL}			±10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{LOL}			− 10	μA	V_{OUT} = 0.45 V
Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Supply Current	I_{CC}			85	mA	

CAPACITANCE

$T_a = 25°C$; $V_{CC} = GND = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured Pins Returned to V_{SS}

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$; GND = 0V

PARAMETER	SYMBOL	LIMITS ② 8259 MIN	LIMITS ② 8259 MAX	LIMITS 8259-5 MIN	LIMITS 8259-5 MAX	UNIT	TEST CONDITIONS
READ							
$\overline{CS}/A_0$ Stable Before $\overline{RD}$ or $\overline{INTA}$	t_{AR}	50		0		ns	
$\overline{CS}/A_0$ Stable After $\overline{RD}$ or $\overline{INTA}$	t_{RA}	50		0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	420		250		ns	
Data Valid From $\overline{RD}/\overline{INTA}$	t_{RD}		300		150	ns	①
Data Float After $\overline{RD}/\overline{INTA}$	t_{DF}	20	200	20	100	ns	①
WRITE							
A_0 Stable Before $\overline{WR}$	t_{AW}	50		0		ns	
A_0 Stable After $\overline{WR}$	t_{WA}	20		0		ns	
$\overline{CS}$ Stable Before $\overline{WR}$	t_{CW}	50				ns	
$\overline{CS}$ Stable After $\overline{WR}$	t_{WC}	20				ns	
$\overline{WR}$ Pulse Width	t_{WW}	400		250		ns	
Data Valid to $\overline{WR}$ (T.E.)	t_{DW}	300		150		ns	
Data Valid After $\overline{WR}$	t_{WD}	40		0		ns	
OTHER							
Width of Interrupt Request Pulse	t_{IW}	100		100		ns	
INT ↑ After IR ↑	t_{INT}	400		250		ns	
Cascade Line Stable After $\overline{INTA}$ ↑	t_{IC}	400		300		ns	

Note: ① For μPD8259: C_L = 100 pf; for μPD8259-5: C_L = 150 pf
② Data for Comparison only

9

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupt request register and in-service register store the in-coming interrupt request signals appearing on the IR0-7 lines (refer to functional block diagram). The inputs requesting service are stored in the IRR while the interrupts actually being serviced are stored in the ISR.

A positive transition on an IR input sets the corresponding bit in the Interrupt Request Register, and at the same time the INT output of the μPD8259-5 is set high. The IR input line must remain high until the first INTA input has been received. Multiple, non-masked interrupts occurring simultaneously can be stored in the IRR. The incoming $\overline{\text{INTA}}$ sets the appropriate ISR bit (determined by the programmed interrupt algorithm) and resets the corresponding IRR bit. The ISR bit stays high-active during the interrupt service subroutine until it is reset by the programmed End-of-Interrupt (EOI) command.

PRIORITY RESOLVER

The priority resolver decides the priority of the interrupt levels in the IRR. When the highest priority interrupt is determined it is loaded into the appropriate bit of the In-Service register by the first $\overline{\text{INTA}}$ pulse.

DATA BUS BUFFER

The 3-state, 8-bit, bi-directional data bus buffer interfaces the μPD8259-5 to the processor's system bus. It buffers the Control Word and Status Data transfers between the μPD8259-5 and the processor bus.

READ/WRITE LOGIC

The read/write logic accepts processor data and stores it in its Initialization Command Word (ICW) and Operation Command Word (OCW) registers. It also controls the transfer of the Status Data to the processor's data bus.

CHIP SELECT ($\overline{\text{CS}}$)

The μPD8259-5 is enabled when an active-low signal is received at this input. Reading or writing of the μPD8259-5 is inhibited when it is not selected.

WRITE ($\overline{\text{WR}}$)

This active-low signal instructs the μPD8259-5 to receive Command Data from the processor.

READ ($\overline{\text{RD}}$)

When an active-low signal is received on the $\overline{\text{RD}}$ input, the status of the Interrupt Request Register, In-Service Register, Interrupt Mask Register or binary code of the Interrupt Level is placed on the data bus.

INTERRUPT (INT)

The interrupt output from the μPD8259-5 is directly connected to the processor's INT input. The voltage levels of this output are compatible with the 8080/8085 input voltage and timing requirements.

INTERRUPT MASK REGISTER (IMR)

The interrupt mask register stores the bits for the individual interrupt bits to be masked. The IMR masks the data in the ISR. Lower priority lines are not affected by masking a higher priority line.

FUNCTIONAL DESCRIPTION (CONT.)

INTERRUPT ACKNOWLEDGE ($\overline{INTA}$)

The interrupt acknowledge signal is usually received from the 8228 (system controller for the 8080A). The system controller generates three INTA pulses to signal the 8259-5 to issue a 3-byte CALL instruction onto the data bus.

A_0

A_0 is usually connected to the processor's address bus. Together with $\overline{WR}$ and $\overline{RD}$ signals it directs the loading of data into the command register or the reading of status data. The following table illustrates the basic operations performed. Note that it is divided into three functions: Input, Output and Bus Disable distinguished by the $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ inputs.

μPD8259 BASIC OPERATION						
A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	PROCESSOR INPUT OPERATION (READ)
0			0	1	0	IRR, ISR or IR → Data Bus ①
1			0	1	0	IMR → Data Bus
						PROCESSOR OUTPUT OPERATION (WRITE)
0	0	0	1	0	0	Data Bus → OCW2
0	0	1	1	0	0	Data Bus → OCW3
0	1	X	1	0	0	Data Bus → ICW1
1	X	X	1	0	0	Data Bus → OCW1, ICW2, ICW3 ②
						DISABLE FUNCTION
X	X	X	1	1	0	Data Bus → 3-State
X	X	X	X	X	1	Data Bus → 3-State

Notes: ① The contents of OCW2 written prior to the READ operation governs the selection of the IRR, ISR or Interrupt Level.

② The sequencer logic on the μPD8259-5 aligns these commands in the proper order.

CASCADE BUFFER/COMPARATOR. (For Use in Multiple μPD8259-5 Array.)

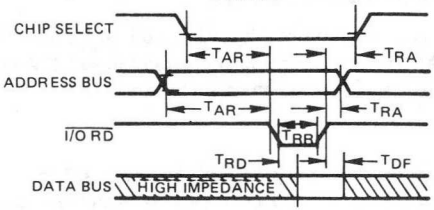
The ID's of all μPD8259-5's are buffered and compared in the cascade buffer/comparator. The master μPD8259-5 will send the ID of the interrupting slave device along the CAS0, 1, 2 lines to all slave devices. The cascade buffer/comparator compares its preprogrammed ID to the CAS0, 1, 2 lines. The next two $\overline{INTA}$ pulses strobe the preprogrammed, 2 byte CALL routine address onto the data bus from the slave whose ID matches the code on the CAS0, 1, 2 lines.

SLAVE PROGRAM ($\overline{SP}$). (For Use in Multiple μPD8259 Array.)

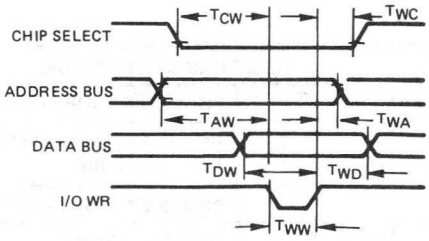
The interrupt capability can be expanded to 64 levels by cascading multiple μPD8259-5's in a master-plus-slaves array. The master controls the slaves through the CAS0, 1, 2 lines. The SP input to the device selects the CAS0-2 lines as either outputs (SP=1) for the master or as inputs (SP=0) for the slaves. For one device only the SP must be set to a logic "1" since it is functioning as a master.

TIMING WAVEFORMS

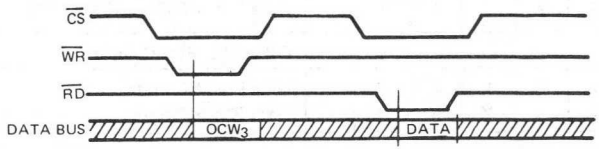
READ



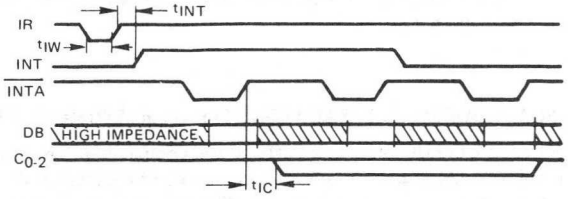
WRITE



READ STATUS/POLL MODE

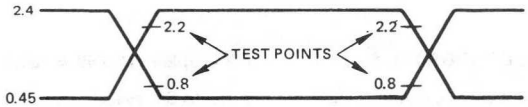


OTHER

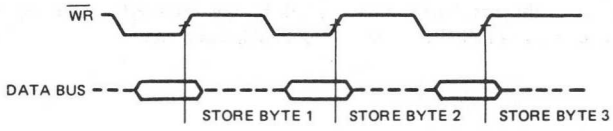


Note: IR must stay "high" at least until the leading edge of 1st $\overline{INTA}$.

INPUT WAVEFORMS FOR AC TESTS



INITIALIZATION SEQUENCE



DETAILED OPERATIONAL DESCRIPTION

The μPD8259-5 derives its versatility from its programmable interrupt modes and its ability to jump to any memory address through programmable CALL instructions. The following sequence demonstrates how the μPD8259-5 interacts with the processor.

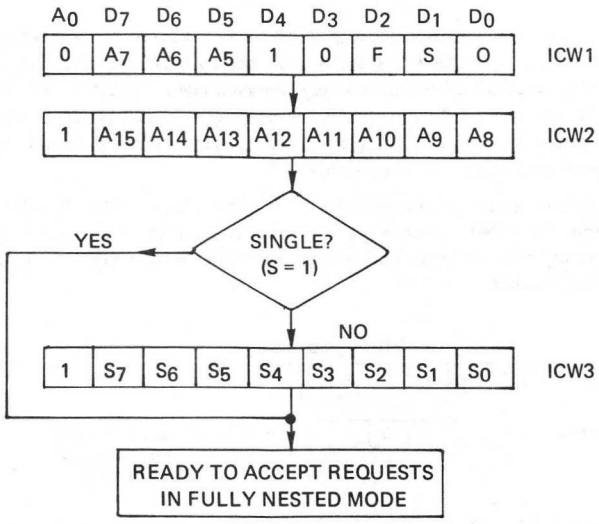
1. An interrupt or interrupts appearing on IR_{0-7} sets the corresponding IR bit(s) high. This in turn sets the corresponding IRR bit(s) high.
2. Once the IRR bit(s) has been set, the μPD8259-5 will resolve the priorities according to the preprogrammed interrupt algorithm. It then issues an INT signal to the processor.
3. The processor group issues an $\overline{\text{INTA}}$ to the μPD8259-5 when it receives the INT.
4. The $\overline{\text{INTA}}$ input to the μPD8259-5 from the processor group sets the highest priority ISR bit and resets the corresponding IRR bit. The INTA also signals the μPD8259-5 to issue an 8-bit CALL instruction op-code (11001101) onto its Data bus lines.
5. The CALL instruction code instructs the processor group to issue two more $\overline{\text{INTA}}$ pulses to the μPD8259-5.
6. The two $\overline{\text{INTA}}$ pulses signal the μPD8259-5 to place its preprogrammed interrupt vector address onto the Data bus. The first $\overline{\text{INTA}}$ releases the low-order 8-bits of the address and the second $\overline{\text{INTA}}$ releases the high-order 8-bits.
7. The μPD8259-5's CALL instruction sequence is complete. A preprogrammed EOI (End-of-Interrupt) command is issued to the μPD8259-5 at the end of an interrupt service routine to reset the ISR bit and allow the μPD8259-5 to service the next interrupt.

PROGRAMMING THE μPD8259-5

Two types of command words are required from the processor to fully define the operating modes of the μPD8259-5.

1. **Initialization Command Words (ICWs)**

   Each μPD8259-5 in the interrupt array must be initialized prior to normal operation. The initialization is performed by a 2 or 3-byte sequence clocked by $\overline{\text{WR}}$ pulses. Figure 1 shows this sequence. (Refer to Figure 2 for bit definitions.)



INITIALIZATION SEQUENCE – FIGURE 1.

PROGRAMMING THE μPD8259-5 (CONT.)

2. Operation Command Words (OCWs)

The operation command words are used to program the various interrupt algorithms listed below:

- Fully Nested Mode
- Rotating Priority Mode
- Special Mask Mode
- Polled Mode

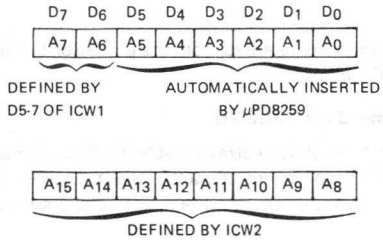
Once the μPD8259-5 has been initialized, OCWs can be written at any time.

INITIALIZATION COMMAND WORDS 1 and 2 (ICW1 and ICW2)

When $A_0 = 0$ and $D_4 = 1$ in a command to the μPD8259-5, together with CS = 0, it is recognized as Initialization Command Word 1. This is the start of the initialization sequence and causes the following to occur:

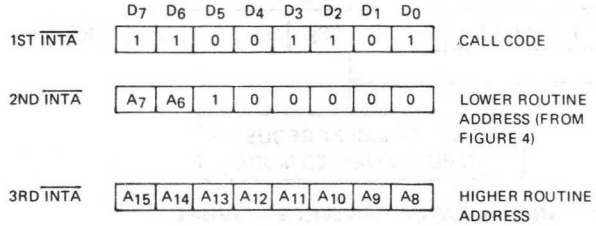
- The Interrupt Request edge-sense circuitry is reset so that an input must make a low-to-high transition to generate its interrupt.
- The initialization sequence clears Interrupt Mask Register to all unmasked and resets the Special Mask Mode and Status Read Flip-Flops.
- IR_7 input is set to priority 7.

There are eight equally-spaced base vector addresses in memory for the eight interrupt inputs. The interval between the base vector addresses can be programmed to be either four or eight requiring 32 or 64 bytes in memory, respectively. The following shows how the address format is mapped onto the Data bus.



The μPD8259-5 automatically defines A_{0-4} with a separate address for each interrupt input. The base vector addresses A_{15-6} are programmed by ICW1 and ICW2. A_5 is either defined by the μPD8259-5 if the address interval is eight or must be user-define the interval is 4. The 8-byte CALL interval is consistent with 8080A processor RESTART instruction software. The 4-byte CALL interval can be used for a compact jump table. Refer to Figure 4 for a table of address formats.

The following is an example of an interrupt acknowledge sequence. The μPD8259-5 has been programmed for a CALL address (base vector address) interval of eight (F = 0) and there is an interrupt appearing on IR_4. The 3-byte sequence is strobed out to the Data bus by three $\overline{INTA}$ pulses.



INITIALIZATION COMMAND WORD 3 (ICW3) ①

It is only necessary to program ICW3 when there are multiple μPD8259-5's in the interrupt array, i.e., S = 0. There are two types of ICW3s. The first is for programming the master μPD8259-5. The second is for the slaves.

1. ICW3-Master μPD8259-5. A "1" is set in S_{0-7} for each corresponding slave in the interrupt array. The S_{0-7} bits, together with $\overline{SP}$ = 1, instructs the cascade buffer/comparator to send the ID of the interrupting slave on the CAS0,1,2 lines.
2. ICW3-SLAVE μPD8259-5(s). Bits D_7-D_3 are "don't care" bits and have no effect on ICW3. The ID of each slave is programmed by bits D_{0-2} ($ID_{0,1,2}$). Once the master μPD8259-5 has sent out the first byte of the CALL sequence, the slave device(s) with their $\overline{SP}$ inputs set to Logic 0, compare their IDs appearing on the CAS0,1,2 lines through the cascade buffer/comparator. The slave whose ID matches the CAS0,1,2 code then issues bytes 2 and 3 of the CALL sequence.

OPERATIONAL COMMAND WORDS (OCWs) ②

Once the μPD8259-5 has been programmed with Initialization Command Words, it can now be programmed for the appropriate interrupt algorithm by the Operation Command Words. Interrupt algorithms in the μPD8259-5 can be changed at any time during program operation by issuing another set of Operation Command Words. The following sections describe the various algorithms available and their associated OCWs.

INTERRUPT MASKS

The individual Interrupt Request input lines are maskable by setting the corresponding bits in the Interrupt Mask Register to a logic "1" through OCW1. The actual masking is performed upon the contents of the In-Service Register (e.g., if Interrupt Request line 3 is to be masked, then only bit 3 of the IMR is set to logic "1." The IMR in turn acts upon the contents of the ISR to mask bit 3). Once the μPD8259-5 has acknowledged an interrupt, i.e., the μPD8259-5 has sent an INT signal to the processor and the system controller has sent it an $\overline{INTA}$ signal, the interrupt input, although it is masked, will inhibit lower priority requests from being acknowledged. There are two means of enabling these lower priority interrupt lines. The first is by issuing an End-of-Interrupt (EOI) through Operation Command Word 2 (OCW2), thereby resetting the appropriate ISR bit. The second approach is to select the Special Mask Mode through OCW3. The Special Mask Mode (SMM) and End-of-Interrupt (EOI) will be described in more detail further on.

FULLY NESTED MODE

The fully nested mode is the μPD8259-5's basic operating mode. It will operate in this mode after the initialization sequence, requiring no Operation Command Words for formatting. Priorities are set IR_0 through IR_7 with IR_0 the highest priority. After the interrupt has been acknowledged by the processor and system controller, only higher priorities will be serviced. Upon receiving an $\overline{INTA}$, the priority resolver determines the priority of the interrupt, the corresponding ISR bit is set, and the vector address is output to the Data bus. The EOI command resets the corresponding ISR bit at the end of its service routine.

Notes: ① Reference Figure 2
② Reference Figure 3

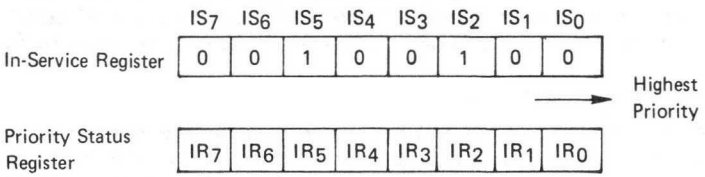
ROTATING PRIORITY MODE COMMANDS

The two variations of Rotating Priorities are the Auto Rotate and Specific Rotate modes. These two modes are typically used to service interrupting devices of equivalent priorities.

1. Auto Rotate Mode

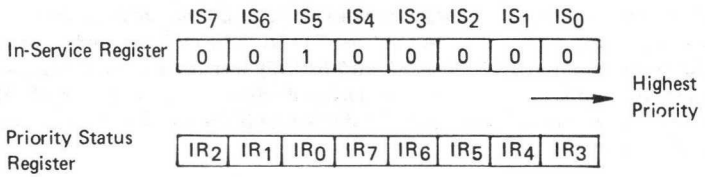
   Programming the Auto Rotate Mode through OCW2 assigns priorities 0-7 to the interrupt request input lines. Interrupt line IR_0 is set to the highest priority and IR_7 to the lowest. Once an interrupt has been serviced it is automatically assigned the lowest priority. That same input must then wait for the devices ahead of it to be serviced before it can be acknowledged again. The Auto Rotate Mode is selected by programming OCW2 in the following way (refer to Figure 3): set Rotate Priority bit "R" to a logic "1"; program EOI to a logic "1" and SEOI to a logic "0." The EOI and SEOI commands are discussed further on. The following is an example of the Auto Rotate Mode with devices requesting interrupts on lines IR_2 and IR_5.

   Before Interrupts are Serviced:



   According to the Priority Status Register, IR_2 has a higher priority than IR_5 and will be serviced first.

   After Servicing:



   At the completion of IR_2's service routine the corresponding In-Service Register bit, IS_2 is reset to "0" by the preprogrammed EOI command. IR_2 is then assigned the lowest priority level in the Priority Status Register. The μPD8259-5 is now ready to service the next highest interrupt, which in this case, is IR_5.

2. Specific Rotate Mode

   The priorities are set by programming the lowest level through OCW2. The μPD8259-5 then automatically assigns the highest priority. If, for example, IR_3 is set to the lowest priority (bits L_2, L_1, L_0 form the binary code of the bottom priority level), then IR_4 will be set to the highest priority. The Specific Rotate Mode is selected by programming OCW2 in the following manner: set Rotate Priority bit "R" to a logic "1," program EOI to a logic "0," SEOI to a logic "1" and L_2, L_1, L_0 to the lowest priority level. If EOI is set to a logic "1," the ISR bit defined by L_2, L_1, L_0 is reset.

OPERATIONAL COMMAND WORDS (CONT.)

END-OF-INTERRUPT (EOI) AND SPECIFIC END-OF-INTERRUPT (SEOI)

The End-of-Interrupt or Specific End-of-Interrupt command must be issued to reset the appropriate In-Service Register bit before the completion of a service routine. Once the ISR bit has been reset to logic "0," the μPD8259-5 is ready to service the next interrupt

Two types of EOIs are available to clear the appropriate ISR bit depending on the μPD8259-5's operating mode.

1. Non-Specific End-of-Interrupt (EOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is preserved (e.g., fully nested mode), the particular ISR bit to be reset at the completion of the service routine can be determined. A non-specific EOI command will automatically reset the highest priority ISR bit of those set. The highest priority ISR bit must necessarily be the interrupt being serviced and must necessarily be the service subroutine returned from.

2. Specific End-of-Interrupt (SEOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is not preserved (e.g., rotating priority mode) the last serviced interrupt level may not be known. In these modes a Specific End-of-Interrupt must be issued to clear the ISR bit at the completion of the interrupt service routine. The SEOI is programmed by setting the appropriate bits in OCW3 (Figure 2) to logic "1"s. Both the EOI and SEOI bits of OCW3 must be set to a logic "1" with L_2, L_1, L_0 forming the binary code of the ISR bit to be reset.

SPECIAL MASK MODE

Setting up an interrupt mask through the Interrupt Mask Register (refer to Interrupt Mask Register section) by setting the appropriate bits in OCW1 to a logic "1" will inhibit lower priority interrupts from being acknowledged. In applications requiring that the lower priorities be enabled while the IMR is set, the Special Mask Mode can be used. The SMM is programmed in OCW3 by setting the appropriate bits to a logic "1." Once the SMM is set, the μPD8259-5 remains in this mode until it is reset. The Special Mask Mode does not affect the higher priority interrupts.

POLLED MODE

In the Poll Mode the processor must be instructed to disable its interrupt input (INT). Interrupt service is initiated through software by a Poll Command. The Poll Mode is programmed by setting the Poll Mode bit in OCW3 (P = 1), during a $\overline{WR}$ pulse. The following $\overline{RD}$ pulse is then considered as an interrupt acknowledge. If an interrupt input is present, that $\overline{RD}$ pulse sets the appropriate ISR bit and reads the interrupt priority level. The Poll Mode is a one-time operation and must be programmed through OCW3 before every read. The word strobed onto the Data bus during Poll Mode is of the form:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I	X	X	X	X	W_2	W_1	W_0

where: I = 1 if there is an interrupt requesting service
= 0 if there are no interrupts

$W_{2\text{-}0}$ forms the binary code of the highest priority level of the interrupts requesting service

The Poll Mode can be used when an interrupt service routine is common to several interrupt inputs. The $\overline{INTA}$ sequence is no longer required offering a saving in ROM space. The Poll Mode can also be used to expand the number of interrupts beyond 64.

9

READING μPD8259-5 STATUS

The following major registers' status is available to the processor by appropriately formatting OCW3 and issuing $\overline{RD}$ command.

INTERRUPT REQUEST REGISTER (8-BITS)

The Interrupt Request Register stores the interrupt levels awaiting acknowledgement. Once it has been acknowledged, the highest priority in-service bit is reset. (Note that the Interrupt Mask Register has no effect on the IRR.) A $\overline{WR}$ command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. The bits which determine whether the IRR and ISR are being read from are RIS and ERIS. To read contents of the IRR, ERIS must be logic "1" and RIS a logic "0."

IN-SERVICE REGISTER (8-BITS)

The In-Service Register stores the priorities of the interrupt levels being serviced. Assertion of an End-of-Interrupt (EOI) updates the ISR to the next priority level. A $\overline{WR}$ command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. Both ERIS and RIS should be set to a logic "1."

INTERRUPT MASK REGISTER (8-BITS)

The Interrupt Mask Register holds mask data modifying interrupt levels. To read the IMR status a $\overline{WR}$ pulse preceding the $\overline{RD}$ is not necessary. The IMR data is available to the data bus when $\overline{RD}$ is asserted with A_0 at a logic "1."

A single OCW3 is sufficient to enable successive status reads providing it is of the same register. A status read is over-ridden by the Poll Mode where bits P and ERIS of OCW3 are set to a logic "1."

CASCADING MULTIPLE μPD8259-5's

If more than eight interrupt levels are required, multiple μPD8259-5's can be cascaded with one master and up to eight slaves, to accommodate up to 64 levels of interrupt.

As shown in Figure 5, the master device directs the appropriate slave to release its CALL address through its three cascade lines (CAS0,1,2).

The INT output of the slave devices go to the IR inputs of the master device. The master μPD8259-5's INT output is connected to the processor's control bus. When the slave device signals the master that it has acknowledged an interrupt, the master issues an 8080A CALL Op-code at the first $\overline{INTA}$ pulse. The master then signals that slave device (via CAS0,1,2) to issue the appropriate CALL address during the second and third $\overline{INTA}$ pulses.

The slave address code is present on cascade lines 0,1,2 (active-high logic) from the trailing edge of the first $\overline{INTA}$ to the trailing edge of the third $\overline{INTA}$. Each device in the μPD8259-5 array must be individually initialized and can be programmed in different operating modes. Two End-of-Interrupt commands must be issued for the master and its corresponding slave. An address decoder is used to drive the Chip Select inputs for each μPD8259-5 in the array. The Slave Program ($\overline{SP}$) input must be held at a logic " "0" level for each slave device and held at logic "1" level for the master. The SP input selects the Cascade lines as either inputs (SP = 0) or outputs (SP = 1).

INITIALIZATION COMMAND WORD FORMAT

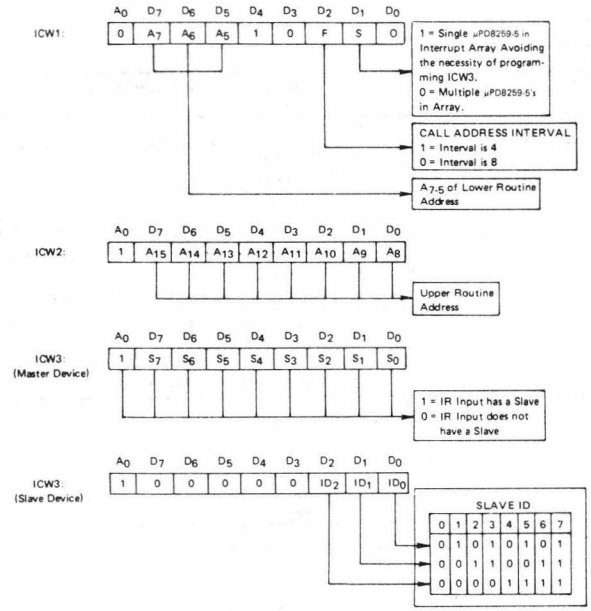


FIGURE 2

OPERATION COMMAND WORD FORMAT

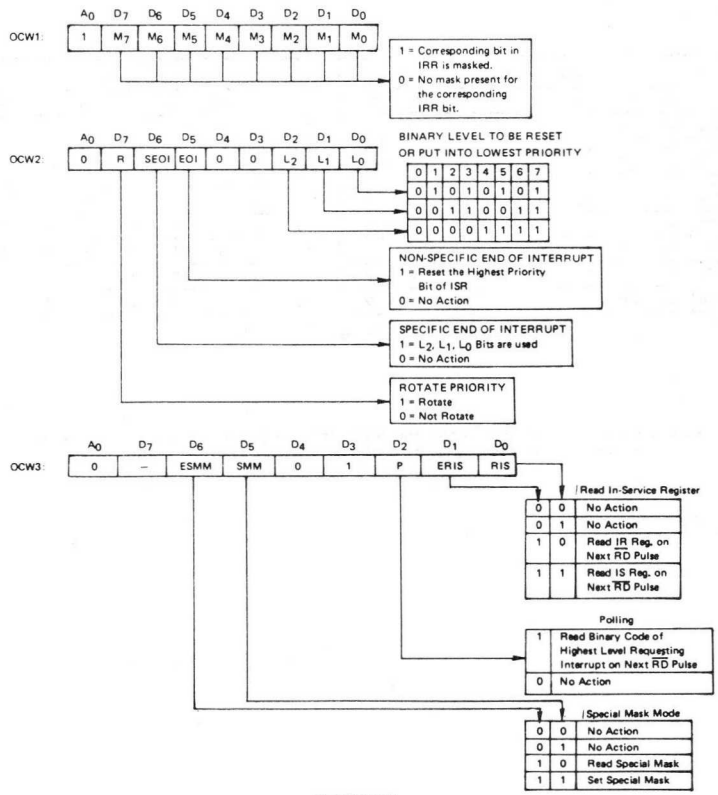


FIGURE 3

9

SUMMARY OF OPERATION COMMAND WORD PROGRAMMING

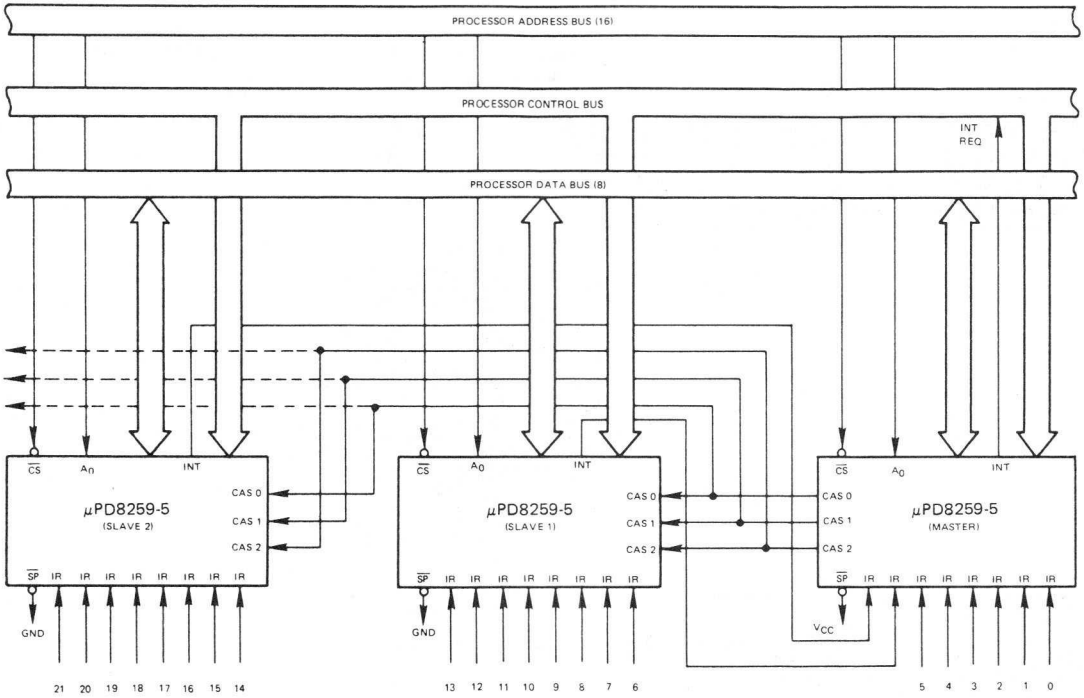
	A_0	D_4	D_3				
OCW1	1	X	X	M_7-M_0			IMR (Interrupt Mask Register) $\overline{WR}$ loads IMR data while $\overline{RD}$ reads status
OCW2	0	0	0	R	SEOI	EOI	
				0	0	0	No Action
				0	0	1	Non-Specific End-of-Interrupt
				0	1	0	No Action
				0	1	1	Specific-End-of-Interrupt L_2, L_1, L_0 forms binary representation of level to be reset.
				1	0	0	No Action
				1	0	1	Rotate Priority at End-of-Interrupt (Auto Mode)
				1	1	0	Rotate Priority, L_2, L_1, L_0 specifies bottom priority without End-of-Interrupt
				1	1	1	Rotate Priority at End-of-Interrupt (Specific Mode). L_2, L_1, L_0 specifies bottom priority, and its In-Service Register bit is reset.
OCW3	0	0	1	ESMM	SMM		
				0	0		Special Mask not affected
				0	1		
				1	0		Reset Special Mask
				1	1		Set Special Mask
				ERIS	RIS		
				0	0		No Action
				0	1		
				1	0		Read IR Register Status
				1	1		Read IS Register Status

LOWER MEMORY INTERRUPT VECTOR ADDRESS

	INTERVAL = 4								INTERVAL = 8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_7	A_7	A_6	A_5	1	1	1	0	0	A_7	A_6	1	1	1	0	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0	A_7	A_6	1	1	0	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0	A_7	A_6	1	0	1	0	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0	A_7	A_6	1	0	0	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0	A_7	A_6	0	1	1	0	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0	A_7	A_6	0	1	0	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0	A_7	A_6	0	0	1	0	0	0
IR_0	A_7	A_6	A_5	0	0	0	0	0	A_7	A_6	0	0	0	0	0	0

FIGURE 4

Note: Insure that the processor's interrupt input is disabled during the execution of any control command and initialization sequence for all μPD8259-5's.

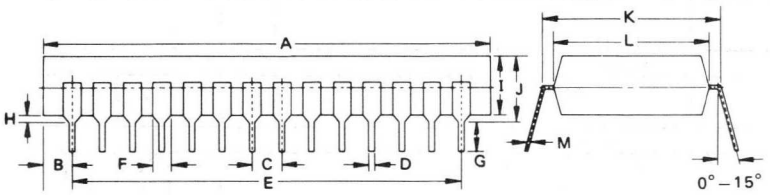


INSTRUCTION SET

Instruction Number	Mnemonic	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operation Description
1	ICW1 A	0	A_7	A_6	A_5	1	0	1	1	0	Byte 1 Initialization, Format = 4, Single
2	ICW1 B	0	A_7	A_6	A_5	1	0	1	0	0	Byte 1 Initialization, Format = 4, Not Single
3	ICW1 C	0	A_7	A_6	A_5	1	0	0	1	0	Byte 1 Initialization, Format = 8, Single
4	ICW1 D	0	A_7	A_6	A_5	1	0	0	0	0	Byte 1 Initialization, Format = 8, Not Single
5	ICW2	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	Byte 2 Initialization (Address No. 2)
6	ICW3 M	1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	Byte 2 Initialization – MASTER
7	ICW3 S	1	0	0	0	0	0	S_2	S_1	S_0	Byte 3 Initialization – SLAVE
8	OCW1	1	M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0	Load Mask Register, Read Mask Register
9	OCW2 E	0	0	0	1	0	0	0	0	0	Non-Specific EOI
10	OCW2 SE	0	0	1	1	0	0	L_2	L_1	L_0	Specific EOI, L_2, L_1, L_0 Code of IS to be Reset
11	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate at EOI (Auto Mode)
12	OCW2 RSE	0	1	1	1	0	0	L_2	L_1	L_0	Rotate at EOI (Specific Mode). L_2, L_1, L_0 Code of Line to be Reset and Selected as Bottom Priority.
13	OCW2 RS	0	1	1	0	0	0	L_2	L_1	L_0	L_2, L_1, L_0 – Code of Bottom Priority Line.
14	OCW3 P	0	–	0	0	0	1	1	0	0	Poll Mode
15	OCW3 RIS	0	–	0	0	0	1	0	1	1	Read IS Register
16	OCW3 RR	0	–	0	0	0	1	0	1	0	Read Requests Register
17	OCW3 SM	0	–	1	1	0	1	0	0	0	Set Special Mask Mode
18	OCW3 RSM	0	–	1	0	0	1	0	0	0	Reset Special Mask Mode

Note: Insure that the processor's interrupt input is disabled during the execution of any control command and initialization sequence for all μPD8259-5's.

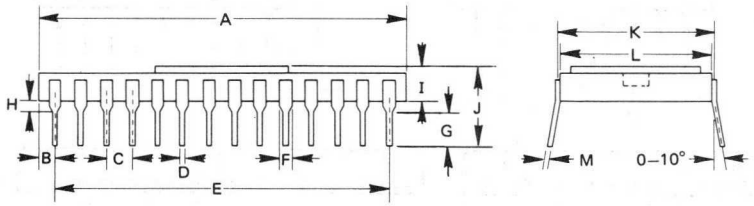
PACKAGE OUTLINE
μPD8259-5C



(Plastic)

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

μPD8259-5D



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	36.2 MAX.	1.43 MAX.
B	1.59 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.46 ± 0.01	0.02 ± 0.004
E	33.02 ± 0.1	1.3 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.002

PROGRAMMABLE INTERRUPT CONTROLLER

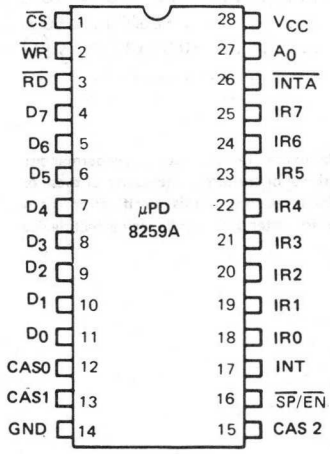
DESCRIPTION

The NEC μPD8259A is a programmable interrupt controller directly compatible with the 8080A/8085A/8086/8088 microprocessors. It can service eight levels of interrupts and contains on-chip logic to expand interrupt capabilities up to 64 levels with the addition of other μPD8259As. The user is offered a selection of priority algorithms to tailor the priority processing to meet his system requirements. These can be dynamically modified during operation, expanding the versatility of the system.
The μPD8259A is completely upward compatible with the μPD8259-5, so software written for the μPD8259-5 will run on the μPD8259A.

FEATURES

- Eight Level Priority Controller
- Programmable Base Vector Address
- Expandable to 64 Levels
- Programmable Interrupt Modes (Algorithms)
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- Full Compatibility with 8080A/8085A/8086/8088
- Available in 28 Pin Plastic and Ceramic Packages

PIN CONFIGURATION

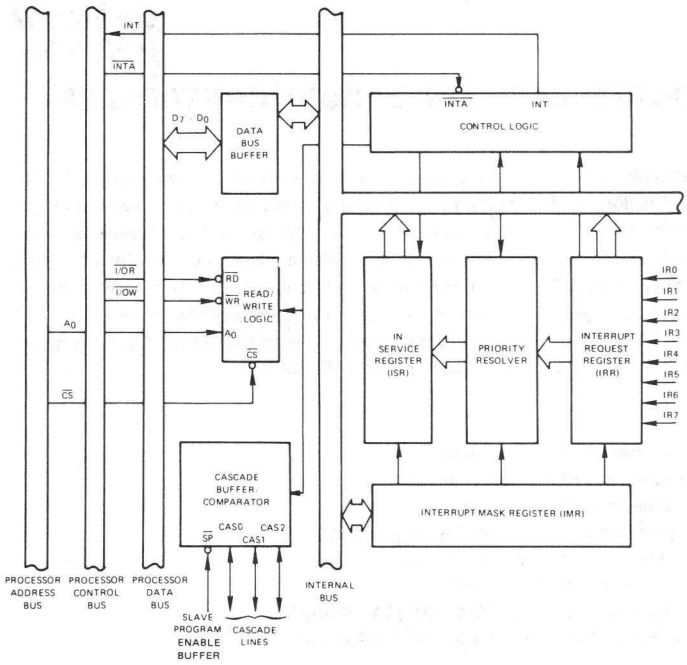


PIN NAMES

$D_7 - D_0$	Data Bus (Bi-Directional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Command Select Address
CAS2 – CAS0	Cascade Lines
$\overline{SP}/\overline{EN}$	Slave Program Input/ Enable Buffer
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0 – IR7	Interrupt Request Inputs
$\overline{CS}$	Chip Select

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5 to +7 Volts (1)
Power Dissipation	1W

Note: (1) With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5V	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -400 μA
Interrupt Output-High Voltage	V_{OH-INT}	2.4			V	I_{OH} = -400 μA
		3.5			V	I_{OH} = -50 μA
Input Leakage Current for IR_{0-7}	I_{IL} (IR_{0-7})			-300	μA	V_{IN} = 0V
				10	μA	$V_{IN} = V_{CC}$
Input Leakage Current for other Inputs	I_{IL}			10	μA	$V_{IN} = V_{CC}$ to 0V
Output Leakage Current	I_{LOL}			- 10	μA	V_{OUT} = 0.45 V
Output Leakage Current	I_{LOH}			10	μA	$V_{OUT} = V_{CC}$
V_{CC} Supply Current	I_{CC}			100	mA	

CAPACITANCE

$T_a = 25°C$; $V_{CC} = GND = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured Pins Returned to V_{SS}

AC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$ (μPD8259A)

PARAMETER	SYMBOL	μPD8259A MIN	μPD8259A MAX	μPD8259A-2 MIN	μPD8259A-2 MAX	UNIT	TEST CONDITIONS
AO/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$↓	t_{AHRL}	0		0		ns	
AO/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$↑	t_{RHAX}	0		0		ns	
$\overline{RD}$ Pulse Width	t_{RLRH}	235		160		ns	
AO/$\overline{CS}$ Setup to $\overline{WR}$↓	t_{AHWL}	0		0		ns	
AO/$\overline{CS}$ Hold after $\overline{WR}$↑	t_{WHAX}	0		0		ns	
$\overline{WR}$ Pulse Width	t_{WLWH}	290		190		ns	
Data Setup to $\overline{WR}$↑	t_{DVWH}	240		160		ns	
Data Hold after $\overline{WR}$↑	t_{WHDX}	0		0		ns	
Interrupt Request Width (Low)	t_{JLJH}	100		100		ns	①
Cascade Setup to Second or Third $\overline{INTA}$↓ (Slave Only)	t_{CVIAL}	55		40		ns	
End of $\overline{RD}$ to Next Command	t_{RHRL}	160		160		ns	
End of $\overline{WR}$ to Next Command	t_{WHRL}	190		190		ns	

Note: ① This is the low time required to clear the input latch in the edge triggered mode.

PARAMETER	SYMBOL	μPD8259A MIN	μPD8259A MAX	μPD8259A-2 MIN	μPD8259A-2 MAX	UNIT	TEST CONDITIONS
Data Valid from $\overline{RD}$/$\overline{INTA}$↓	t_{RLDV}		200		120	ns	C of Data Bus = 100 pF
Data Float after $\overline{RD}$/$\overline{INTA}$↑	t_{RHDZ}		100		85	ns	C of Data Bus Max Test C = 100 pF Min Test C = 15 pF
Interrupt Output Delay	t_{JHIH}		350		300	ns	
Cascade Valid from First $\overline{INTA}$↓ (Master Only)	t_{IAHCV}		565		360	ns	C_{INT} = 100 pF
Enable Active from $\overline{RD}$↓ or $\overline{INTA}$↓	t_{RLEL}		125		100	ns	$C_{CASCADE}$ = 100 pF
Enable Inactive from $\overline{RD}$↑ or $\overline{INTA}$↑	t_{RHEH}		150		150	ns	
Data Valid from Stable Address	t_{AHDV}		200		200	ns	
Cascade Valid to Valid Data	t_{CVDV}		300		200	ns	

FUNCTIONAL DESCRIPTION

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupt request register and in-service register store the in-coming interrupt request signals appearing on the IR0-7 lines (refer to functional block diagram). The inputs requesting service are stored in the IRR while the interrupts actually being serviced are stored in the ISR.

A positive transition on an IR input sets the corresponding bit in the Interrupt Request Register, and at the same time the INT output of the μPD8259 is set high. The IR input line must remain high until the first $\overline{\text{INTA}}$ input has been received. Multiple, non-masked interrupts occurring simultaneously can be stored in the IRR. The incoming $\overline{\text{INTA}}$ sets the appropriate ISR bit (determined by the programmed interrupt algorithm) and resets the corresponding IRR bit. The ISR bit stays high-active during the interrupt service subroutine until it is reset by the programmed End-of-Interrupt (EOI) command.

PRIORITY RESOLVER

The priority resolver decides the priority of the interrupt levels in the IRR. When the highest priority interrupt is determined it is loaded into the appropriate bit of the In-Service register by the first $\overline{\text{INTA}}$ pulse.

DATA BUS BUFFER

The 3-state, 8-bit, bi-directional data bus buffer interfaces the μPD8259 to the processor's system bus. It buffers the Control Word and Status Data transfers between the μPD8259 and the processor bus.

READ/WRITE LOGIC

The read/write logic accepts processor data and stores it in its Initialization Command Word (ICW) and Operation Command Word (OCW) registers. It also controls the transfer of the Status Data to the processor's data bus.

CHIP SELECT ($\overline{\text{CS}}$)

The μPD8259 is enabled when an active-low signal is received at this input. Reading or writing of the μPD8259 is inhibited when it is not selected.

WRITE ($\overline{\text{WR}}$)

This active-low signal instructs the μPD8259 to receive Command Data from the processor.

READ ($\overline{\text{RD}}$)

When an active-low signal is received on the $\overline{\text{RD}}$ input, the status of the Interrupt Request Register, In-Service Register, Interrupt Mask Register or binary code of the Interrupt Level is placed on the data bus.

INTERRUPT (INT)

The interrupt output from the μPD8259 is directly connected to the processor's INT input. The voltage levels of this output are compatible with the 8080A/8085A/8086/8088.

INTERRUPT MASK REGISTER (IMR)

The interrupt mask register stores the bits for the individual interrupt bits to be masked. The IMR masks the data in the ISR. Lower priority lines are not affected by masking a higher priority line.

FUNCTIONAL DESCRIPTION (CONT.)

INTERRUPT ACKNOWLEDGE ($\overline{INTA}$)

$\overline{INTA}$ pulses cause the μPD8259A to put vectoring information on the bus. The number of pulses depends upon whether the μPD8259A is in μPD8085A mode or 8086/8088 mode.

A_0

A_0 is usually connected to the processor's address bus. Together with $\overline{WR}$ and $\overline{RD}$ signals it directs the loading of data into the command register or the reading of status data. The following table illustrates the basic operations performed. Note that it is divided into three functions: Input, Output and Bus Disable distinguished by the $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ inputs.

μPD8259A BASIC OPERATION						
A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	PROCESSOR INPUT OPERATION (READ)
0			0	1	0	IRR, ISR or IR → Data Bus ①
1			0	1	0	IMR → Data Bus
						PROCESSOR OUTPUT OPERATION (WRITE)
0	0	0	1	0	0	Data Bus → OCW2
0	0	1	1	0	0	Data Bus → OCW3
0	1	X	1	0	0	Data Bus → ICW1
1	X	X	1	0	0	Data Bus → OCW1, ICW2, ICW3 ②
						DISABLE FUNCTION
X	X	X	1	1	0	Data Bus → 3-State
X	X	X	X	X	1	Data Bus → 3-State

Notes: ① The contents of OCW2 written prior to the READ operation governs the selection of the IRR, ISR or Interrupt Level.

② The sequencer logic on the μPD8259A aligns these commands in the proper order.

CASCADE BUFFER/COMPARATOR. (For Use in Multiple μPD8259 Array.)

The ID's of all μPD8259A's are buffered and compared in the cascade buffer/comparator. The master μPD8259A sends the ID of the interrupting slave device along the CAS0, 1, 2 lines to all slave devices. The cascade buffer/comparator compares its preprogrammed ID to the CAS0, 1, 2 lines. The next two $\overline{INTA}$ pulses strobe the preprogrammed, 2 byte CALL routine address onto the data bus from the slave whose ID matches the code on the CAS0, 1, 2 lines.

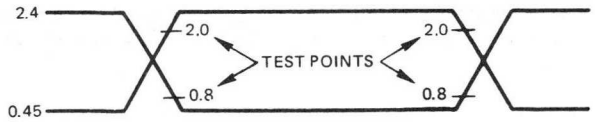
SLAVE PROGRAM ($\overline{SP}$). (For Use in Multiple μPD8259A Array.)

The interrupt capability can be expanded to 64 levels by cascading multiple μPD8259A's in a master-plus-slaves array. The master controls the slaves through the CAS0, 1, 2 lines. The $\overline{SP}$ input to the device selects the CAS0-2 lines as either outputs ($\overline{SP}$=1) for the master or as inputs ($\overline{SP}$=0) for the slaves. For one device only the $\overline{SP}$ must be set to a logic "1" since it is functioning as a master.

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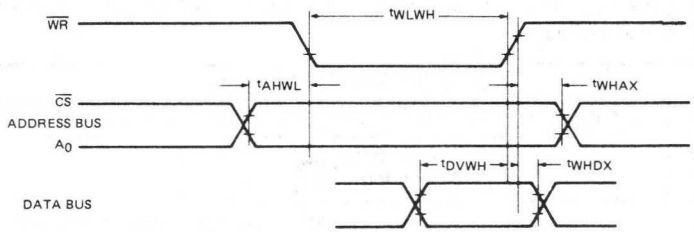
AC CHARACTERISTICS (CONT.)

INPUT WAVEFORMS FOR AC TESTS

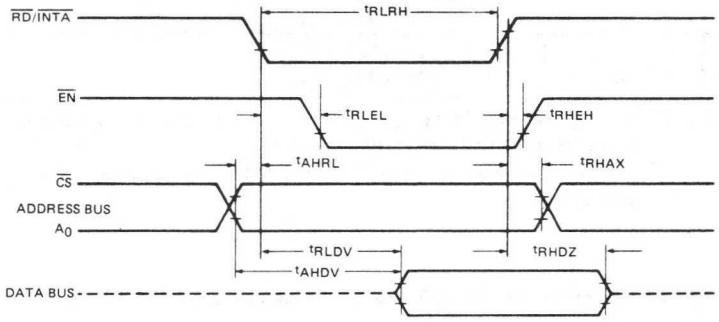


TIMING WAVEFORMS

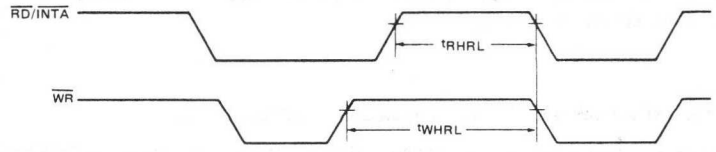
WRITE MODE



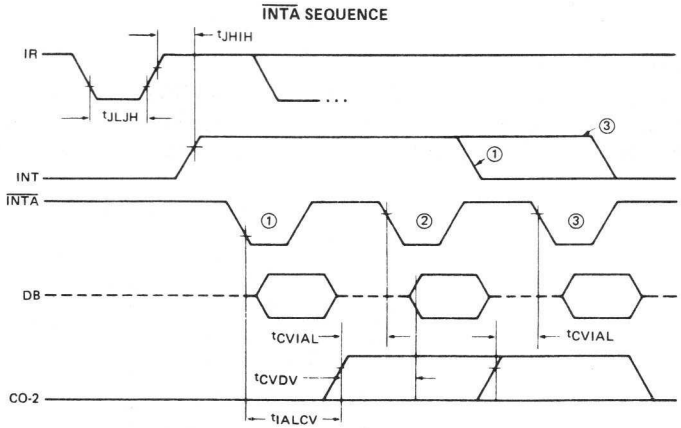
READ/INTA MODE



OTHER TIMING



TIMING WAVEFORMS (CONT.)



DETAILED OPERATIONAL DESCRIPTION

The sequence used by the μPD8259A to handle an interrupt depends upon whether an 8080A/8085A or 8086/8088 CPU is being used.

The following sequence applies to 8080A/8085A systems:

The μPD8259A derives its versatility from programmable interrupt modes and the ability to jump to any memory address through programmable CALL instructions. The following sequence demonstrates how the μPD8259A interacts with the processor.

1. An interrupt or interrupts appearing on IR_{0-7} sets the corresponding IR bit(s) high. This in turn sets the corresponding IRR bit(s) high.
2. Once the IRR bit(s) has been set, the μPD8259A will resolve the priorities according to the preprogrammed interrupt algorithm. It then issues an INT signal to the processor.
3. The processor group issues an $\overline{INTA}$ to the μPD8259A when it receives the INT.
4. The $\overline{INTA}$ input to the μPD8259A from the processor group sets the highest priority ISR bit and resets the corresponding IRR bit. The $\overline{INTA}$ also signals the μPD8259A to issue an 8-bit CALL instruction op-code (11001101) onto its Data bus lines.
5. The CALL instruction code instructs the processor group to issue two more $\overline{INTA}$ pulses to the μPD8259A.
6. The two $\overline{INTA}$ pulses signal the μPD8259A to place its preprogrammed interrupt vector address onto the Data bus. The first $\overline{INTA}$ releases the low-order 8-bits of the address and the second $\overline{INTA}$ releases the high-order 8-bits.
7. The μPD8259A's CALL instruction sequence is complete. A preprogrammed EOI (End-of-Interrupt) command is issued to the μPD8259A at the end of an interrupt service routine to reset the ISR bit and allow the μPD8259A to service the next interrupt.

For 8086/8088 systems the first three steps are the same as described above, then the following sequence occurs:

4. During the first $\overline{INTA}$ from the processor, the μPD8259A does not drive the data bus. The highest priority ISR bit is set and the corresponding IRR bit is reset.
5. The μPD8259A puts vector onto the data bus on the second $\overline{INTA}$ pulse from the 8086/8088.
6. There is no third $\overline{INTA}$ pulse in this mode. In the AEOI mode the ISR bit is reset at the end of the second $\overline{INTA}$ pulse, or it remains set until an EOI command is issued.

8080A/8085A MODE

INTERRUPT SEQUENCE

For these processors, the μPD8259A is controlled by three $\overline{\text{INTA}}$ pulses. The first $\overline{\text{INTA}}$ pulse will cause the μPD8259A to put the CALL op-code onto the data bus. The second and third $\overline{\text{INTA}}$ pulses will cause the upper and lower address of the interrupt vector to be released on the bus.

FIRST $\overline{\text{INTA}}$

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

SECOND $\overline{\text{INTA}}$

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

THIRD $\overline{\text{INTA}}$

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

In this mode only two $\overline{\text{INTA}}$ pulses are sent to the μPD8259A. After the first $\overline{\text{INTA}}$ pulse, the μPD8259A does not output a CALL but internally sets priority resolution. If it is a master, it sets the cascade lines. The interrupt vector is output to the data bus on the second $\overline{\text{INTA}}$ pulse.

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

INITIALIZATION COMMAND WORDS

ICW1 AND ICW2

A_5-A_{15}. *Page starting address of service routines.* In an 8085A system, the 8 request levels generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the μPD8259A, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the μPD8259A, while A_6-A_{15} are programmed externally.

The 8-byte interval maintains compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an MCS-86 system, T7-T3 are inserted in the five most significant bits of the vectoring byte and the μPD8259A sets the three least significant bits according to the interrupt level. A_{10}-A_5 are ignored and ADI (Address Interval) has no effect.

LTIM: If LTIM = 1, then the μPD8259A operates in the level interrupt mode. Edge detect logic on the interrupt inputs is disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only μPD8259A in the system. If SNGL = 1 no ICW3 is issued.

IC4: If this bit is set – ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

ICW3

This word is read only when there is more than one μPD8259A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then releases byte 1 of the call sequence (for 8085A system) and enables the corresponding slave to release bytes 2 and 3 (for 8086/8088 only byte 2) through the cascade lines.

b. In the slave mode (either when SP = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and if they are equal, bytes 2 and 3 of the CALL sequence (or just byte 2 for 8086/8088) are released by it on the Data Bus.

ICW4

SFNM: If SFNM = 1 the special fully nested mode is programmed.

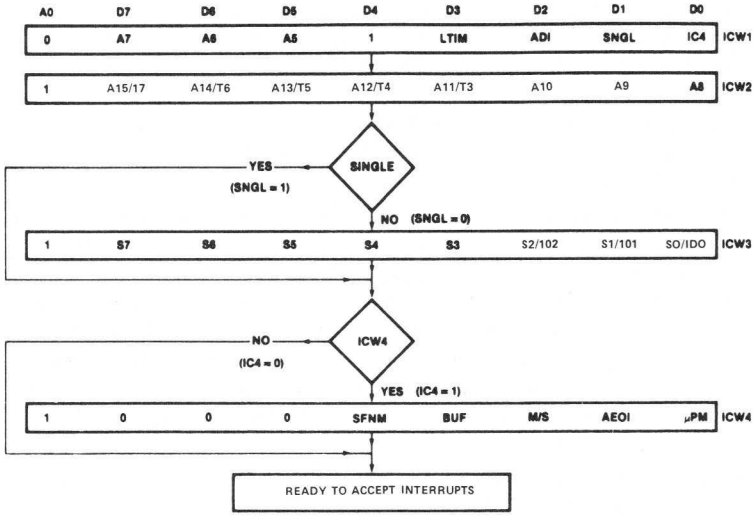
BUF: If BUF = 1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the μPD8259A is programmed to be a master, M/S = 0 means the μPD8259A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the μPD8259A for 8085A system operation, μPM = 1 sets the μPD8259A for 8086 system operation.

INITIALIZATION SEQUENCE



OPPERATIONAL COMMAND WORDS (OCW's) ②

Once the μPD8259A has been programmed with Initialization Command Words, it can be programmed for the appropriate interrupt algorithm by the Operation Command Words. Interrupt algorithms in the μPD8259A can be changed at any time during program operation by issuing another set of Operation Command Words. The following sections describe the various algorithms available and their associated OCWs.

INTERRUPT MASKS

The individual Interrupt Request input lines are maskable by setting the corresponding bits in the Interrupt Mask Register to a logic "1" through OCW1. The actual masking is performed upon the contents of the In-Service Register (e.g., if Interrupt Request line 3 is to be masked, then only bit 3 of the IMR is set to logic "1." The IMR in turn acts upon the contents of the ISR to mask bit 3). Once the μPD8259A has acknowledged an interrupt, i.e., the μPD8259A has sent an INT signal to the processor and the system controller has sent it an $\overline{\text{INTA}}$ signal, the interrupt input, although it is masked, inhibits lower priority requests from being acknowledged. There are two means of enabling these lower priority interrupt lines. The first is by issuing an End-of-Interrupt (EOI) through Operation Command Word 2 (OCW2), thereby resetting the appropriate ISR bit. The second approach is to select the Special Mask Mode through OCW3. The Special Mask Mode (SMM) and End-of-Interrupt (EOI) will be described in more detail further on.

FULLY NESTED MODE

The fully nested mode is the μPD8259A's basic operating mode. It will operate in this mode after the initialization sequence, without requiring Operation Command Words for formatting. Priorities are set IR_0 through IR_7, with IR_0 the highest priority. After the interrupt has been acknowledged by the processor and system controller, only higher priorities will be serviced. Upon receiving an INTA, the priority resolver determines the priority of the interrupt, sets the corresponding IR bit, and outputs the vector address to the Data bus. The EOI command resets the corresponding ISR bits at the end of its service routines.

Notes: ① Reference Figure 2
② Reference Figure 3

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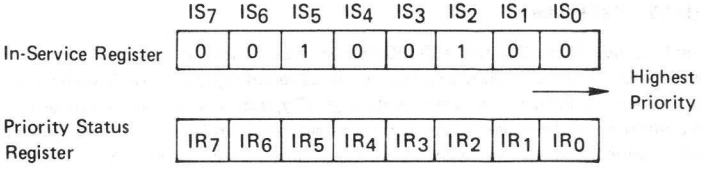
ROTATING PRIORITY MODE COMMANDS

The two variations of Rotating Priorities are the Auto Rotate and Specific Rotate modes. These two modes are typically used to service interrupting devices of equivalent priorities.

1. Auto Rotate Mode

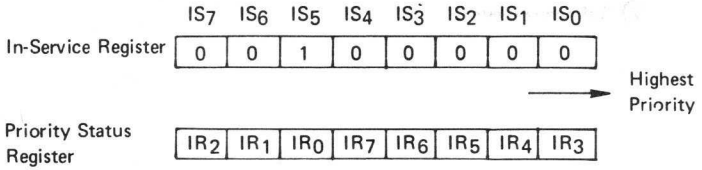
   Programming the Auto Rotate Mode through OCW2 assigns priorities 0-7 to the interrupt request input lines. Interrupt line IR_0 is set to the highest priority and IR_7 to the lowest. Once an interrupt has been serviced it is automatically assigned the lowest priority. That same input must then wait for the devices ahead of it to be serviced before it can be acknowledged again. The Auto Rotate Mode is selected by programming OCW2 in the following way (refer to Figure 3): set Rotate Priority bit "R" to a logic "1"; program EOI to a logic "1" and SEOI to a logic "0." The EOI and SEOI commands are discussed further on. The following is an example of the Auto Rotate Mode with devices requesting interrupts on lines IR_2 and IR_5.

   Before Interrupts are Serviced:



   According to the Priority Status Register, IR_2 has a higher priority than IR_5 and will be serviced first.

   After Servicing:



   At the completion of IR_2's service routine the corresponding In-Service Register bit, IS_2 is reset to "0" by the preprogrammed EOI command. IR_2 is then assigned the lowest priority level in the Priority Status Register. The μPD8259A is now ready to service the next highest interrupt, which in this case, is IR_5.

2. Specific Rotate Mode

   The priorities are set by programming the lowest level through OCW2. The μPD8259A then automatically assigns the highest priority. If, for example, IR_3 is set to the lowest priority (bits L_2, L_1, L_0 form the binary code of the bottom priority level), then IR_4 will be set to the highest priority. The Specific Rotate Mode is selected by programming OCW2 in the following manner: set Rotate Priority bit "R" to a logic "1," program EOI to a logic "0," SEOI to a logic "1" and L_2, L_1, L_0 to the lowest priority level. If EOI is set to a logic "1," the ISR bit defined by L_2, L_1, L_0 is reset.

OPERATIONAL COMMAND WORDS (CONT.)

END-OF-INTERRUPT (EOI) AND SPECIFIC END-OF-INTERRUPT (SEOI)

The End-of-Interrupt or Specific End-of-Interrupt command must be issued to reset the appropriate In-Service Register bit before the completion of a service routine. Once the ISR bit has been reset to logic "0," the μPD8259A is ready to service the next interrupt.

Two types of EOIs are available to clear the appropriate ISR bit depending on the μPD8259A's operating mode.

1. Non-Specific End-of-Interrupt (EOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is preserved (e.g., fully nested mode), the particular ISR bit to be reset at the completion of the service routine can be determined. A non-specific EOI command automatically resets the highest priority ISR bit of those set. The highest priority ISR bit must necessarily be the interrupt being serviced and must necessarily be the service subroutine returned from.

2. Specific End-of-Interrupt (SEOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is not preserved (e.g., rotating priority mode) the last serviced interrupt level may not be known. In these modes a Specific End-of-Interrupt must be issued to clear the ISR bit at the completion of the interrupt service routine. The SEOI is programmed by setting the appropriate bits in OCW3 (Figure 2) to logic "1"s. Both the EOI and SEOI bits of OCW3 must be set to a logic "1" with L_2, L_1, L_0 forming the binary code of the ISR bit to be reset.

SPECIAL MASK MODE

Setting up an interrupt mask through the Interrupt Mask Register (refer to Interrupt Mask Register section) by setting the appropriate bits in OCW1 to a logic "1" inhibits lower priority interrupts from being acknowledged. In applications requiring that the lower priorities be enabled while the IMR is set, the Special Mask Mode can be used. The SMM is programmed in OCW3 by setting the appropriate bits to a logic "1." Once the SMM is set, the μPD8259A remains in this mode until it is reset. The Special Mask Mode does not affect the higher priority interrupts.

POLLED MODE

In Poll Mode the processor must be instructed to disable its interrupt input (INT). Interrupt service is initiated through software by a Poll Command. Poll Mode is programmed by setting the Poll Mode bit in OCW3 (P = 1), during a $\overline{WR}$ pulse. The following $\overline{RD}$ pulse is then considered as an interrupt acknowledge. If an interrupt input is present, that $\overline{RD}$ pulse sets the appropriate ISR bit and reads the interrupt priority level. Poll Mode is a one-time operation and must be programmed through OCW3 before every read. The word strobed onto the Data bus during Poll Mode is of the form:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I	X	X	X	X	W_2	W_1	W_0

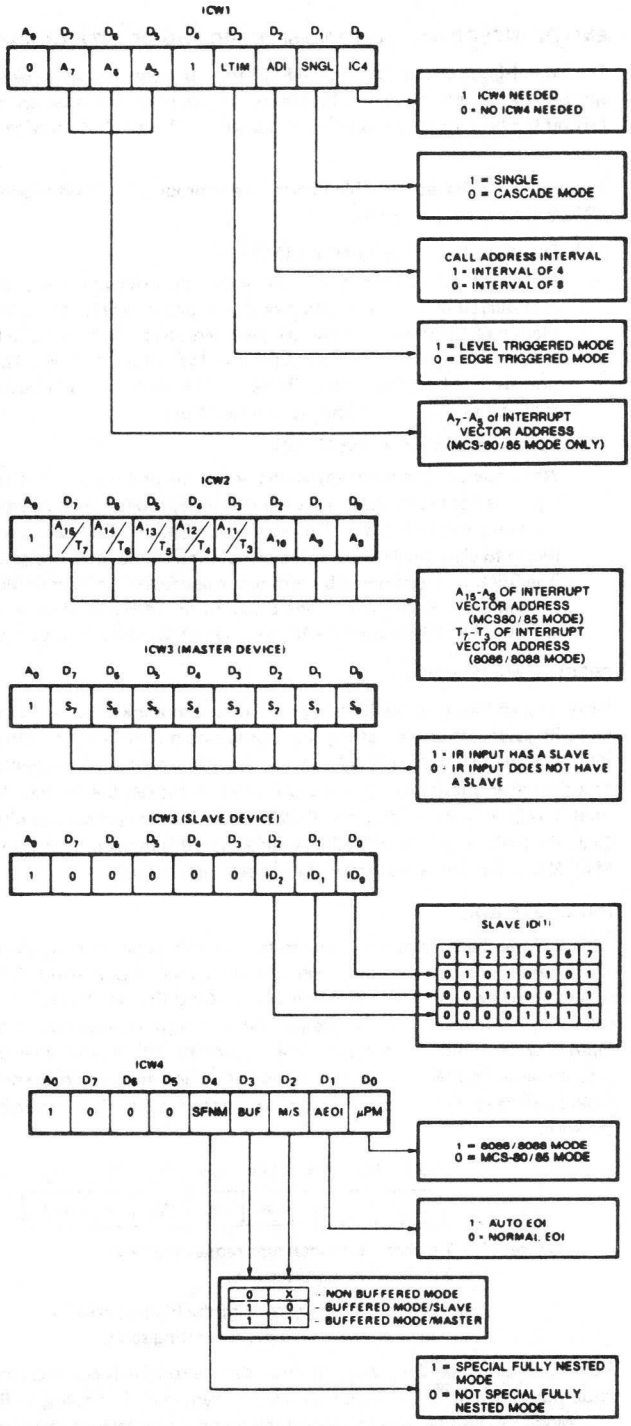
where: I = 1 if there is an interrupt requesting service
= 0 if there are no interrupts

$W_{2\text{-}0}$ forms the binary code of the highest priority level of the interrupts requesting service

Poll Mode can be used when an interrupt service routine is common to several interrupt inputs. The $\overline{INTA}$ sequence is no longer required, thus saving in ROM space. Poll Mode can also be used to expand the number of interrupts beyond 64.

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INITIALIZATION COMMAND WORD FORMAT



NOTE 1: SLAVE ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT.

READING μPD8259 STATUS

The following major registers' status is available to the processor by appropriately formatting OCW3 and issuing $\overline{RD}$ command.

INTERRUPT REQUEST REGISTER (8-BITS)

The Interrupt Request Register stores the interrupt levels awaiting acknowledgement. The highest priority in-service bit is reset once it has been acknowledged. (Note that the Interrupt Mask Register has no effect on the IRR.) A WR command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. The bits which determine whether the IRR and ISR are being read from are RIS and ERIS. To read contents of the IRR, ERIS must be logic "1" and RIS a logic "0."

IN-SERVICE REGISTER (8-BITS)

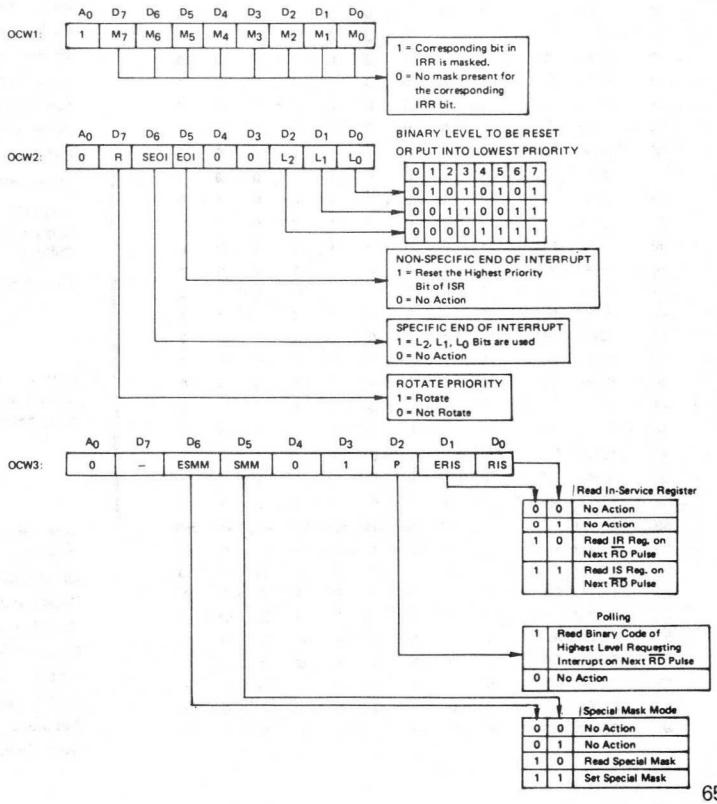
The In-Service Register stores the priorities of the interrupt levels being serviced. Assertion of an End-of-Interrupt (EOI) updates the ISR to the next priority level. A $\overline{WR}$ command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. Both ERIS and RIS should be set to a logic "1."

INTERRUPT MASK REGISTER (8-BITS)

The Interrupt Mask Register holds mask data modifying interrupt levels. To read the IMR status a $\overline{WR}$ pulse preceding the $\overline{RD}$ is not necessary. The IMR data is available to the data bus when $\overline{RD}$ is asserted with A_0 at a logic "1."

A single OCW3 is sufficient to enable successive status reads providing it is of the same register. A status read is over-ridden by the Poll Mode when bits P and ERIS of OCW3 are set to a logic "1."

OPERATION COMMAND WORD FORMAT



SUMMARY OF 8259A INSTRUCTION SET

Inst. #	Mnemonic		A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation Description	
1	ICW1	A	0	A7	A6	A5	1	0	1	1	0		Format = 4, single, edge triggered
2	ICW1	B	0	A7	A6	A5	1	1	1	1	0		Format = 4, single, level triggered
3	ICW1	C	0	A7	A6	A5	1	0	1	0	0	Byte 1 Initialization	Format = 4, not single, edge triggered
4	ICW1	D	0	A7	A6	A5	1	1	1	0	0		Format = 4, not single, level triggered
5	ICW1	E	0	A7	A6	0	1	0	0	1	0	No ICW4 Required	Format = 8, single, edge triggered
6	ICW1	F	0	A7	A6	0	1	1	0	1	0		Format = 8, single, level triggered
7	ICW1	G	0	A7	A6	0	1	0	0	0	0		Format = 8, not single, edge triggered
8	ICW1	H	0	A7	A6	0	1	1	0	0	0		Format = 8, not single, level triggered
9	ICW1	I	0	A7	A6	A5	1	0	1	1	1		Format = 4, single, edge triggered
10	ICW1	J	0	A7	A6	A5	1	1	1	1	1		Format = 4, single, level triggered
11	ICW1	K	0	A7	A6	A5	1	0	1	0	1	Byte 1 Initialization	Format = 4, not single, edge triggered
12	ICW1	L	0	A7	A6	A5	1	1	1	0	1		Format = 4, not single, level triggered
13	ICW1	M	0	A7	A6	0	1	0	0	1	1	ICW4 Required	Format = 8, single, edge triggered
14	ICW1	N	0	A7	A6	0	1	1	0	1	1		Format = 8, single, level triggered
15	ICW1	O	0	A7	A6	0	1	0	0	0	1		Format = 8, not single, edge triggered
16	ICW1	P	0	A7	A6	0	1	1	0	0	1		Format = 8, not single, level triggered
17	ICW2		1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization	
18	ICW3	M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization — master	
19	ICW3	S	1	0	0	0	0	0	S2	S1	S0	Byte 3 initialization — slave	
20	ICW4	A	1	0	0	0	0	0	0	0	0	No action, redundant	
21	ICW4	B	1	0	0	0	0	0	0	0	1	Non-buffered mode, no AEOI, 8086/8088	
22	ICW4	C	1	0	0	0	0	0	0	1	0	Non-buffered mode, AEOI, 80/85	
23	ICW4	D	1	0	0	0	0	0	0	1	1	Non-buffered mode, AEOI, 8086/8088	
24	ICW4	E	1	0	0	0	0	0	1	0	0	No action, redundant	
25	ICW4	F	1	0	0	0	0	0	1	0	1	Non-buffered mode, no AEOI, 8086/8088	
26	ICW4	G	1	0	0	0	0	0	1	1	0	Non-buffered mode, AEOI, 80/85	
27	ICW4	H	1	0	0	0	0	0	1	1	1	Non-buffered mode, AEOI, 8086/8088	
28	ICW4	I	1	0	0	0	0	1	0	0	0	Buffered mode, slave, no AEOI, 80/85	
29	ICW4	J	1	0	0	0	0	1	0	0	1	Buffered mode, slave, no AEOI, 8086/8088	
30	ICW4	K	1	0	0	0	0	1	0	1	0	Buffered mode, slave, AEOI, 80/85	
31	ICW4	L	1	0	0	0	0	1	0	1	1	Buffered mode, slave, AEOI, 8086/8088	
32	ICW4	M	1	0	0	0	0	1	1	0	0	Buffered mode, master, no AEOI, 80/85	
33	ICW4	N	1	0	0	0	0	1	1	0	1	Buffered mode, master, no AEOI, 8086/8088	
34	ICW4	O	1	0	0	0	0	1	1	1	0	Buffered mode, master, AEOI, 80/85	
35	ICW4	P	1	0	0	0	0	1	1	1	1	Buffered mode, master AEOI, 8086, 8088	
36	ICW4	NA	1	0	0	0	1	0	0	0	0		
37	ICW4	NB	1	0	0	0	1	0	0	0	1	Fully nested mode, 8085A, non-buffered, no AEOI	
38	ICW4	NC	1	0	0	0	1	0	0	1	0	ICW4 NB through ICW4 ND are identical to	
39	ICW4	ND	1	0	0	0	1	0	0	1	1	ICW4 B through ICW4 D with the addition of	
40	ICW4	NE	1	0	0	0	1	0	1	0	0	Fully Nested Mode	
41	ICW4	NF	1	0	0	0	1	0	1	0	1	Fully Nested Mode, 80/85, non-buffered, no AEOI	
42	ICW4	NG	1	0	0	0	1	0	1	1	0		
43	ICW4	NH	1	0	0	0	1	0	1	1	1		
44	ICW4	NI	1	0	0	0	1	1	0	0	0		
45	ICW4	NJ	1	0	0	0	1	1	0	0	1		
46	ICW4	NK	1	0	0	0	1	1	0	1	0	ICW4 NF through ICW4 NP are identical to	
47	ICW4	NL	1	0	0	0	1	1	0	1	1	ICW4 F through ICW4 P with the addition of	
48	ICW4	NM	1	0	0	0	1	1	1	0	0	Fully Nested Mode	
49	ICW4	NN	1	0	0	0	1	1	1	0	1		
50	ICW4	NO	1	0	0	0	1	1	1	1	0		
51	ICW4	NP	1	0	0	0	1	1	1	1	1		
52	OCW1		1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask register, read mark register	
53	OCW2	E	0	0	0	1	0	0	0	0	0	Non-specific EOI	
54	OCW2	SE	0	0	1	1	0	0	L2	L1	L0	Specific EOI, L0-L2 code of IS FF to be reset	
55	OCW2	RE	0	1	0	1	0	0	0	0	0	Rotate on Non-Specific EOI	
56	OCW2	RSE	0	1	1	1	0	0	L2	L1	L0	Rotate on Specific EOI L0-L2 code of line	
57	OCW2	R	0	1	0	0	0	0	0	0	0	Rotate in Auto EOI (set)	
58	OCW2	CR	0	0	0	0	0	0	0	0	0	Rotate in Auto EOI (clear)	
59	OCW2	RS	0	1	1	0	0	0	L2	L1	L0	Set Priority Command	
60	OCW3	P	0	0	0	0	0	1	1	0	0	Poll mode	
61	OCW3	RIS	0	0	0	0	0	1	0	1	1	Read IS register	

SUMMARY OF OPERATION COMMAND WORD PROGRAMMING

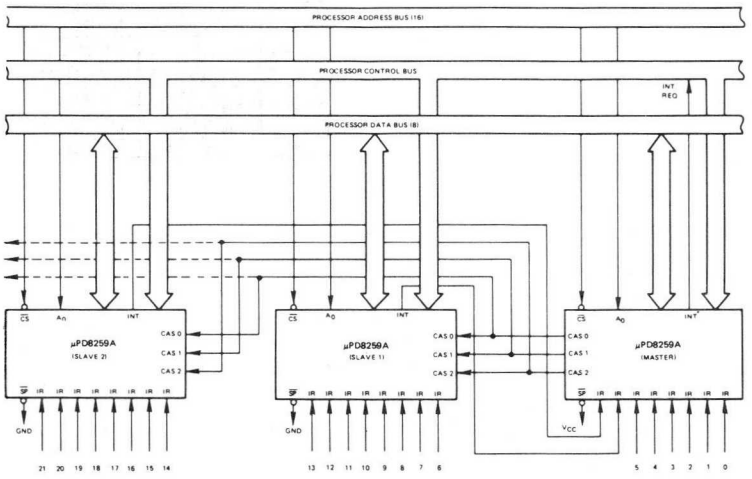
	A_0	D_4	D_3				
OCW1	1	X	X	M_7-M_0			IMR (Interrupt Mask Register) $\overline{WR}$ loads IMR data while $\overline{RD}$ reads status
OCW2	0	0	0	R	SEOI	EOI	
				0	0	0	No Action
				0	0	1	Non-Specific End-of-Interrupt
				0	1	0	No Action
				0	1	1	Specific-End-of-Interrupt L_2, L_1, L_0 forms binary representation of level to be reset.
				1	0	0	No Action
				1	0	1	Rotate Priority at End-of-Interrupt (Auto Mode)
				1	1	0	Rotate Priority, L_2, L_1, L_0 specifies bottom priority without End-of-Interrupt
				1	1	1	Rotate Priority at End-of-Interrupt (Specific Mode). L_2, L_1, L_0 specifies bottom priority, and its In-Service Register bit is reset.
OCW3	0	0	1	ESMM	SMM		
				0	0		Special Mask not affected
				0	1		
				1	0		Reset Special Mask
				1	1		Set Special Mask
				ERIS	RIS		
				0	0		No Action
				0	1		
				1	0		Read IR Register Status
				1	1		Read IS Register Status

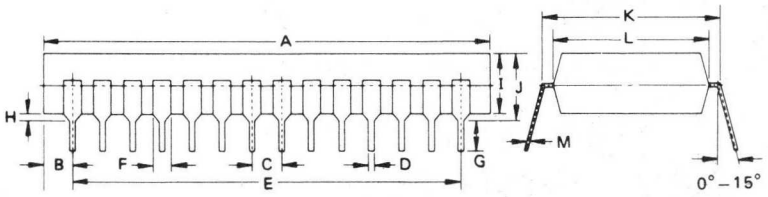
LOWER MEMORY INTERRUPT VECTOR ADDRESS

	INTERVAL = 4								INTERVAL = 8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_7	A_7	A_6	A_5	1	1	1	0	0	A_7	A_6	1	1	1	0	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0	A_7	A_6	1	1	0	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0	A_7	A_6	1	0	1	0	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0	A_7	A_6	1	0	0	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0	A_7	A_6	0	1	1	0	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0	A_7	A_6	0	1	0	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0	A_7	A_6	0	0	1	0	0	0
IR_0	A_7	A_6	A_5	0	0	0	0	0	A_7	A_6	0	0	0	0	0	0

FIGURE 4

Note: Insure that the processor's interrupt input is disabled during the execution of any control command and initialization sequence for all μPD8259As.

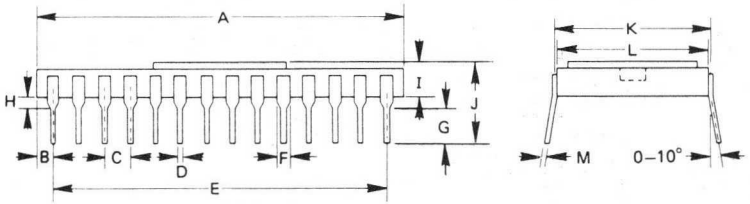




PACKAGE OUTLINE
μPD8259AC

(Plastic)

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$



μPD8259AD

(Ceramic)

ITEM	MILLIMETERS	INCHES
A	36.2 MAX.	1.43 MAX.
B	1.59 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.46 ± 0.01	0.02 ± 0.004
E	33.02 ± 0.1	1.3 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.002

PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

DESCRIPTION

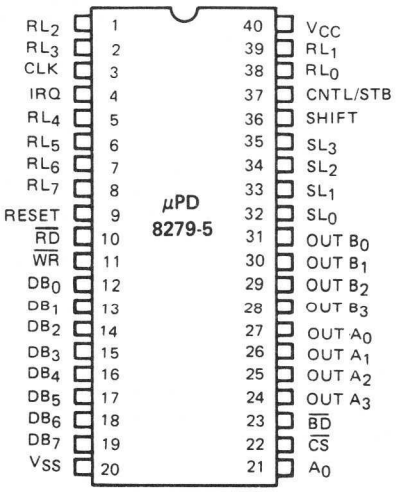
The μPD8279-5 is a programmable keyboard and display Input/Output device. It provides the user with the ability to display data on alphanumeric segment displays or simple indicators. The display RAM can be programmed as 16 x 8 or a dual 16 x 4 and loaded or read by the host processor. The display can be loaded with right or left entry with an auto-increment of the display RAM address.

The keyboard interface provides a scanned signal to a 64 contact key matrix expandable to 128. General sensors or strobed keys may also be used. Keystrokes are stored in an 8 character FIFO and can be either 2 key lockout or N key rollover. Keyboard entries generate an interrupt to the processor.

FEATURES

- Programmable by Processor
- 32 HEX or 16 Alphanumeric Displays
- 64 Expandable to 128 Keyboard
- Simultaneous Keyboard and Display
- 8 Character Keyboard – FIFO
- 2 Key Lockout or N Key Rollover
- Contact Debounce
- Programmable Scan Timer
- Interrupt on Key Entry
- Single +5 Volt Supply, ±10%
- Fully Compatible with 8080A, 8085A, μPD780 (Z80™)
- Available in 40 Pin Plastic Package

PIN CONFIGURATION



PIN NAMES

DB_{0-7}	Data Bus (Bi-directional)
CLK	Clock Input
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Buffer Address
IRQ	Interrupt Request Output
SL_{0-3}	Scan Lines
RL_{0-7}	Return Lines
SHIFT	Shift Input
CNTL/STB	Control/Strobe Input
OUT A_{0-3}	Display (A) Outputs
OUT B_{0-3}	Display (B) Outputs
$\overline{BD}$	Bland Display Output

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TM: Z80 is a registered trademark of Zilog.

μPD8279-5

FUNCTIONAL DESCRIPTION

The μPD8279-5 has two basic functions: 1) to control displays to output and 2) to control a keyboard for input. Its specific purpose is to unburden the host processor from monitoring keys and refreshing displays. The μPD8279-5 is designed to directly interface the microprocessor bus. The microprocessor must program the operating mode to the μPD8279-5, these modes are as follows:

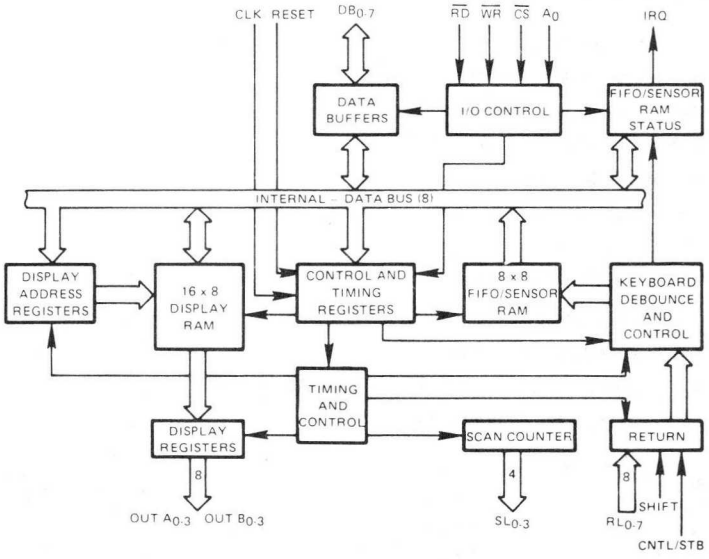
Output Modes

- 8 or 16 Character Display
- Right or Left Entry

Input Modes

- Scanned Keyboard with Encoded 8 x 8 x 4 Key Format or Decoded 4 x 8 x 8 Scan Lines.
- Scanned Sensor Matrix with Encoded 8 x 8 or Decoded 4 x 8 Scan Lines.
- Strobed Input.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages	-0.5 to +7 Volts①
All Input Voltages	-0.5 to +7 Volts①
Supply Voltages	-0.5 to +7 Volts①
Power Dissipation	1W

Note: ① With respect to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

PIN IDENTIFICATION

PIN			DESCRIPTION
NO.	SYMBOL	NAME	
1, 2, 5, 6, 7, 8, 38, 39	RL_{0-7}	Return Lines	Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.
3	CLK	Clock	Clock from system used to generate internal timing.
4	IRQ	Interrupt Request	Interrupt Request. In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
9	Reset	Reset Input	A high signal on this pin resets the μPD8279-5.
10	$\overline{RD}$	Read Input	Input/Output read and write. These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
11	$\overline{WR}$	Write Input	
12-19	DB_{0-7}	Data Bus	Bi-Directional data bus. All data and commands between the processor and the μPD8279-5 are transmitted on these lines.
20	V_{SS}	Ground Reference	Power Supply Ground
21	A_0	Buffer Address	Buffer Address. A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data.
22	$\overline{CS}$	Chip Select	Chip Select. A low on this pin enables the interface functions to receive or transmit.
23	$\overline{BD}$	Blank Display Output	Blank Display. This output is used to blank the display during digit switching or by a display blanking command.
24-27	OUT A_{0-3}	Display A Outputs	These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL_0-SL_3) for multiplexed digit displays. The two 4-bit ports may be blanked independently. These two ports may also be considered as one 8-bit port.
28-31	OUT B_{0-3}	Display B Outputs	
32-35	SL_{0-3}	Scan Lines	Scan Lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
36	Shift	Shift Input	The shift input status is stored along with the key position on key closure in the Scanned Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low.
37	CNTL/STB	Control/ Strobe Input	For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in Strobed input mode (Rising Edge). It has an active internal pullup to keep it high until a switch closure pulls it low.
40	V_{CC}	+5V Input	Power Supply Input

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$; $V_{SS} = 0V$.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage for Shift, Control and Return Lines	V_{IL1}	-0.5		1.4	V	
Input Low Voltage (Others)	V_{IL2}	-0.5		0.8	V	
Input High Voltage for Shift, Control and Return Lines	V_{IH1}	2.2			V	
Input High Voltage (Others)	V_{IH2}	2.0			V	
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 2.2$ mA
Output High Voltage on Interrupt Line	V_{OH}	3.5			V	$I_{OH} = -400\ \mu A$
Input Current on Shift, Control and Return Lines	I_{IL1}			+10	μA	$V_{IN} = V_{CC}$
				-100	μA	$V_{IN} = 0V$
Input Leakage Current (Others)	I_{IL2}			±10	μA	$V_{IN} = V_{CC}$ to 0V
Output Float Leakage	I_{OFL}			±10	μA	$V_{OUT} = V_{CC}$ to 0V
Power Supply Current	I_{CC}			120	mA	

CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}	5		10	pF	$V_{IN} = V_{CC}$
Output Capacitance	C_{OUT}	10		20	pF	$V_{OUT} = V_{CC}$

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
READ						
Address Stable Before $\overline{READ}$	t_{AR}	0			ns	
Address Hold Time for $\overline{READ}$	t_{RA}	0			ns	
$\overline{READ}$ Pulse Width	t_{RR}	250			ns	
Data Delay from $\overline{READ}$	t_{RD}			150	ns	$C_L = 150$ pF
Address to Data Valid	t_{AD}			250	ns	$C_L = 150$ pF
$\overline{READ}$ to Data Floating	t_{DF}	10		100	ns	
Read Cycle Time	t_{RCY}	1			μs	
WRITE						
Address Stable Before $\overline{WRITE}$	t_{AW}	0			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	0			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	250			ns	
Data Set Up Time for $\overline{WRITE}$	t_{DW}	150			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	0			ns	
OTHER						
Clock Pulse Width	$t_{\phi W}$	120			ns	
Clock Period	t_{CY}	320			ns	

GENERAL TIMING

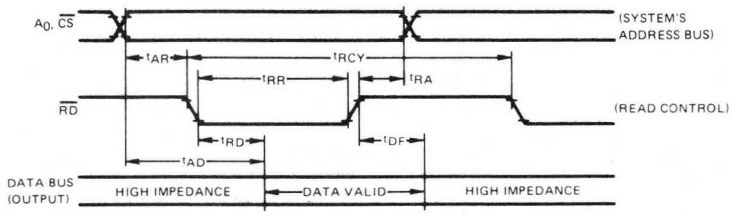
Keyboard Scan Time:	5.1 ms	Digit-on Time:	480 μs
Keyboard Debounce Time:	10.3 ms	Blanking Time:	160 μs
Key Scan Time:	80 μs	Internal Clock Cycle:	10 μs
Display Scan Time:	10.3 ms		

TIMING WAVEFORMS

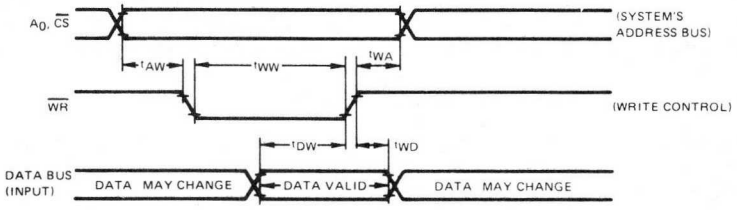
INPUT FOR AC TESTS



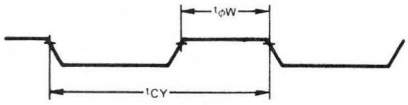
READ



WRITE



CLOCK INPUT



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OPERATIONAL DESCRIPTION

The following is a description of each section of the μPD8279-5. See the block diagram for functional reference.

I/O Control and Data Buffers

Communication to and from the μPD8279-5 is performed by selecting $\overline{CS}$, A_0, $\overline{RD}$ and $\overline{WR}$. The type of information written or read by the processor is selected by A_0. A logic 0 states that information is data while a 1 selects command or status. $\overline{RD}$ and $\overline{WR}$ select the direction by which the transfer occurs through the Data Buffers. When the chip is deselected ($\overline{CS}$ = 1) the bi-directional Data Buffers are in a high impedance state thus enabling the μPD8279-5 to be tied directly to the processor data bus.

Timing Registers and Timing Control

The Timing Registers store the display and keyboard modes and other conditions programmed by the processor. The timing control contains the timing counter chain. One counter is a divide by N scaler which may be programmed to match the processor cycle time. The scaler must take a value between 2 and 31 in binary. A value which scales the internal frequency to 100 KHz gives a 5.1 ms scan time and 10.3 ms switch debounce. The other counters divide down to make key, row matrix and display scans.

Scan Counter

The scan counter can operate in either the encoded or decoded mode. In the encoded mode, the counter provides a count which must be decoded to provide the scan lines. In the decoded mode, the counter provides a 1 out of 4 decoded scan. In the encoded mode the scan lines are active high and in the decoded mode they are active low.

Return Buffers, Keyboard Debounce and Control

The eight return lines are buffered and latched by the return buffers. In the keyboard mode these lines are scanned sampling for key closures in each row. If the debounce circuit senses a closure, about 10 ms are timed out and a check is performed again. If the switch is still pressed, the address of the switch matrix plus the status of shift and control are written into the FIFO. In the scanned sensor mode, the contents of return lines are sent directly to the sensor RAM (FIFO) each key scan. In the strobed mode, the transfer takes place on the rising edge of CNTL/STB.

FIFO/Sensor RAM and Status

This section is a dual purpose 8 x 8 RAM. In strobe or keyboard mode it is a FIFO. Each entry is pushed into the FIFO and read in order. Status keeps track of the number of entries in the FIFO. Too many reads or writes to the FIFO will be treated as an error condition. The status logic generates an IRQ whenever the FIFO has an entry. In the sensor mode the memory is a sensor RAM which detects changes in the status of a sensor. If a change occurs, the IRQ is generated until the change is acknowledged.

Display Address Registers and Display RAM

The Display Address Register contains the address of the word being read or written by the processor, as well as the word being displayed. This address may be programmed to auto-increment after each read or write. The display RAM may be read by the processor any time after the mode and address is set. Data entry to the display RAM may be set to either right or left entry.

COMMAND OPERATION

The commands programmable to the μPD8279-5 via the data bus with $\overline{CS}$ active (0) and A_0 high are as follows:

Keyboard/Display Mode Set

0	0	0	D	D	K	K	K

MSB LSB

Display Mode:

DD

0	0	8-8-bit character display – Left entry
0	1 ①	16-8 bit character display – Left entry
1	0	8-8 bit character display – Right entry
1	1	16-8 bit character display – Right entry

Note: ① Power on default condition

Keyboard Mode:

KKK

0	0	0	Encoded Scan – 2 Key Lockout
0	0	1	Decoded Scan – 2 Key Lockout
0	1	0	Encoded Scan – N Key Rollover
0	1	1	Decoded Scan – N Key Rollover
1	0	0	Encoded Scan-Sensor Matrix
1	0	1	Decoded Scan-Sensor Matrix
1	1	0	Strobed Input, Encoded Display Scan
1	1	1	Strobed Input, Decoded Display Scan

Program Clock

0	0	1	P	P	P	P	P

Where PPPPP is the prescaler value between 2 and 31 this prescaler divides the external clock by PPPPP to develop its internal frequency. After reset, a default value of 31 is generated.

Read FIFO/Sensor RAM

0	1	0	A1	X	A	A	A

$A_0 = 0$

A_1 is the auto-increment flag. AAA is the row to be read by the processor. The read command is accomplished with ($\overline{CS} \cdot RD \cdot \overline{A0}$) by the processor. If A_1 is 1, the row select counter will be incremented after each read. Note that auto-incrementing has no effect on the display.

Read Display RAM

0	1	1	A1	A	A	A	A

$A_0 = 0$

Where A_1 is the auto-increment flag and AAAA is the character which the processor is about to read.

Write Display RAM

1	0	0	A1	A	A	A	A

where AAAA is the character the processor is about to write.

Display Write Inhibit Blanking

1	0	1	X	IW A	IW B	BL A	BL B

Where IWA and IWB are Inhibit Writing nibble A and B respectively, and BLA, BLB are blanking. When using the display as a dual 4-bit, it is necessary to mask one of the 4-bit halves to eliminate interaction between the two halves. This is accomplished with the IW flags. The BL flags allow the programmer to blank either half of the display independently. To blank a display formatted as a single 8-bit, it is necessary to set both BLA and BLB. Default after a reset is all zeros. All signals are active high (1).

Clear

1	1	0	C_D	C_D	C_D	C_F	C_A

C_D	C_D	C_D	
1	0	X	All zeros
1	1	0	AB = 20_{16}
1	1	1	All ones
0	X	X	Disable clear display

This command is used to clear the display RAM, the FIFO, or both. The C_D options allow the user the ability to clear the display RAM to either all zeros or all ones.

C_F clears the FIFO.
C_A clears all.

Clearing the display takes one complete display scan. During this time the processor can't write to the display RAM.

C_F will set the FIFO empty flag and reset IRQ. The sensor matrix mode RAM pointer will then be set to row 0.

C_A is equivalent to C_F and C_D. The display is cleared using the display clear code specified and resets the internal timing logic to synchronize it.

End Interrupt/Error Mode Set

1	1	1	E	X	X	X	X

In the sensor matrix mode, this instruction clears IRQ and allows writing into RAM.

In N key rollover, setting the E bit to 1 allows for operating in the special Error mode. See Description of FIFO status.

FIFO Status

D_U	S/E	O	U	F	N	N	N

Where: D_U = Display Unavailable because a clear display or clear all command is in progress.
S/E = Sensor Error flag due to multiple closure of switch matrix.
O = FIFO Overrun since an attempt was made to push too many characters into the FIFO.
U = FIFO Underrun. An indication that the processor tried to read an empty FIFO.
F = FIFO Full Flag.
NNN = The Number of characters presently in the FIFO.

The FIFO Status is Read with A_0 high and $\overline{CS}$, $\overline{RD}$ active low.

The Display not available is an indication that the C_D or C_A command has not completed its clearing. The S/E flags are used to show an error in multiple closures has occurred. The O or U, overrun or underrun, flags occur when too many characters are written into the FIFO or the processor tries to read an empty FIFO. F is an indication that the FIFO is full and NNN is the number of characters in the FIFO.

Data Read

Data can be read during A_0 = 0 and when $\overline{CS}$, $\overline{RD}$ are active low. The source of the data is determined by the Read Display or Read FIFO commands.

Data Write

Data is written to the chip when A_0, $\overline{CS}$, and $\overline{WR}$ are active low. Data will be written into the display RAM with its address selected by the latest Read or Write Display command.

COMMAND OPERATION (CONT.)

Data Format

CNTL	SH	SCAN	RET

In the Scanned Key mode, the characters in the FIFO correspond to the above format where CNTL and SH are the most significant bits and the SCAN and return lines are the scan and column counters.

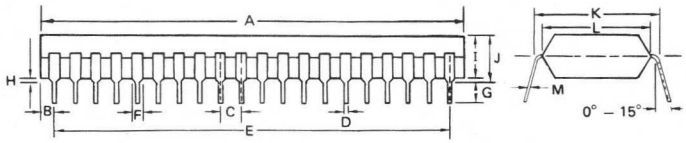
RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0

In the Sensor Matrix mode, the data corresponds directly to the row of the sensor RAM being scanned. Shift and control (SH, CNTL) are not used in this mode.

Control Address Summary

A_0	DATA MSB							LSB	
1	0	0	0	D	D	K	K	K	Keyboard Display Mode Set
1	0	0	1	P	P	P	P	P	Load Program Clock
0	0	1	0	A_1	X	A	A	A	Read FIFO/Sensor RAM
0	0	1	1	A_1	A	A	A	A	Read Display RAM
1	1	0	0	A_1	A	A	A	A	Write Display RAM
1	1	0	1	X	IW A	IW B	BL A	BL B	Display Write Inhibit/Blanking
1	1	1	0	C_D	C_D	C_D	C_F	C_A	Clear
1	1	1	1	E	X	X	X	X	End Interrupt/Error Mode Set
1	D_U	S/E	0	U	F	N	N	N	FIFO Status

PACKAGE OUTLINE μPD8279-5C



(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{0.05}$	$0.010^{+0.004}_{0.002}$

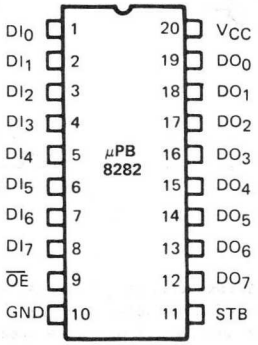
OCTAL LATCH

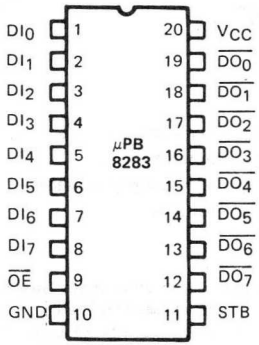
DESCRIPTION

The μPB8282/8283 are 8-bit latches with tri-state output buffers. The 8282 is non-inverting and the 8283 inverts the input data. These devices are ideal for demuxing the address/data buses on the 8085A/8086 microprocessors.
The 8282/8283 are fabricated using NEC's Schottky bipolar process.

FEATURES

- Supports 8080, 8085A, 8048, 8086 Family Systems
- Transparent During Active Strobe
- Fully Parallel 8-Bit Data Register and Buffer
- High Output Drive Capability (32 mA) for Driving the System Data Bus
- Tri-State Outputs
- 20-Pin Package





PIN NAMES

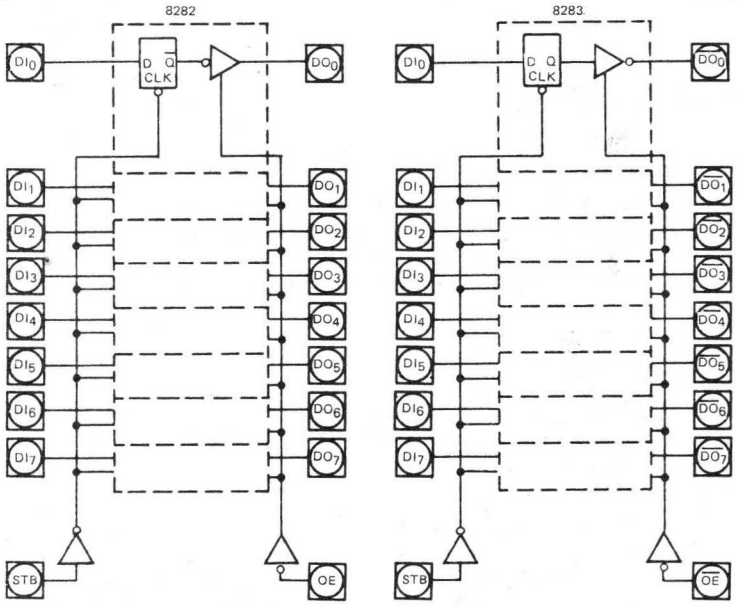
DI_0-DI_7	DATA IN
$DO_0$$DO_7$	DATA OUT
$\overline{OE}$	OUTPUT ENABLE
STB	STROBE

FUNCTIONAL DESCRIPTION

The μPB8282/8283 are 8-bit latches with tri-state output buffers. Data on the inputs is latched into the data latches on a high to low transition of the STB line. When STB is high, the latches appear transparent. The OE input enables the latched data to be transferred to the output pins. When OE is high, the outputs are put in the tri-state condition. OE will not cause transients to appear on the data outputs.

μPB8282/8283

BLOCK DIAGRAMS



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to 5.5V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

Conditions: V_{CC} = 5V ± 5%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Clamp Voltage	V_C		−1	V	I_C = −5 mA
Power Supply Current	I_{CC}		160	mA	
Forward Input Current	I_F		−0.2	mA	V_F = 0.45V
Reverse Input Current	I_R		50	μA	V_R = 5.25V
Output Low Voltage	V_{OL}		0.50	V	I_{OL} = 32 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −5 mA
Output Off Current	I_{OFF}		±50	μA	V_{OFF} = 0.45 to 5.25V
Input Low Voltage	V_{IL}		0.8	V	V_{CC}=5.0V①
Input High Voltage	V_{IH}	2.0		V	V_{CC}=5.0V① F=1 MHz
Input Capacitance	C_{IN}		12	pF	V_{BIAS}=2.5V, V_{CC}=5V T_a=25°C

Notes: ① Output Loading I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF

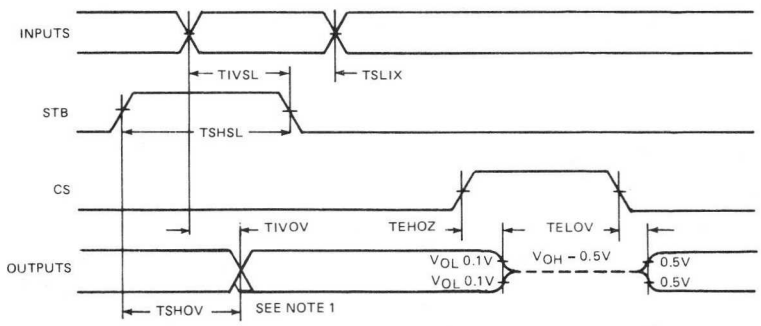
AC CHARACTERISTICS

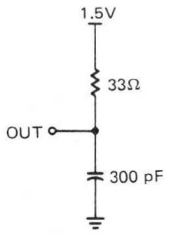
Conditions: V_{CC} = 5V ± 5%, T_a = 0°C to 70°C

Loading: Outputs – I_{OL} = 32 mA, I_{OH} = –5 mA, C_L = 300 pF

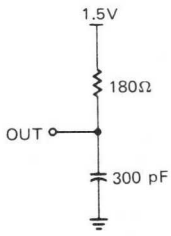
PARAMETER	SYMBOL	MIN	MAX	UNITS
Input to Output Delay	TIVOV			
—Inverting			25	ns
—Non-Inverting			35	ns
STB to Output Delay	TSHOV			
—Inverting			45	ns
—Non-Inverting			55	ns
Output Disable Time	TEHOZ		25	ns
Output Enable Time	TELOV	10	50	ns
Input to STB Setup Time	TIVSL	0		ns
Input to STB Hold Time	TSLIX	25		ns
STB High Time	TSHSL	15		ns

TIMING WAVEFORMS

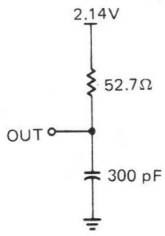




3-STATE TO V_{OL}



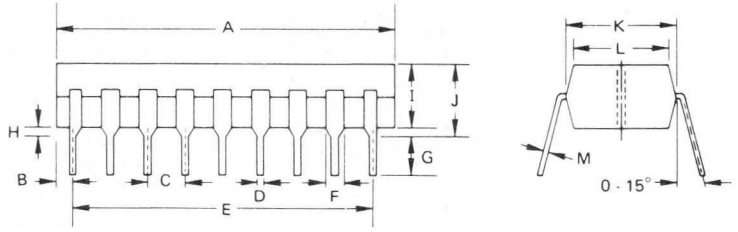
3-STATE TO V_{OH}



SWITCHING

9

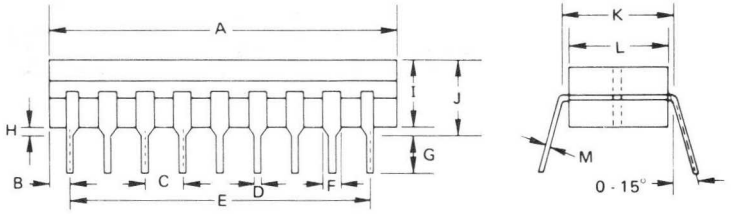
PACKAGE OUTLINES
μPB8282C
μPB8283C



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPB8282D
μPB8283D



Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

CLOCK GENERATOR AND DRIVER FOR 8086/8088 MICROPROCESSORS

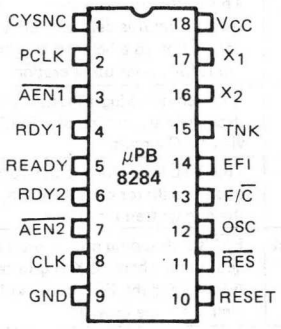
DESCRIPTION

The μPB8284 is a clock generator and driver for the 8086 and 8088 microprocessors This bipolar driver provides the microprocessor with a reset signal and also provides properly synchronized READY timing. A TTL clock is also provided for peripheral devices.

FEATURES

- Generate System Clock for the 8086 and 8088
- Frequency Source can be a Crystal or a TTL Signal
- MOS Level Output for the Processor
- TTL Level Output for Peripheral Devices
- Power-Up Reset for the Processor
- READY Synchronization
- +5V Supply
- 18 Pin Package

PIN CONFIGURATION



PIN NAMES

X_1, X_2	Crystal Connections
TANK	For Overtone Crystal
$F/\overline{C}$	Clock Source Select
EFI	External Clock Input
CSYNC	Clock Synchronization Input
RDY1, RDY2	Ready Signal from Multibus™* Systems
$\overline{AEN1}$, $\overline{AEN2}$	Address Enable Qualifiers for the two RDY Signals
$\overline{RES}$	Reset Input
RESET	Synchronized Reset Output
OSC	Oscillator Output
CLK	MOS Clock for the Processor
PCLK	TTL Clock for Peripherals
READY	Synchronized Ready Output

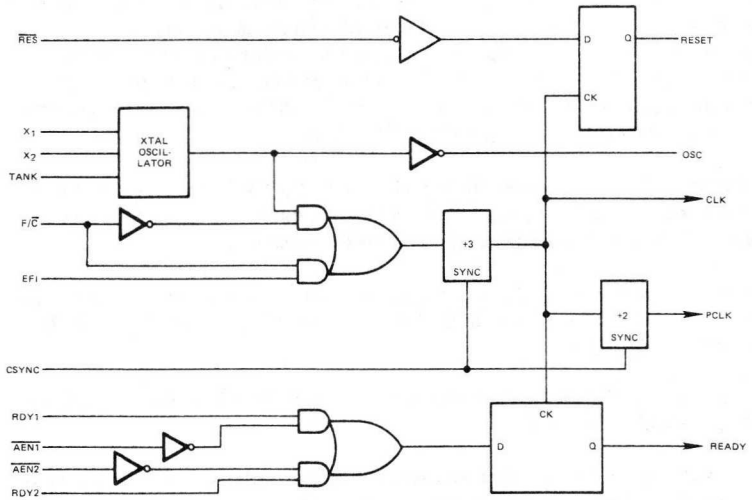
*TM - Multibus is a trademark of Intel Corporation.

9

PIN IDENTIFICATION

NO.	SYMBOL	NAME	FUNCTION
1	CSYNC	Clock Synchronization	An active high signal which allows multiple 8284s to be synchronized. When CYSNC is low, the internal counters count and when high the counters are reset. CYSNC should be grounded when the internal oscillator is used.
2	PCLK	Peripheral Clock	A TTL level clock for use with peripheral devices. This clock is one-half the frequency of CLK.
3, 7	$\overline{AEN1}$, $\overline{AEN2}$	Address Enable	This active low signal is used to qualify its respective RDY inputs. If there is only one bus to interface to, $\overline{AEN}$ inputs are to be grounded.
4, 6	RDY1, RDY2	Bus Ready	This signal is sent to the 8284 from a peripheral device on the bus to indicate that data has been received or data is available to be read.
5	READY	Ready	The READY signal to the microprocessor is synchronized by the RDY inputs to the processor CLK. READY is cleared after the guaranteed hold time to the processor has been met.
8	CLK	Processor Clock	This is the MOS level clock output of 33% duty cycle to drive the microprocessor and bipolar support devices (8288) connected to the processor. The frequency of CLK is one third of the crystal or EFI frequency.
10	RESET	Reset	This is used to initialize the processor. Its input is derived from an RC connection to a Schmitt trigger input for power up operation.
11	$\overline{RES}$	Reset In	This Schmitt trigger input is used to determine the timing of RESET out via an RC circuit.
12	OSC	Oscillator Output	This TTL level clock is the output of the oscillator circuit running at the crystal frequency.
13	F/$\overline{C}$	Frequency Crystal Select	F/$\overline{C}$ is a strapping option used to determine where CLK is generated. A low is for the EFI input, and a high is for the crystal.
14	EFI	External Frequency In	A square wave in at three times the CLK output. A TTL level clock to generate CLK.
16, 17	X_1, X_2	Crystal In	A crystal is connected to these inputs to generate the processor clock. The crystal chosen is three times the desired CLK output.
15	TNK	Tank	This is used for overtone type crystals. (See diagram below.)
18	VCC	VCC	+5V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to +5.5V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

Conditions: T_a = 0°C to 70°C; V_{CC} = 5V ± 10%

PARAMETER	SYMBOL	MIN	MAX	UNIT	TEST CONDITIONS
Forward Input Current	I_F		−0.5	mA	V_F = 0.45V
Reverse Input Current	I_R		50	μA	V_R = 5.25V
Input Forward Clamp Voltage	V_C		−1.0	V	I_C = −5 mA
Power Supply Current	I_{CC}		140	mA	
Input Low Voltage	V_{IL}		0.8	V	V_{CC} = 5.0V
Input High Voltage	V_{IH}	2.0		V	V_{CC} = 5.0V
Reset Input High Voltage	V_{IHR}	2.6		V	V_{CC} = 5.0V
Output Low Voltage	V_{OL}		0.45	V	5 mA = I_{OL}
Output High Voltage CLK Other Outputs	V_{OH}	4 2.4		V V	−1 mA } I_{OH} −1 mA }
$\overline{RES}$ Input Hysteresis	V_{IHR}-V_{ILR}	0.25		V	V_{CC} = 5.0V

FUNCTIONAL DESCRIPTION

The clock generator can provide the system clock from either a crystal or an external TTL source. There is an internal divide by three counter which receives its input from either the crystal or TTL source (EFI Pin) depending on the state of the F/$\overline{C}$ input strapping. There is also a clear input (C SYNC) which is used for either inhibiting the clock, or synchronizing it with an external event (or perhaps another clock generator chip). Note that if the TTL input is used, the crystal oscillator section can still be used for an independent clock source, using the OSC output.

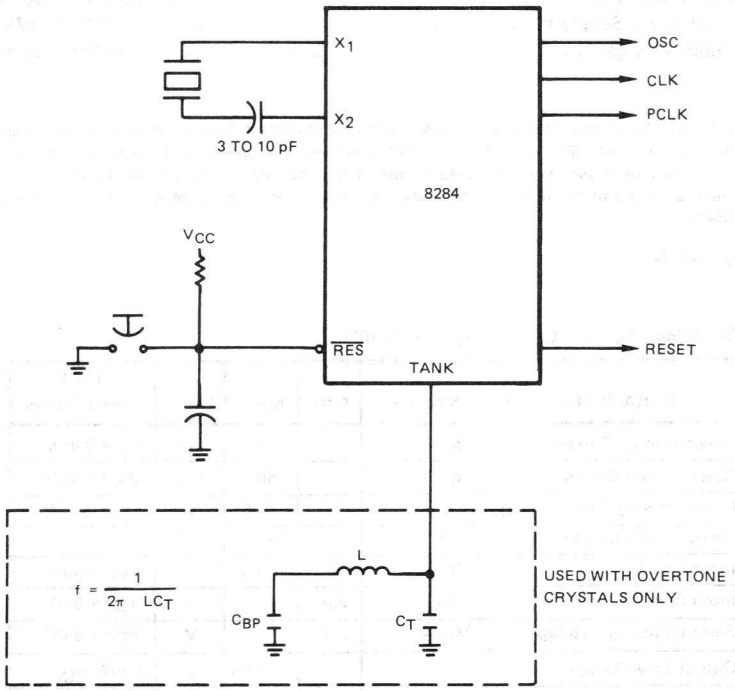
For driving the MOS output level, there is a 33% duty cycle MOS output (CLK) for the microprocessor, and a TTL output (PCLK) with a 50% duty cycle for use as a peripheral clock signal. This clock is at one half of the processor clock speed.

Reset timing is provided by a Schmitt Trigger input ($\overline{RES}$) and a flip-flop to synchronize the reset timing to the falling edge of CLK. Power-on reset is provided by a simple RC circuit on the $\overline{RES}$ input.

There are two READY inputs, each with its own qualifier ($\overline{AEN1}$, $\overline{AEN2}$). The unused $\overline{AEN}$ signal should be tied low.

The READY logic in the 8284 synchronizes the RDY1 and RDY2 asynchronous inputs to the processor clock to insure proper set up time, and to guarantee proper hold time before clearing the ready signal.

TANK INSERT CIRCUIT DIAGRAM



The tank input to the oscillator allows the use of overtone mode crystals. The tank circuit shunts the crystal's fundamental and high overtone frequencies and allows the third harmonic to oscillate. The external LC network is connected to the TANK input and is AC coupled to ground.

AC CHARACTERISTICS

Conditions: $T_a = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$

TIMING REQUIREMENTS

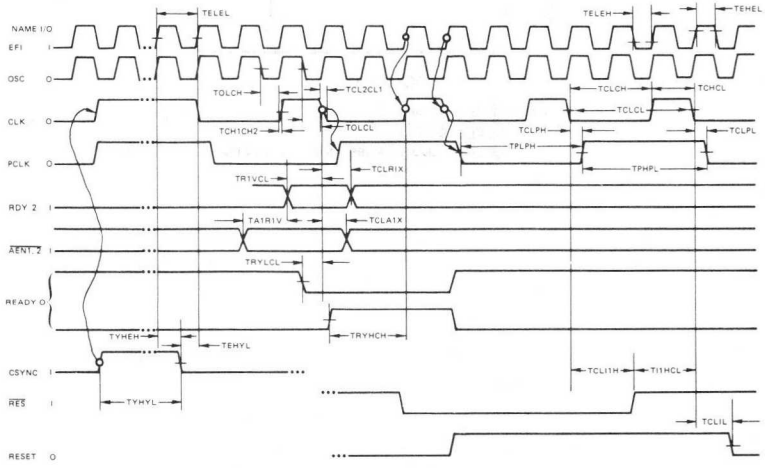
PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
External Frequency High Time	TEHEL	20		ns	90%-90% V_{IN}
External Frequency Low Time	TELEH	20		ns	10%-10% V_{IN}
EFI Period	TELEL	TEHEL + TELEH + δ		ns	①
XTAL Frequency		12	25	MHz	
RDY1, RDY2 Set-Up to CLK	TR1VCL	35		ns	
RDY1, RDY2 Hold to CLK	TCLR1X	0		ns	
AEN1, AEN2 Set-Up to RDY1, RDY2	TA1VR1V	15		ns	
AEN1, AEN2 Hold to CLK	TCLA1X	0		ns	
CSYNC Set-Up to EFI	TYHEH	20		ns	
CSYNC Hold to EFI	TEHYL	20		ns	
CSYNC Width	TYHYL	2 TELEL		ns	
RES Set-Up to CLK	TI1HCL	65		ns	②
RES Hold to CLK	TCLI1H	20		ns	②

TIMING RESPONSES

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
CLK Cycle Period	TCLCL	125		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2.0		ns	Figure 3 and Figure 4
CLK Low Time	TCLCH	(2/3 TCLCL) −15.0		ns	Figure 3 and Figure 4
CLK Rise and Fall Time	TCH1CH2 TCL2CL1		10	ns	1.0V to 3.5V
PCLK High Time	TPHPL	TCLCL −20		ns	
PCLK Low Time	TPLPH	TCLCL −20		ns	
Ready Inactive to CLK ④	TRYLCL	−8		ns	Figure 5 and Figure 6
Ready Active to CLK ③	TRYHCH	(2/3 TCLCL) −15.0		ns	Figure 5 and Figure 6
CLK To Reset Delay	TCLIL		40	ns	
CLK to PCLK High Delay	TCLPH		22	ns	
CLK to PCLK Low Delay	TCLPL		22	ns	
OSC to CLK High Delay	TOLCH	−5	12	ns	
OSC to CLK Low Delay	TOLCL	2	20	ns	

Notes: ① δ = EFI rise (5 ns max) + EFI fall (5 ns max).
② Set up and hold only necessary to guarantee recognition at next clock.
③ Applies only to T3 and TW states.
④ Applies only to T2 states.

TIMING WAVEFORMS*



*ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

AC TEST CIRCUITS

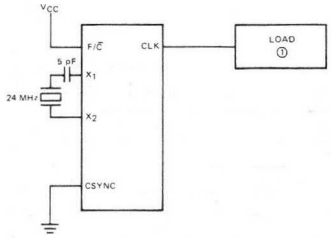


FIGURE 1
CLOCK HIGH AND LOW TIME

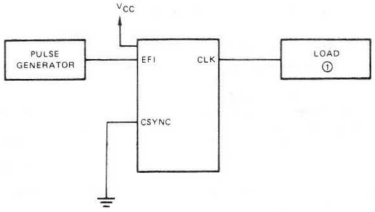


FIGURE 2
CLOCK HIGH AND LOW TIME

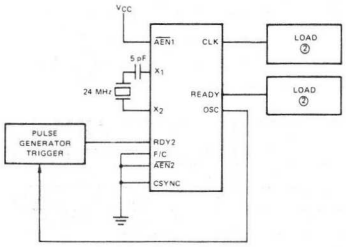


FIGURE 3
READY TO CLK

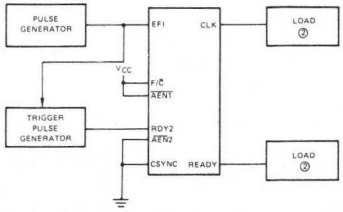
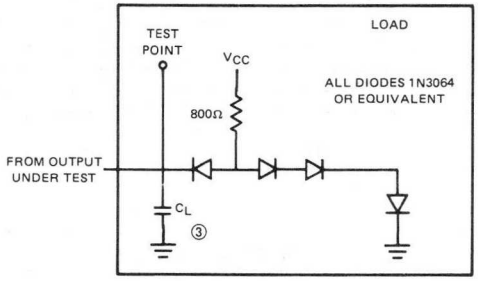


FIGURE 4
READY TO CLK

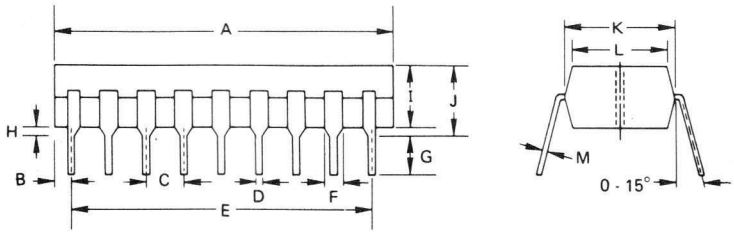


OUTPUT

NOTES: ① C_L = 100 pF
② C_L = 30 pF
③ C_L INCLUDES PROBE AND JIG CAPACITANCE

PACKAGE OUTLINES

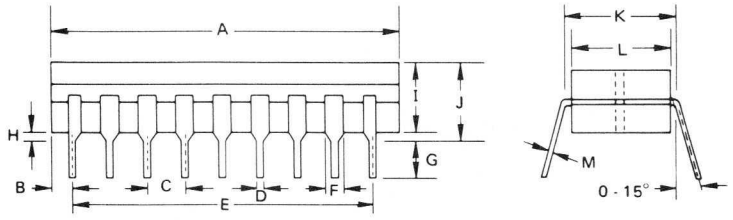
μPB8284C



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPB8284D



Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

8-BIT BUS TRANSCEIVER

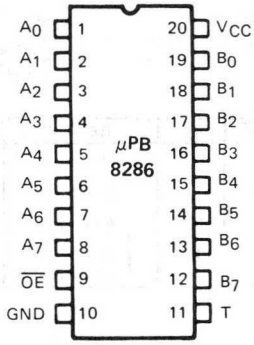
DESCRIPTION

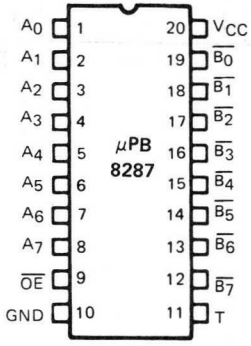
The 8286 and 8287 are octal bus transceivers used for buffering microprocessor bus lines. Being bi-directional, they are ideal for buffering the data bus lines on 8 or 16 bit microprocessors. Each B output is capable of driving 32 mA low or 5 mA high.

FEATURES

- Data Bus Buffer Driver for μCOM-8 (8080, 8085A, 780) and μCOM-16 (8086) families
- Low Input Load Current -- 0.2 mA max.
- High Output Drive Capability for Driving System Data Bus
- Tri-State Outputs
- 20 Pin Package with Fully Parallel 8-Bit Transceivers

PIN CONFIGURATIONS



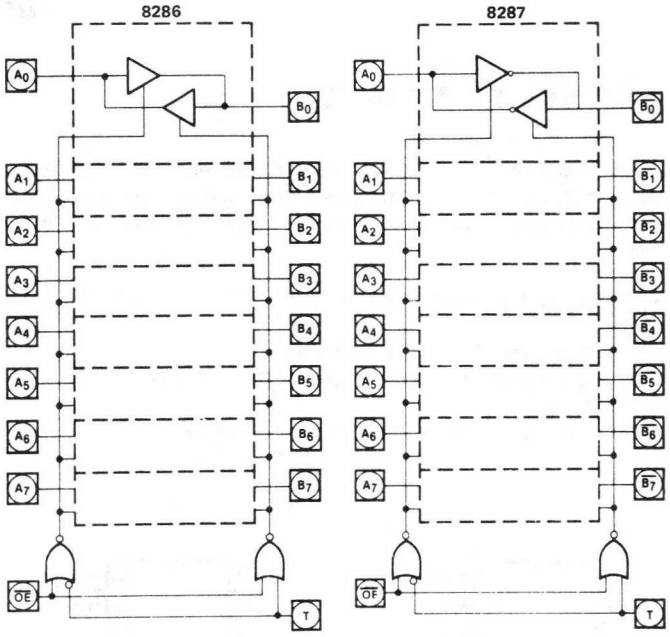


PIN NAMES

A_0-A_7	Local Bus Data
B_0-B_7	System Bus Data
OE	Output Enable
T	Transmit

9

BLOCK DIAGRAMS



$\overline{OE}$	T	RESULT
0	0	B → A
0	1	A → B
1	0	A and B HIGH IMPEDANCE
1	1	A and B HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Power Dissipation . . . . . 1 W

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETER		SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Clamp Voltage		V_C		−1	V	$I_C = -5$ mA
Power Supply Current	− 8287	I_{CC}		130	mA	
	− 8286	I_{CC}		160	mA	
Forward Input Current		I_F		−0.2	mA	$V_F = 0.45V$
Reverse Input Current		I_R		50	μA	$V_R = 5.25V$
Output Low Voltage	− B Outputs	V_{OL}		0.5	V	$I_{OL} = 32$ mA
	− A Outputs			0.5	V	$I_{OL} = 10$ mA
Output High Voltage	− B Outputs	V_{OH}	2.4		V	$I_{OH} = -5$ mA
	− A Outputs		2.4		V	$I_{OH} = -1$ mA
Output Off Current		I_{OFF}		I_F		$V_{OFF} = 0.45V$
Output Off Current		I_{OFF}		I_R		$V_{OFF} = 5.25V$
Input Low Voltage	− A Side	V_{IL}		0.8	V	$V_{CC} = 5.0V$ ①
	− B Side	V_{IL}		0.9	V	$V_{CC} = 5.0V$ ①
Input High Voltage		V_{IH}	2.0		V	$V_{CC} = 5.0V$ ① F = 1 MHz
Input Capacitance	− A Side	C_{IN}		16	pF	$V_{BIAS} = 2.5V$, $V_{CC} = 5V$
	− B Side			22		$T_a = 25°C$

Note: ① B Outputs – $I_{OL} = 32$ mA, $I_{OH} = -5$ mA, $C_L = 300$ pF
A Outputs – $I_{OL} = 10$ mA, $I_{OH} = -1$ mA, $C_L = 100$ pF

CAPACITANCE

$T_a = 25°C$; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I		5	8	pF	$V_I = 0V$
Output Capacitance	C_O		8	12	pF	$V_O = 0V$

AC CHARACTERISTICS

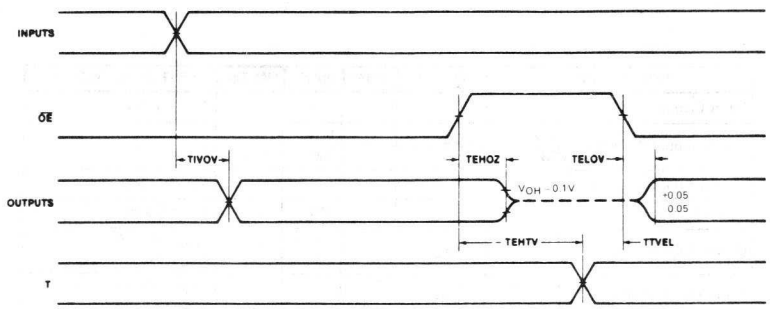
$T_a = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	MIN	MAX	UNITS
TIVOV	Input to Output Delay			
	Inverting		25	ns
	Non-Inverting		35	ns
TEHTV	Transmit/Receive Hold Time	TEHOZ		ns
TTVEL	Transmit/Receive Setup	30		ns
TEHOZ	Output Disable Time		25	ns
TELOV	Output Enable Time	10	50	ns

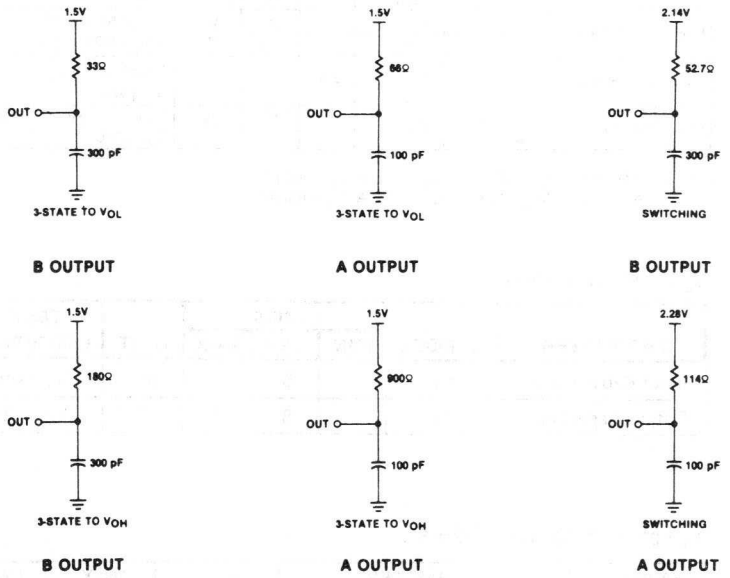
Notes: See waveforms and test load circuit.
B Outputs – $I_{OL} = 32$ mA, $I_{OH} = -5$ mA, $C_L = 300$ pF
A Outputs – $I_{OL} = 10$ mA, $I_{OH} = -1$ mA, $C_L = 100$ pF

9

WAVEFORMS



TEST LOAD CIRCUITS



FUNCTIONAL DISCRIPTION

MOS microprocessors like the 8080/8085A/8086 are generally capable of driving a single TTL load. This also applies to MOS memory devices. While sufficient for minimum type small systems on a single PC board, it is usually necessary to buffer the microprocessor and memory signals when a system is expanded or signals go to other PC boards.
These octal bus transceivers are designed to do the necessary buffering.

Bi-Directional Driver

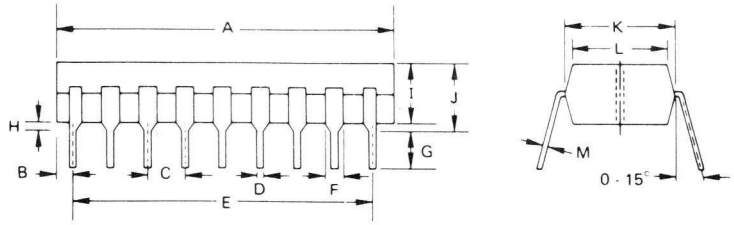
Each buffered line of the octal driver consists of two separate tri-state buffers. The B side of the driver is designed to drive 32 mA and interface the system side of the bus to I/O, memory, etc. The A side is connected to the microprocessor.

Control Gating, $\overline{OE}$, T

The $\overline{OE}$ (output enable) input is an active low signal used to enable the drivers selected by T on to the respective bus.

T is an input control signal used to select the direction of data through the transceivers. When T is high, data is transferred from the A_0-A_7 inputs to the B_0-B_7 outputs, and when low, data is transferred from B_0-B_7 to the A_0-A_7 outputs.

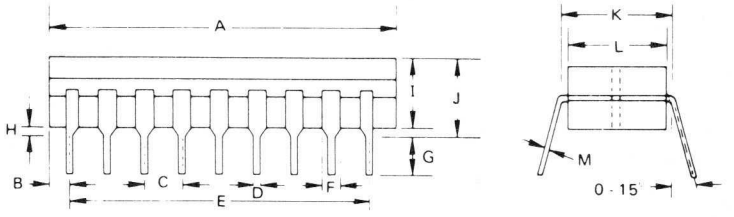
PACKAGE OUTLINE
μPD8286C
μPD8287C



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPD8286D
μPD8287D



Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

9

8286/8287-DS-10-80-CAT

μPD8086/8088 CPU SYSTEM BUS CONTROLLER

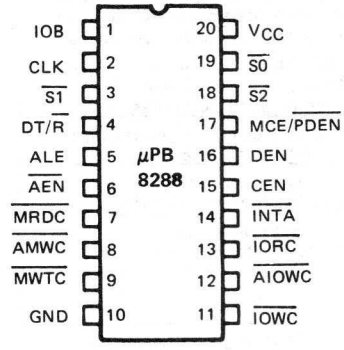
DESCRIPTION

The μPB8288 bus controller is for use in medium to large μPD8086/8088 systems. This 20-pin bipolar component provides command and control timing generation, plus bipolar drive capability and optimal system performance. It provides both Multibus™ command signals and control outputs for the microprocessor system. There is an option to use the controller with a multi-master system bus and separate I/O bus.

FEATURES

- System Controller for μPD8086/8088 Systems
- Bipolar Drive Capability
- Provides Advanced Commands
- Tri-State Output Drivers
- Can be used with an I/O Bus
- Enables Interface to One or Two Multi-Master Buses
- 20-Pin Package

PIN CONFIGURATION



PIN NAMES

S0-S2	Status Input Pins
CLK	Clock
ALE	Address Latch Enable
DEN	Data Enable
DT/R	Data Transmit/Receive
AEN	Address Enable
CEN	Command Enable
IOB	I/O Bus Mode
AIOWC	Advanced I/O Write
IOWC	I/O Write Command
IORC	I/O Read Command
AMWC	Advanced Memory Write
MWTC	Memory Write Command
MRDC	Memory Read Command
INTA	Interrupt Acknowledge
MCE/PDEN	Master Cascade/Peripheral Data Enable

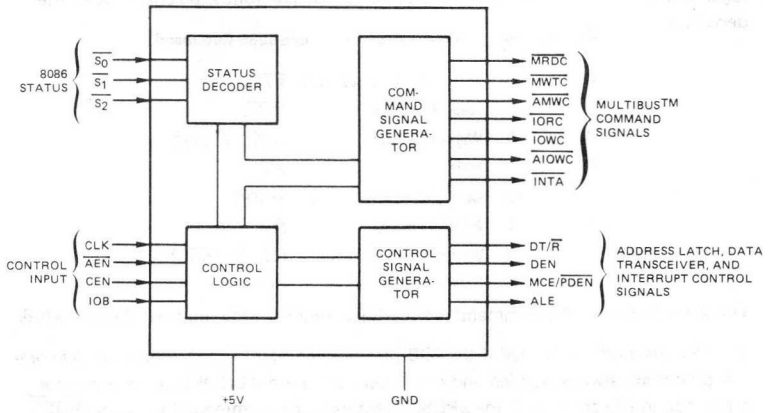
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™ — Multibus is a trademark of Intel Corp.

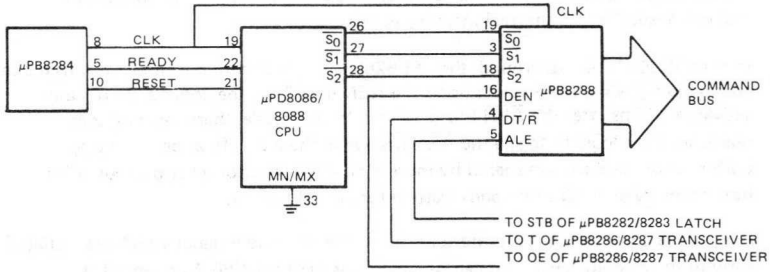
PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1	IOB	I/O Bus Mode	Sets mode of μPB8288, high for the I/O bus mode and low for the system bus mode.
2	CLK	Clock	The clock signal from the μPB8284 clock generator synchronizes the generation of command and control signals.
3, 19, 18	$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	Status Input Pins	The μPB8288 decodes these status lines from the μPB8086 to generate command and control signals. When not in use, these pins are high.
4	DT/$\overline{R}$	Data Transmit/Receive	This signal is used to control the bus transceivers in a system. A high for writing to I/O or memory and a low for reading data.
5	ALE	Address Latch Enable	This signal is used for controlling transparent D type latches (μPB8282/8283). It will strobe in the address on a high to low transition.
6	$\overline{AEN}$	Address Enable	In the I/O system bus mode, AEN enables the command outputs of the μPB8288 105 ns after it becomes active. If AEN is inactive, the command outputs are tri-stated.
7	$\overline{MRDC}$	Memory Read Command	This active low signal is for switching the data from memory to the data bus.
8	$\overline{AMWC}$	Advanced Memory Write Command	This is an advanced write command which occurs early in the machine cycle, with timing the same as the read command.
9	$\overline{MWTC}$	Memory Write Command	This is the memory write command to transfer data bus to memory, but not as early as $\overline{AMWC}$. (See timing waveforms.)
11	$\overline{IOWC}$	I/O Write Command	This command is for transferring information to I/O devices.
12	$\overline{AIOWC}$	Advanced I/O Write Command	This write command occurs earlier in the machine cycle than $\overline{IOWC}$.
13	$\overline{IORC}$	I/O Read Command	This signal enables the CPU to read data from an I/O device.
14	$\overline{INTA}$	Interrupt Acknowledge	This is to signal an interupting device to put the vector information on the data bus
15	CEN	Command Enable	This signal enables all command and control outputs. If CEN is low, these outputs are inactive.
16	DEN	Data Enable	This signal enables the data transceivers onto the bus.
17	MCE/$\overline{PDEN}$	Master Cascade Enable Peripheral Data Enable	Dual function pin system. MC/E – In the bus mode, this signal is active during an interrupt sequence to read the cascade address from the master interrupt controller onto the data bus. $\overline{PDEN}$ – In the I/O bus mode, it enables the transceivers for the I/O bus just as DEN enables bus transceivers in the system bus mode.

BLOCK DIAGRAM



CONNECTING THE BUS CONTROLLER TO THE CPU



ABSOLUTE MAXIMUM RATINGS*

OPERATING TEMPERATURE	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Output and Supply Voltages ①	−0.5V to +7V
All Input Voltages ①	−1.0V to +5.5V
Power Dissipation	1.5W

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

The three status lines ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) from the μPD8086 CPU are decoded by the command logic to determine which command is to be issued. The following chart shows the decoding:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	μPD8086 State	μPB8288 Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

There are two ways the command is issued depending on the mode of the μPB8288.

The I/O bus mode is enabled if the IOB pin is pulled high. In this mode, all I/O command lines are always enabled and not dependent upon $\overline{AEN}$. When the processor sends out an I/O command, the μPB8288 activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control any bus transceivers.

This mode is advantageous if I/O or peripherals dedicated to one microprocessor are in a multiprocessor system, allowing the μPB8288 to control two external buses. No waiting is required when the CPU needs access to the I/O bus, as an $\overline{AEN}$ low signal is needed to gain normal memory access.

If the IOB pin is tied to ground, the μPB8288 is in the system bus mode. In this mode, command signals are dependent upon the $\overline{AEN}$ line. Thus the command lines are activated 105 ns after the $\overline{AEN}$ line goes low. In this mode, there must be some bus arbitration logic to toggle the $\overline{AEN}$ line when the bus is free for use. Here, both memory and I/O are shared by more than one processor, over one bus, with both memory and I/O commands waiting for bus arbitration.

Among the command outputs are some advanced write commands which are initiated early in the machine cycle and can be used to prevent the CPU from entering unnecessary wait states.

The $\overline{INTA}$ signal acts as an I/O read during an interrupt cycle. This is to signal the interrupting device that its interrupt is being acknowledged, and to place the interrupt vector on the data bus.

The control outputs of the μPB8288 are used to control the bus transceivers in a system. DT/$\overline{R}$ determines the direction of the data transfer, and $\overline{DEN}$ is used to enable the outputs of the transceiver. In the IOB mode the MCE/$\overline{PDEN}$ pin acts as a dedicated data enable signal for the I/O bus.

The MCE signal is used in conjunction with an interrupt acknowledge cycle to control the cascade address when more than one interrupt controller (such as a μPD8259A) is used. If there is only one interrupt controller in a system, MCE is not used as the $\overline{INTA}$ signal gates the interrupt vector onto the processor bus. In multiple interrupt controller systems, MCE is used to gate the μPD8259A's cascade address onto the processors local bus, where ALE strobes it into the address latches. This occurs during the first $\overline{INTA}$ cycle. During the second $\overline{INTA}$ cycle the addressed slave μPD8259A gates its interrupt vector onto the processor bus.

The ALE signal occurs during each machine cycle and is used to strobe data into the address latches and to strobe the status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) into the μPB8288. ALE also occurs during a halt state to accomplish this.

The CEN (Command Enable) is used to control the command lines. If pulled high the μPB8288 functions normally and if grounded all command lines are inactive.

DC CHARACTERISTICS

V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	MIN	MAX	UNIT	TEST CONDITIONS
Input Clamp Voltage	V_C		−1	V	I_C = −5 mA
Power Supply Current	I_{CC}		230	mA	
Forward Input Current	I_F		−0.7	mA	V_F = 0.45V
Reverse Input Current	I_R		50	μA	$V_R = V_{CC}$
Output Low Voltage — Command Outputs Control Outputs	V_{OL}		0.5 0.5	V V	I_{OL} = 32 mA I_{OL} = 16 mA
Output High Voltage — Command Outputs Control Outputs	V_{OH}	2.4 2.4		V V	I_{OH} = −5 mA I_{OH} = −1 mA
Input Low Voltage	V_{IL}		0.8	V	
Input High Voltage	V_{IH}	2.0		V	
Output Off Current	I_{OFF}		100	μA	V_{OFF} = 0.4 to 5.25V

AC CHARACTERISTICS

V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

TIMING REQUIREMENTS

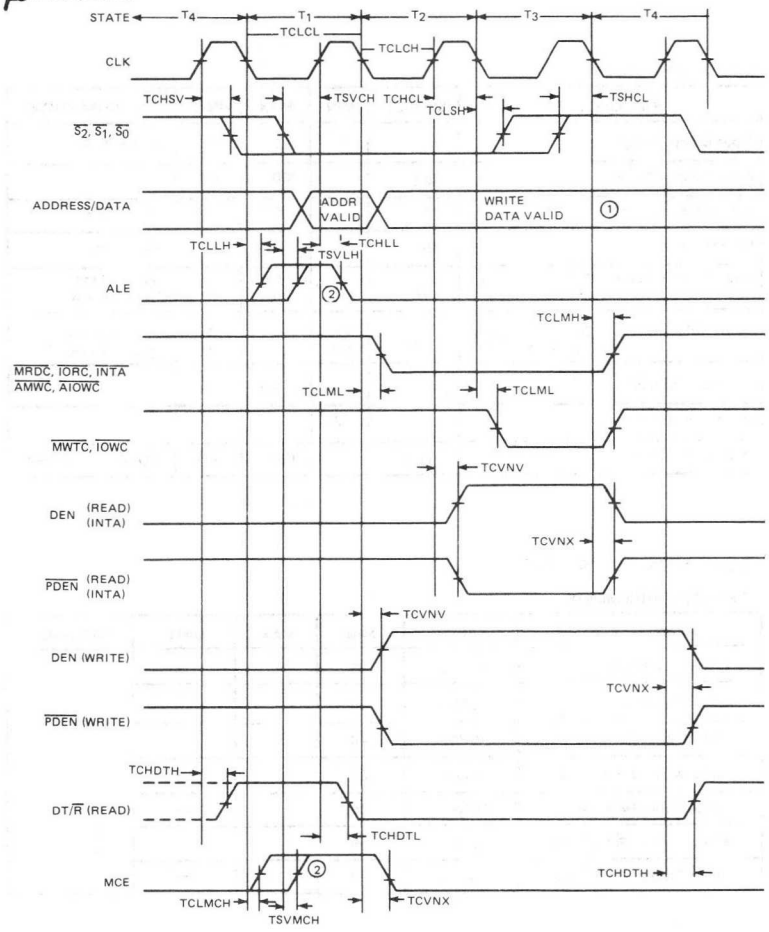
PARAMETER	SYMBOL	MIN	MAX	UNIT	LOADING
CLK Cycle Period	TCLCL	125		ns	
CLK Low Time	TCLCH	66		ns	
CLK High Time	TCHCL	40		ns	
Status Active Setup Time	TSVCH	65		ns	
Status Active Hold Time	TCHSV	10		ns	
Status Inactive Setup Time	TSHCL	55		ns	
Status Inactive Hold Time	TCLSH	10		ns	

TIMING RESPONSES

PARAMETER	SYMBOL	MIN	MAX	UNIT	LOADING
Control Active Delay	TCVNV	5	45	ns	
Control Inactive Delay	TCVNX	10	45	ns	
ALE MCE Active Delay (from CLK)	TCLLH, TCLMCH		15	ns	
ALE MCE Active Delay (from Status)	TSVLH, TSVMCH		15	ns	$\overline{MRDC}$, $\overline{IORC}$, $\overline{MWTC}$, $\overline{IOWC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{AIOWC}$: I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF
ALE Inactive Delay	TCHLL		15	ns	
Command Active Delay	TCLML	10	35	ns	
Command Inactive Delay	TCLMH	10	35	ns	
Direction Control Active Delay	TCHDTL		50	ns	
Direction Control Inactive Delay	TCHDTH		30	ns	
Command Enable Time	TAELCH		40	ns	
Command Disable Time	TAEHCZ		40	ns	
Enable Delay Time	TAELCV	105	275	ns	Other: I_{OL} = 16 mA, I_{OH} = −1 mA, C_L = 80 pF
AEN to DEN	TAEVNV		20	ns	
CEN to DEN, PDEN	TCEVNV		20	ns	
CEN to Command	TCELRH		TCLML	ns	

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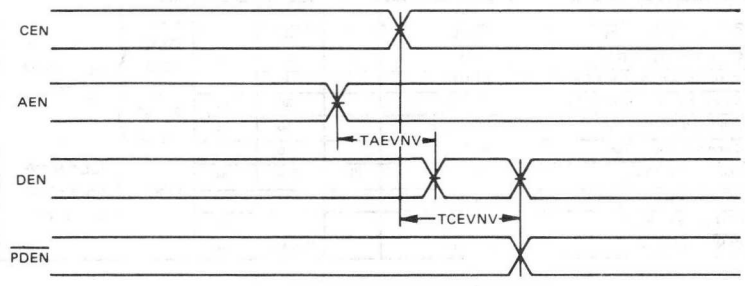
TIMING WAVEFORMS



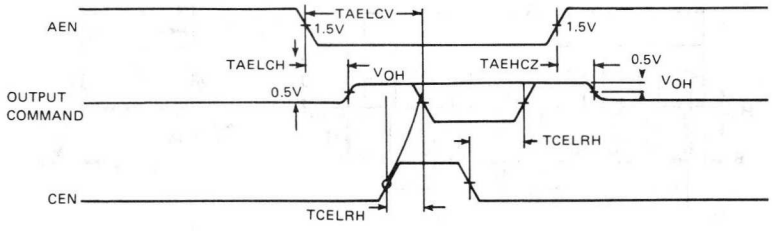
NOTES:

1. ADDRESS/DATA BUS IS SHOWN ONLY FOR REFERENCE PURPOSES.
2. LEADING EDGE OF ALE AND MCE IS DETERMINED BY THE FALLING EDGE OF CLK OR STATUS GOING ACTIVE, WHICHEVER OCCURS LAST.
3. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS SPECIFIED OTHERWISE.

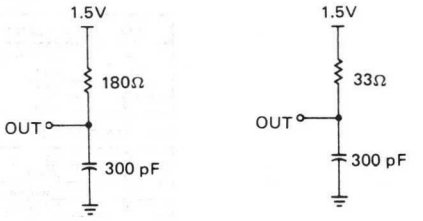
DEN, $\overline{\text{PDEN}}$ QUALIFICATION TIMING



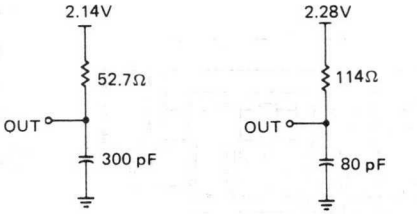
μPB8288 ADDRESS ENABLE ($\overline{AEN}$) TIMING (3-STATE ENABLE/DISABLE)



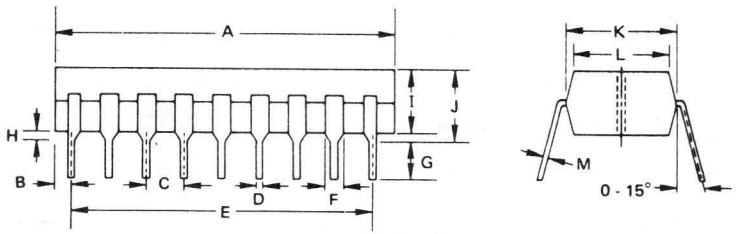
TEST LOAD CIRCUITS



3-STATE COMMAND OUTPUT TEST LOAD



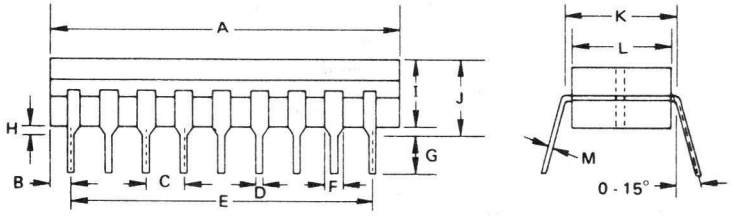
PACKAGE OUTLINES
μPB8288C



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPB8288D



Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

16,384 BIT ROM WITH I/O PORTS
16,384 BIT EPROM WITH I/O PORTS*

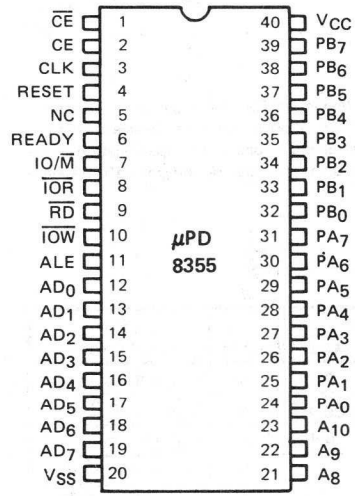
DESCRIPTION

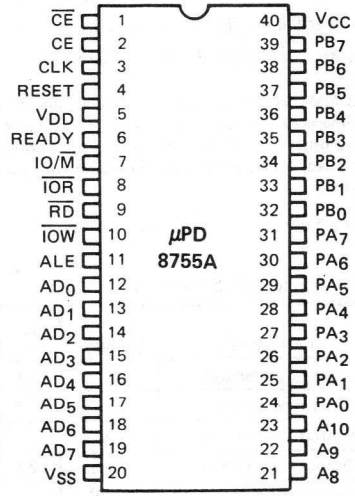
The μPD8355 and the μPD8755A are μPD8085A Family components. The μPD8355 contains 2048 x 8 bits of mask ROM and the μPD8755A contains 2048 x 8 bits of mask EPROM for program development. Both components also contain two general purpose 8-bit I/O ports. They are housed in 40 pin packages, are designed to directly interface to the μPD8085A, and are pin-for-pin compatible with each other.

FEATURES

- 2048 X 8 Bits Mask ROM (μPD8355)
- 2048 X 8 Bits Mask EPROM (μPD8755A)
- 2 Programmable I/O Ports
- Single Power Supplies: +5V
- Directly Interfaces to the μPD8085A
- Pin for Pin Compatible
- μPD8755A: UV Erasable and Electrically Programmable
- μPD8335 Available in Plastic Package
- μPD8755A Available in Ceramic Package

PIN CONFIGURATIONS





NC: Not Connected

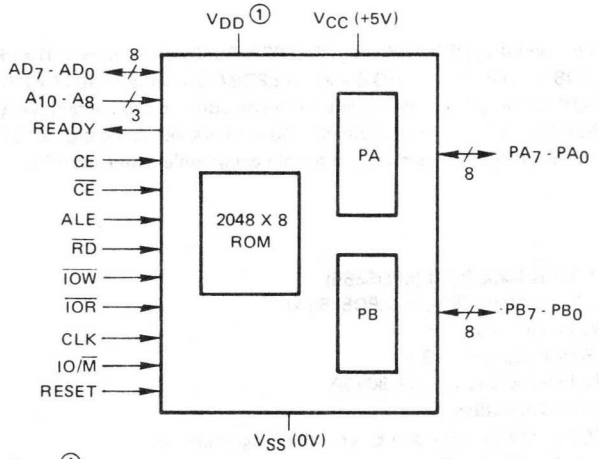
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FUNCTIONAL DESCRIPTION

The μPD8355 and μPD8755A contain 16,384 bits of mask ROM and EPROM respectively, organized as 2048 X 8. The 2048 word memory location may be selected anywhere within the 64K memory space by using the upper 5 bits of address from the μPD8085A as a chip select.

The two general purpose I/O ports may be programmed input or output at any time. Upon power up, they will be reset to the input mode.

BLOCK DIAGRAM



Note: ① V_{DD} applies to μPD8755A only.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature (μPD8355)	0°C to +70°C
(μPD8755A)	-10°C to +70°C
Storage Temperature (Ceramic Package)	-65°C to +150°C
(Plastic Package)	-40°C to +125°C
Voltage on Any Pin (μPD8355)	-0.3 to +7 Volts ①
(μPD8755A)	-0.5 to +7 Volts ①
Power Dissipation	1.5W

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	V_{CC} = 5.0V ①
Input High Voltage	V_{IH}	2.0		V_{CC}+0.5	V	V_{CC} = 5.0V ①
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -400 μA
Input Leakage	I_{IL}			10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{LO}			±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CC} Supply Current	I_{CC}			180	mA	

Note: ① These conditions apply to μPD8355 only.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1,2	$\overline{CE}$, CE	Chip Enables	Enable Chip activity for memory or I/O
3	CLK	Clock Input	Used to Synchronize Ready
4	Reset	Reset Input	Resets PA and PB to all inputs
5 ①	NC	Not Connected	
5 ②	V_{DD}	Programming Voltage	Used as a programming voltage, tied to +5V normally
6	Ready	Ready Output	A tri-state output which is active during data direction register loading
7	IO/$\overline{M}$	I/O or Memory Indicator	An input signal which is used to indicate I/O or memory activity
8	IOR	I/O Read	I/O Read Strobe In
9	$\overline{RD}$	Memory Read	Memory Read Strobe In
10	$\overline{IOW}$	I/O Write	I/O Write Strobe In
11	ALE	Address Low Enable	Indicates information on Address/Data lines is valid
12-19	AD_0-AD_7	Low Address/Data Bus	Multiplexed Low Address and Data Bus
20	V_{SS}	Ground	Ground Reference
21-23	A_8-A_{10}	High Address	High Address inputs for ROM reading
24-31	PA_0-PA_7	Port A	General Purpose I/O Port
32-39	PB_0-PB_7	Port B	General Purpose I/O Port
40	V_{CC}	5V Input	Power Supply

Notes: ① μPD8355
② μPD8755A

I/O PORTS

I/O port activity is controlled by performing I/O reads and writes to selected I/O port numbers. Any activity to and from the μPD8355 requires the chip enables to be active. This can be accomplished with no external decoding for multiple devices by utilizing the upper address lines for chip selects. ① Port activity is controlled by the following I/O addresses:

AD_1	AD_0	PORT SELECTED	FUNCTION
0	0	A	Read or Write PA
0	1	B	Read or Write PB
1	0	A	Write PA Data Direction
1	1	B	Write PB Data Direction

Since the data direction registers for PA and PB are each 8-bits, any pin on PA or PB may be programmed as input or output (0 = in, 1 = out).

Note: ① During ALE time the data/address lines are duplicated on A_{15}-A_8.

AC CHARACTERISTICS

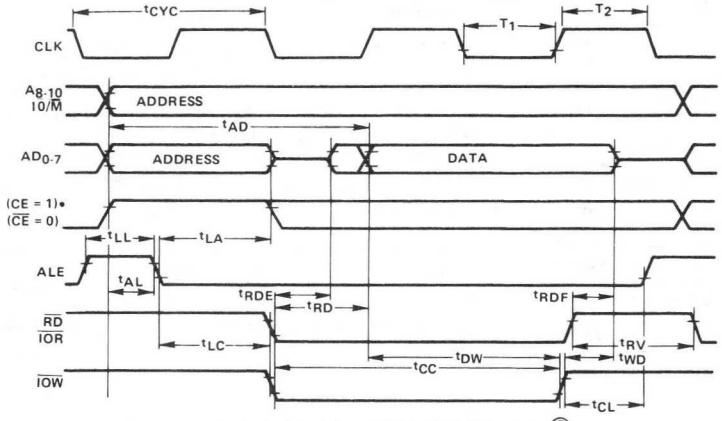
T_a = 0°C to +70°C; V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Cycle Time	t_{CYC}	320			ns	
CLK Pulse Width	T_1	80			ns	C_{LOAD} = 150 pF
CLK Pulse Width	T_2	120			ns	
CLK Rise and Fall Time	t_f, t_r			30	ns	
Address to Latch Set Up Time	t_{AL}	50			ns	
Address Hold Time After Latch	t_{LA}	80			ns	
Latch to READ/WRITE Control	t_{LC}	100			ns	
Valid Data Out Delay from READ Control	t_{RD}			170 ① / 150 ②	ns	
Address Stable to Data Out Valid	t_{AD}			400	ns	150 pF Load
Latch Enable Width	t_{LL}	100			ns	
Data Bus Float After READ	t_{RDF}	0		100	ns	
READ/WRITE Control to Latch Enable	t_{CL}	20			ns	
READ/WRITE Control Width	t_{CC}	250			ns	
Data In to WRITE Set Up Time	t_{DW}	150			ns	
Data In Hold Time After WRITE	t_{WD}	10③			ns	
WRITE to Port Output	t_{WP}			400	ns	
Port Input Set Up Time	t_{PR}	50			ns	
Port Input Hold Time	t_{RP}	50			ns	
READY HOLD TIME	t_{RYH}	0		160 ① / 120 ②	ns	
ADDRESS (CE) to READY	t_{ARY}			160	ns	
Recovery Time Between Controls	t_{RV}	300			ns	
Data Out Delay from READ Control	t_{RDE}	10			ns	

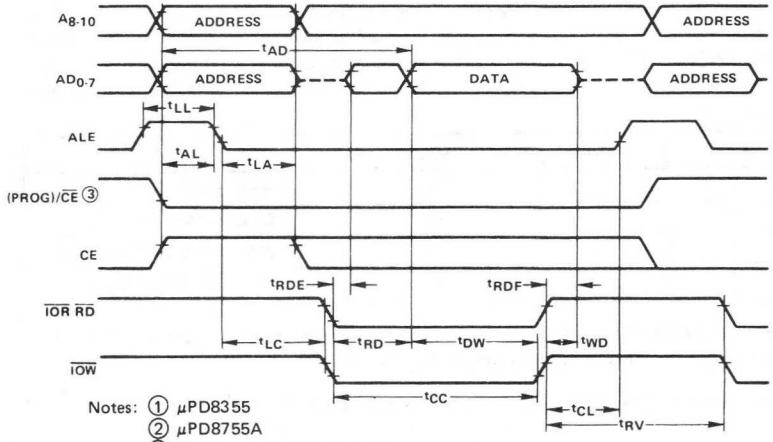
Notes: ① μPD8355 ② μPD8755A ③ 30 ns for μPD8755A

TIMING WAVEFORMS

ROM READ, I/O READ AND WRITE ①



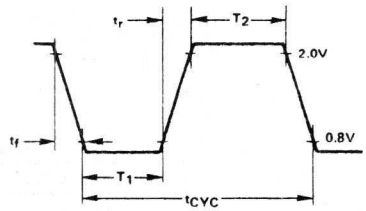
PROM READ, I/O READ AND WRITE ②



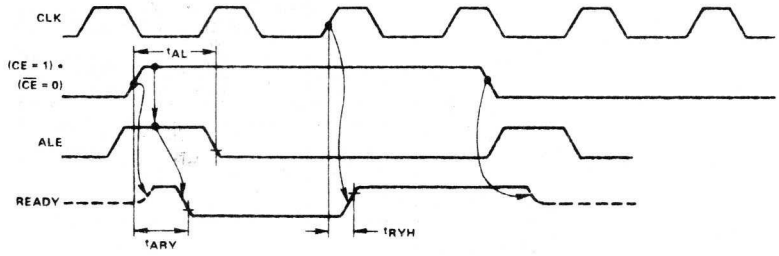
Notes: ① μPD8355
② μPD8755A
③ CE must remain low for the entire cycle

TIMING WAVEFORMS (CONT.)

CLOCK

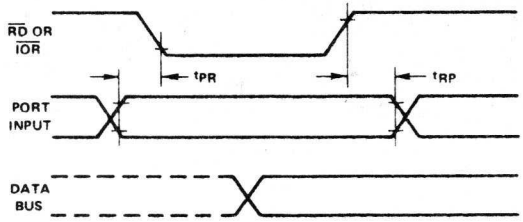


WAIT STATE TIMING (READY = 0)

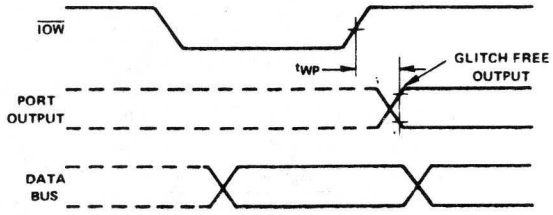


I/O PORT

INPUT MODE:

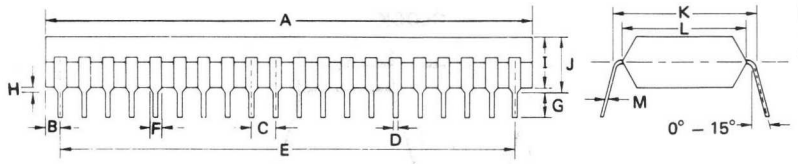


OUTPUT MODE:



EPROM PROGRAMMING μPD8755A

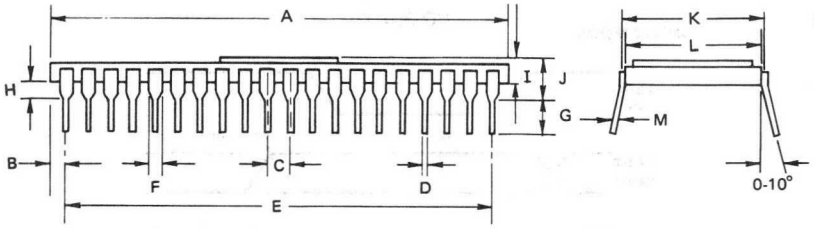
Erasure of the μPD8755A occurs when exposed to ultraviolet light sources of wavelengths less than 4000 Å. It is recommended, if the device is exposed to room fluorescent lighting or direct sunlight, that opaque labels be placed over the window to prevent exposure. To erase, expose the device to ultraviolet light at 2537 Å at a minimum of 15 W-sec/cm^2 (intensity X expose time). After erasure, all bits are in the logic 1 state. Logic 0's must be selectively programmed into the desired locations. It is recommended that NEC's PROM programmer be used for this application.



PACKAGE OUTLINE
μPD8355C

(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



μPD8755AD

(CERAMIC)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.03 MAX.
B	1.62 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.0019

BOARD PRODUCTS 10

NEC Microcomputers, Inc. BP-0200

16K CMOS RAM Board

STANDARD FEATURES

- 16K Bytes of Read/Write Memory Utilizing the NEC μPD444/6514 CMOS RAM for Both 8-Bit Byte and 16-Bit Data Words
- Minimum of 7 Days (168 Hrs.) of Continuous Battery Back-Up
- On-Board Batteries and Battery Charger with Short Circuit and Overcharge Protection
- Test Points Provided for Battery Status
- Provision for A/C Low Line Input
- Memory Inhibit Allows Paging of 2 or More Boards to the Same Address Block
- Memory Deselect in 2K Byte Blocks
- Supports Both 16-Bit and 20-Bit Addressing

DESCRIPTION

The BP-0200 interfaces directly to any Multibus™ system. The board contains 16K bytes of read/write memory utilizing NEC Microcomputers, Inc.'s μPD444/6514 CMOS RAM memory components.

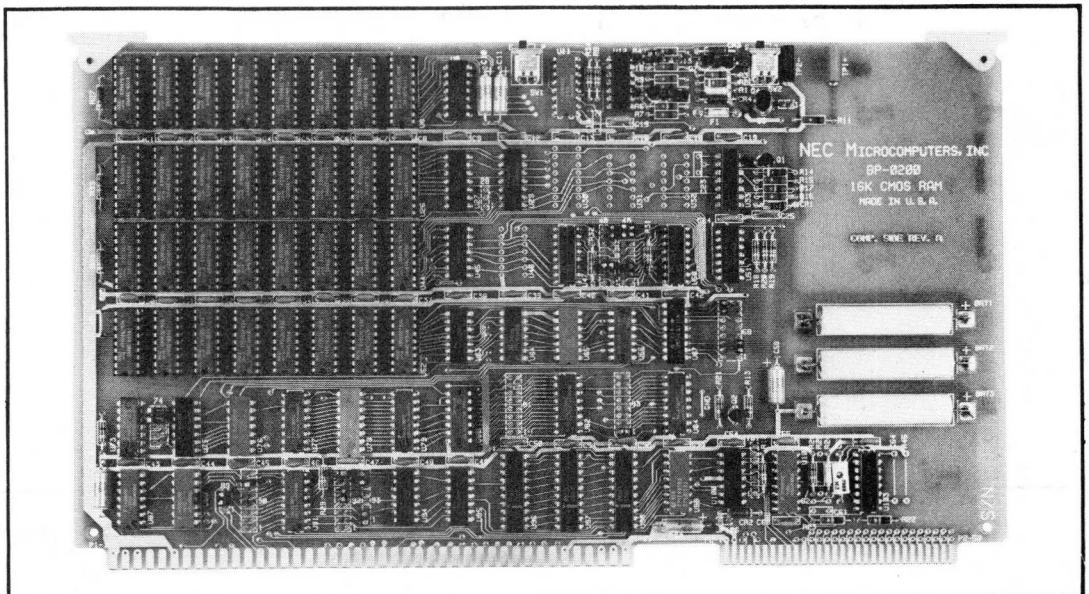
The BP-0200 contains jumpers to allow the user to locate memory anywhere in a one megabyte field along any 16K boundary starting at 00000_H, (i.e., 04000_H, 08000_H, $0C000_H$, etc.). The board contains a memory inhibit function which allows 2 or more of the CMOS RAM boards to be used in a paging technique. Memory, for systems flexibility, can be deselected by jumpers in 2K byte blocks.

The BP-0200 operates as a slave to the processor but contains its own power source in case of power failure. The BP-0200 NiCd batteries supply a minimum of 7 days of battery back-up, when the batteries are fully charged. The on-board batteries can be disconnected and power fail sense circuits disabled for battery changing or for storage.

The BP-0200 has an input port which can test the status of Memory Inhibit, Battery Level, Power Fail Sense, and Power Fail Memory Inhibit. The BP-0200 Output port can control Memory Inhibit of the 16K RAM and can reset Power Fail Sense.

If AC power fails or drops below 103/203 VAC, the system power supply should raise AC Power Low (ACLO) to initiate an orderly power-down sequence. The processor is immediately interrupted so that it may store machine status. Approximately 3.8 milliseconds after the Power Fail Interrupt, all further access is denied to the BP-0200 RAM until system power is restored.

The BP-0200 is a powerful memory expansion module that allows the user the highest degree of confidence in maintaining critical data during power outages or shortages.



TM: Multibus is a registered trademark of Intel Corp.

BP-0200

SPECIFICATIONS

Word Size
- 8 or 16 bit data bus Software controlled

Memory Size
- 16K bytes (8K words)
- NEC μPD444/6514

Memory Addressing
- 20 bit addressing capability

Address Selection
- Jumper selectable along 16K boundaries starting at 00000_H (00000_H, 04000, 08000 . . . FC000)

Memory Response Time
- Read Access: 450 ns Max.
- Read Cycle: 600 ns Max.

Bus Compatibility
- Interface: TTL compatible
- P_1: 86 pin, double-sided, 0.156 inch centers.
- P_2: 60 pin, double-sided, 0.100 inch centers.

Physical Characteristics
- Width: 12.00 in. (30.48 cm)
- Height: 6.75 in. (17.15 cm)
- Thickness: 0.50 in. (1.27 cm)
- Weight: 376.00 grams

Power Requirements (Operational)
- V_{CC} = +5V ± 5%
- I_{CC} = 0.9A Typ, 1.2A Max.

Battery Power Requirements
- V_{BAT} = 3.6 V (Nominal)
- I_{BAT} = 200 μA Max.

Battery Characteristics
- Type: AAA-size NiCd (3 pcs.)
- Capacity: 180 mA hours
- Voltage: 3.6V nominal

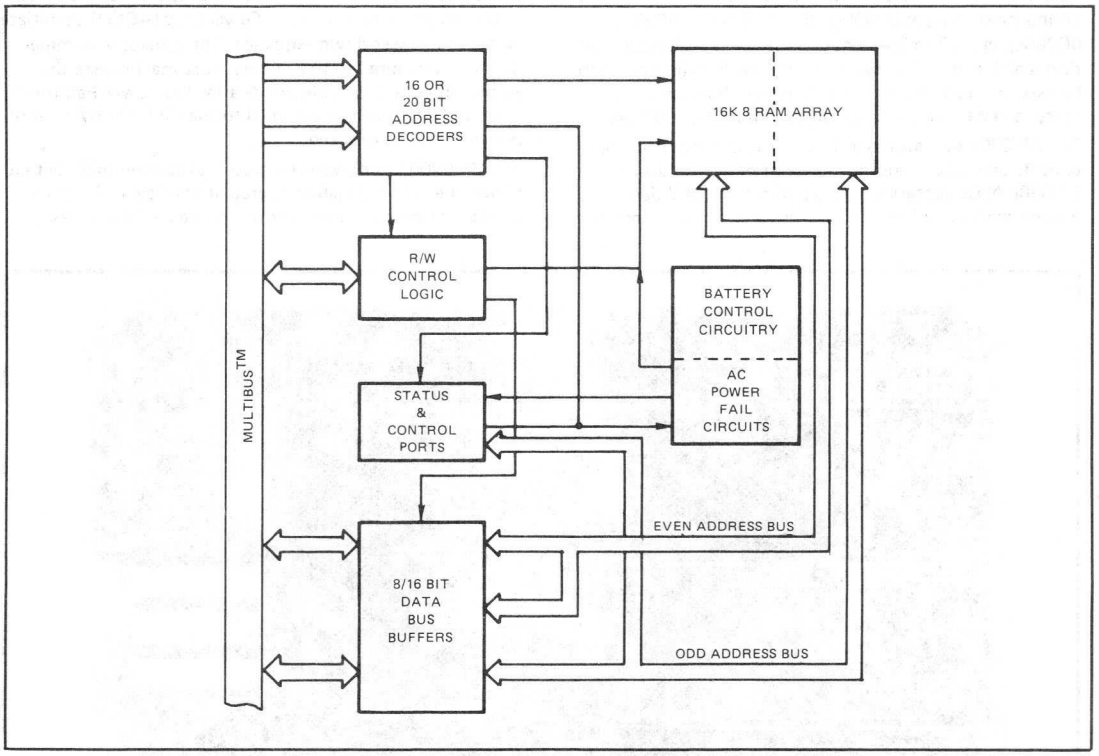
Battery Charge Time
- 14 hours for full charge (180 mA hours), full overcharge and short circuit protection.

Data Retention
- 168 hours following removal of +5V bus power.

Environmental Requirements
- Operating Temp.: 32° to 131°F (0° to 55°C)
- Relative Humidity: to 90% without condensation.

Applicable Literature
- BP-0200 User's Manual

BLOCK DIAGRAM



BP-0200-12-80-CAT

NEC Microcomputers, Inc. BP-0220

CMOS RAM/EPROM Board

STANDARD FEATURES

- ☐ 16K Bytes of Read/Write Memory utilizing NEC μPD444/6514 CMOS RAM for Both 8-Bit Byte and 16-Bit Data Words.
- ☐ Sockets (8) for either industry standard 2716's or 2732's.
- ☐ EPROM address decoding via Bipolar fusable link PROMs.
- ☐ Provision for A/C low line input and 5 volt power fail detect.
- ☐ On Board batteries and battery charger with short circuit and overcharge protection for CMOS and back-up.
- ☐ Memory inhibit allows paging of 2 or more boards to the same address block.
- ☐ Supports 16 bit and 20 bit addressing.

DESCRIPTION

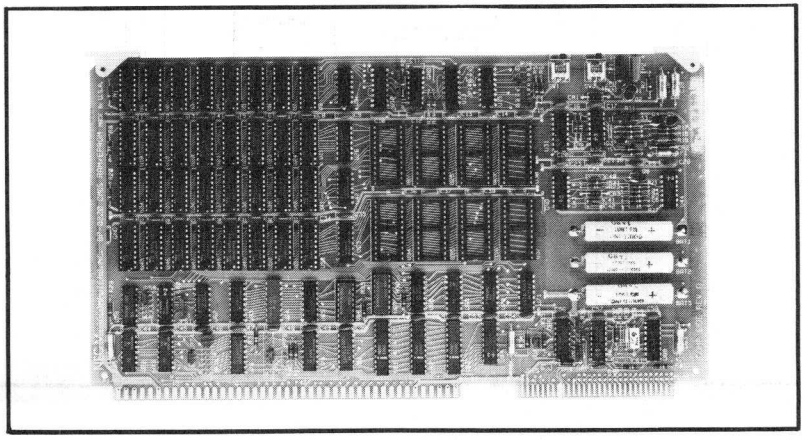
The BP-0220 is a member of the NEC Microcomputers family of Multibus™ boards. The BP-0220 interfaces directly to any Multibus system to expand RAM/ROM memory capacity.

The BP-0220 contains 16K bytes of static Read/Write memory utilizing NEC Microcomputers μPD444/6514 CMOS RAM memory devices, and in addition, contains sockets for either 8-2716 or 8-2732 industry standard EPROMS (user supplied). The BP-0220 memory may be located, through jumper selection, anywhere in a one-megabyte field beginning on any 16K address boundary. Memory address decoding is accomplished by 2-μPB403/74S287 Fuseable Link PROMs. The user has the option of selecting from NEC's four choices of preprogrammed PROMS or creating address decoding patterns on a pair of supplied blank PROMS. The EPROM may be addressed at the same memory location as the CMOS RAM, allowing shadowing techniques to be used. Shadowing allows the user to utilize the EPROMs for initial program start without committing valuable memory space.

The BP-0220 operates as a slave to the processor, but contains its own power source for the CMOS RAM in case of power failure. The power source is provided by three NiCd batteries mounted on the board, which provide a minimum of seven days of battery back-up at full charge. The on-board batteries can be disconnected and power fail sense circuits disabled for battery changing or storage.

The BP-0220 has an on-board status port which the CPU may read for the condition of Memory Inhibit, Battery Voltage Level, Power Fail Sense, and Power Fail Memory Inhibit. The CPU may also write into a status port to control Memory Inhibit of the RAM/EPROM or reset the power fail sense latch. Test points are provided at the edge of the BP-0220 to allow easy monitoring of battery voltage levels.

The BP-0220 16K CMOS RAM/EPROM board provides the maximum in systems memory flexibility and capability by providing both RAM and EPROM on one board. This configuration enables the user to have the highest degree of confidence in maintaining critical data during power outages or shortages.



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TM: Multibus is a registered trademark of Intel Corp.

BP-0220

SPECIFICATIONS

Word Size
- 8 or 16 bit data bus Software controlled

Memory Capacity
- RAM – 16K Bytes (8K words)
- ROM – Using eight μPD2716 or μPD2316E 16K Bytes (8K words)
- ROM – Using eight μPD2732 or μPD2332 32K Bytes (16K words)

Memory Addressing
- 16 and 20 bit addressing capability

Address Selection
- Via 2 μPB403 Fusable Link PROMs (256 x 4) or 2 SN74S287

Memory Response Time
- RAM Response Time
  Read Access: 450 ns Max.
  Read Cycle: 600 ns Max.
- ROM Response Time:
  μPD2716
  Read Access: 700 ns Max.
  Read Cycle: 850 ns Max.
  μPD2316E
  Read Access: 700 ns Max.
  Read Cycle: 850 ns Max.
  μPD2732
  Read Access: 700 ns Max.
  Read Cycle: 850 ns Max.
  μPD2332
  Read Access: 700 ns Max.
  Read Cycle: 850 ns Max.

Note: The 150 ns difference between Read Access and Read Cycle times are due to bus timing requirements for command set up and hold times. Memory Access is defined from Address True to Data Valid. Memory Response is defined as Memory Read/Write to Data Valid.

Bus Compatibility
- Interface: Multibus compatible
- P_1: 86 pin, double-sided, 0.156 inch centers.
- P_2: 60 pin, double-sided, 0.100 inch centers.

Physical Characteristics
- Width: 12.00 in. (30.48 cm)
- Height: 6.75 in. (17.15 cm)
- Thickness: 0.50 in. (1.27 cm)
- Weight: 376.00 grams

Power Requirements (Operational)
- V_{CC} = +5V ± 5%
- I_{CC} = 1.0 A Typ, 1.3A Max.

Battery Power Requirements
- V_{BAT} = 3.6V (Nominal)
- I_{BAT} = 200 μA Max.

Battery Characteristics
- Type: AAA-size NiCd (3 pcs.)
- Capacity: 180 mA hours
- Voltage: 3.6V nominal

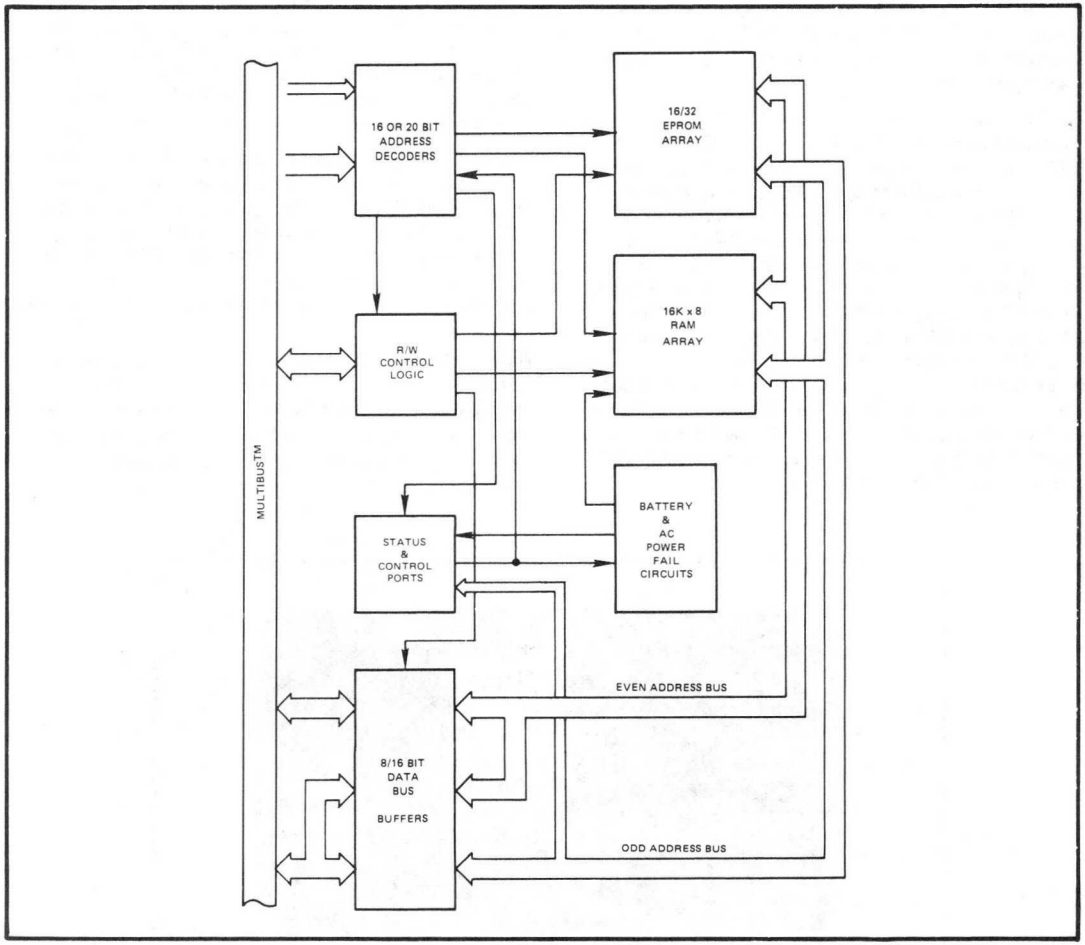
Battery Charge Time
- 14 hours for full charge (180 mA hours), full overcharge and short circuit protection.

Data Retention
- 168 hours following removal of +5V bus power.

Environmental Requirements
- Operating Temp.: 32° to 131°F (0° to 55°C)
- Relative Humidity: to 90% without condensation.

Applicable Literature
- BP-0220 User's Manual

BLOCK DIAGRAM



BP-0220-12-80-CAT

NEC Microcomputers, Inc.

BP-0575

Five-Channel Serial Communication Controller

STANDARD FEATURES

- Five Individually Configurable, Asynchronous Communication Channels
- Full Multibus™ Compatibility
- RS232C or Optically Isolated 20 mA Current Loop Capability
- Jumper-Selectable Baud Rate
- Jumper-Selectable I/O Address
- EIA Modem Control Support
- Field-Proven NEC μPD8251A USARTs

INTRODUCTION

The BP-0575, another member of the NEC Microcomputer family of Multibus™-compatible board products, is a versatile 5-channel asynchronous serial communications controller with both EIA RS232 and optically isolated current loop interface capabilities. The board is designed to be plugged into any standard Multibus™ backplane and to operate with 8 or 16-bit microprocessors.

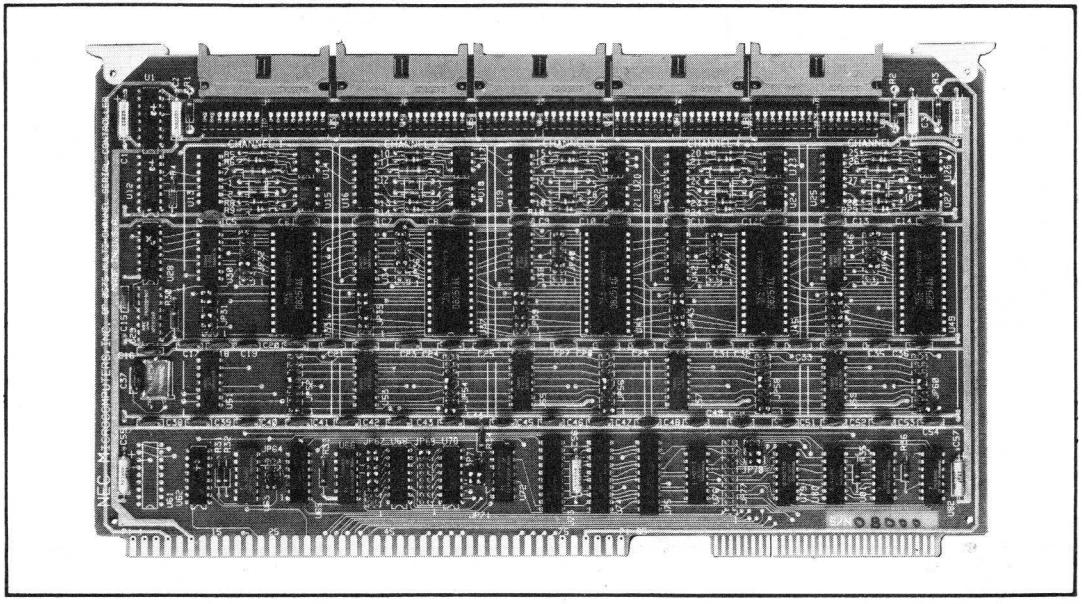
The board accepts data from the host processor in parallel data format and transmits serially to terminals, modems, or printers. The BP-0575 accepts serial data over its duplex channels and transfers it to the host processor in parallel format. Also processor-to-processor, bi-directional, serial communication can be implemented between systems equipped with BP-0575's.

The major functional element in the BP-0575 is the NEC μPD8251A Programmable Communications Interface Chip. NEC manufactures and is the leading world-wide supplier of this industry standard component. One NEC μPD8251A per channel and associated circuitry provide support for the EIA standard modem control signals request to send (RTS), data terminal ready (DTR), clear to send (CTS), and data set ready (DSR). Each channel has jumper-selectable receive/transmit baud rates from 75-19,2000 on the EIA interface and up to 2400 baud on the current loop interface.

A jumper-selectable on-board interrupt scheme gives the user the option of logically ORing together any or all transmit and receive interrupt lines for the five ports to decrease the number of bus interrupts used by the BP-0575.

The BP-0575 can be addressed in any 16-byte block beginning on any 16-byte boundary within the 256 byte I/O page. The board may be accessed through 12 jumper-selectable I/O ports within the 16-byte I/O block, and the user may address the five serial I/O channels and the two interrupt status registers in any order or priority within the addressed block.

This unique combination of features and flexibility makes the BP-0575 the logical choice in a wide range of Multibus™ applications.



TM: Multibus is a registered trademark of the Intel Corp.

BP-0575

SPECIFICATIONS

Bus Compatibility

- Interface: TTL-compatible.
- P1:86 pin, double-sided, 0.156 inch centers.
- P2: Not Used

Physical Characteristics

- Width: 12.00 in. (30.48 cm)
- Height: 6.75 in. (17.15 cm)
- Thickness: 0.50 in. (1.27 cm)
- Weight: 398.00 grams

Power Requirements (Operational)

- V_{CC} = +5V ± 5%
- I_{CC} = 0.9A Typ, 1.2A Max.

Voltage

- V_{CC} = +5V
- V_{DD} = +12V
- V_{AA} = -12V
- I_T = 1.9A Max.

Environmental Requirements

- Operating Temp.: 0° to 55°C
- Relative Humidity: to 90% without condensation.

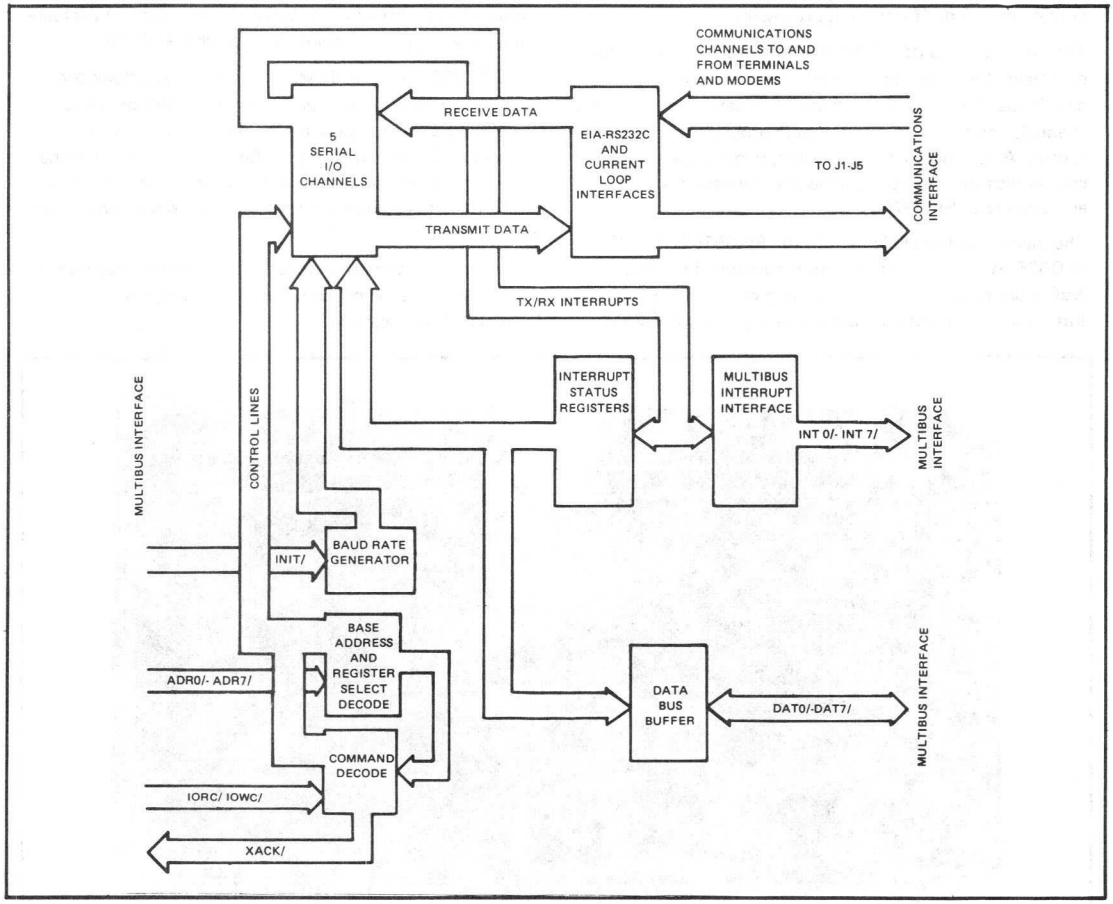
Interfaces — RS232C

- EIA standard RS232C signals provided and supported
  - Carrier Detect
  - Clear to Send
  - Data Set Ready
  - Data Terminal Ready
  - Request to Send
  - Receive Data
  - Transmit Data

Applicable Literature

- BP-0575 User's Manual

BLOCK DIAGRAM



NEC Microcomputers, Inc. BP-2190

Floppy Disk Controller/RAM

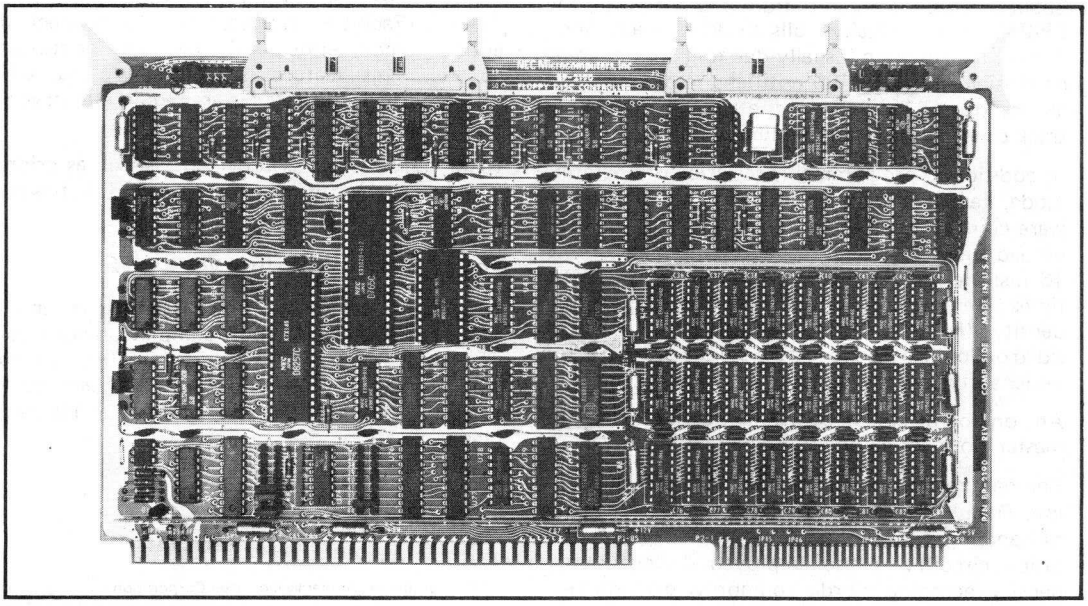
STANDARD FEATURES

The BP-2190 is a complete floppy disk controller with on-board RAM and the following features:

- Occupies a single card slot
- Handles up to four double-sided standard 8" or three mini 5¼" floppy disk drives
- Drives may be a mixture of single- or double-density types (software programmable)
- IBM compatible soft-sector recording format in both single- and double-density modes
- Performs fifteen different READ, SCAN, WRITE, FORMAT, SEEK, SENSE and SPECIFY commands with minimal processor overhead
- 48K x 8 of on-board, automatically refreshed dynamic RAM
- Dual-ported memory allows direct DMA data transfers to/from disk without processor intervention
- On-board priority logic arbitrates simultaneous memory accesses by disk, system bus or refresh logic

DESCRIPTION

The NEC Microcomputers BP-2190 Floppy Disk Controller/RAM is a dual-purpose board. It combines a floppy disk controller (FDC) capable of controlling up to four 8" standard or three 5¼" mini-floppy disk drives with up to 48 kilobytes of dual-ported RAM. Dual-porting makes the RAM available both to the disk for DMA data transfers and to the host processor for data storage and program execution. The BP-2190 can be paired with any compatible single-board computer to make a very powerful two-board, floppy disk based computer system.



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BP-2190

With on-board RAM and all necessary Direct Memory Access Control (DMAC) logic, the BP-2190 is a complete interface between the drives and any Multibus™ single-board computer system. It provides a powerful facility for the control of disk data transfers, and many of its features have been included specifically to minimize processor overhead. All disk data transfers are under control of the FDC (μPD765) and DMAC (μPD8257) and are independent of the processor. Once a disk transfer has been requested by the processor, the FDC and DMAC work together to obtain the proper data and transfer it to/from the on-board memory through one of its dual ports. When the transfer is complete, the FDC notifies the processor by generating an interrupt.

A single READ or WRITE command allows the transfer of a single sector, multiple sectors, an entire track or even an entire cylinder's worth of data (one track on both sides of the diskette). READ and WRITE operations may be performed on normal and/or deleted data fields.

Execution of a FORMAT A TRACK command allows an entire track to be formatted in one diskette revolution. The FDC supplies all information for formatting in either single- or double-density, except for 4 bytes in each ID field. The DMA controller fetches these 4 bytes/sector, thus allowing the user to have non-sequential numbered sectors. SEEK and RECALIBRATE operations can occur on up to four drives simultaneously.

Between FDC commands from the processor, the BP-2190 automatically polls all drive Ready lines; if one changes state (usually due to a door opening or closing), the BP-2190 notifies the processor via an interrupt. This allows the processor to keep track of which drives are on-line or off-line.

In addition to programmable selection of operating mode, key time intervals are selectable under software control. Head load time (2 to 254 ms), head unload time (16 to 240 ms) and stepping rate (1 to 16 ms) are programmable. For mini-floppies these times are automatically doubled. Either single-density (FM) or double-density (MFM), single-sided or double-sided reading/writing can be selected under software control.

An on-board crystal-controlled oscillator is the master clock for all board timing requirements.

The data recovery circuit, which separates raw data into Data Window and RD Data signals, is capable of handling wide peak shift variations. Precompensation circuitry is also employed during double-density recording in order to improve performance.

OPTIONS

The BP-2190's powerful jumper option structure accommodates most floppy disk drives on the market. Along with the standard features, the BP-2190's on-board jumpers allow selection of:

- Standard or Mini-Floppy Drives
- Internal or External Clock
- Generate/Receive/Ignore Bus Clock
- Memory Bank Base Addresses
- FDC I/O Port Base Address
- Memory Protect/Disable
- Interrupt Line (1 of 9)
- Reset at Power-Up, by Software Command or External Switch Closure
- XACK/ and/or AACK/ Acknowledgements

In addition, four radial HEAD LOAD signals are provided, as are four general-purpose software controlled output lines useful for controlling mini-floppy motors, Drive-In-Use lights, door locks, etc.

ON-BOARD MEMORY

The on-board memory is implemented with NEC μPD416 dynamic RAMs. Its dual-port architecture allows either disk data transfers to take place under DMA control, or for the host processor to have access to the memory. All disk data transfers occur between the drive and the on-board RAM.

Each of the three memory banks of 16K are base address selectable at 0000H, 4000H, 8000H or C000H. Facilities are provided to deselect the entire memory either under hardware or software control. This feature is especially useful when system initialization ROMs are required to have the same base address as used by RAM.

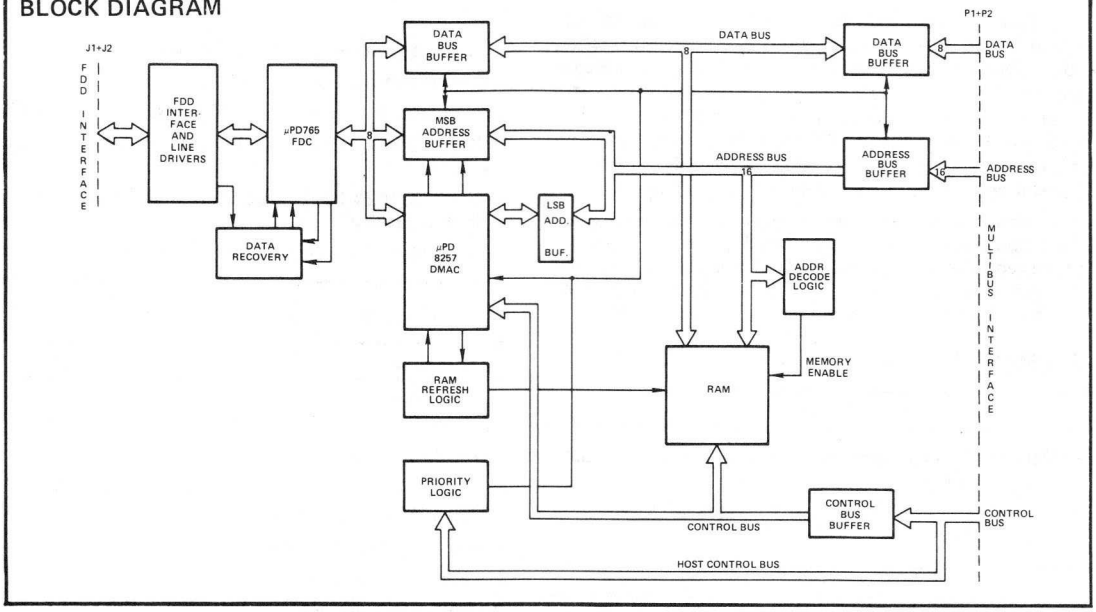
RAM refresh logic is provided, as well as priority circuits which arbitrate simultaneous disk, bus and/or refresh memory access requests.

SOFTWARE DISK DRIVERS

A complete set of I/O Driver routines is supplied with the BP-2190 board. A complete, heavily commented source listing is provided in 8080 assembly language so that the user can easily understand and modify, if necessary, the software to fit his particular application.

TM: Multibus is a trademark of Intel Corporation

BLOCK DIAGRAM



Included in the software routines are READ, WRITE, FORMAT, SEEK, RECALIBRATE and DRIVE STATUS commands. These commands allow multiple sector READs and WRITEs to occur under DMA control. Drive-related parameters such as head load time, head unload time, stepping rate, drive number, etc., are set up or controlled via a convenient I/O parameter block.

These software driver programs allow a first-time user of floppy disk systems to get his BP-2190 board "on the air" in minimum time. The serious OEM may wish to modify or to totally revamp the supplied software, and the accompanying documentation makes this task easy to do.

PROGRAMMING

Eight I/O Ports (relocatable via jumpers) are required to program the BP-2190. While most of the instructions are very simple single-byte transfers, the DMA controller (μPD8257) and the FDC Controller (μPD765) require multi-byte transfers from the processor. These bytes may be supplied in an asynchronous manner. However, once the request for the disk transfer has been made, the operations of loading the head, finding the proper sector and transferring it to the on-board RAM occur automatically with no processor intervention. After the disk transfer has been completed, an interrupt is generated and the processor must read out the results of the disk transfer. This read-out is typically a multi-byte transfer.

OPERATION

Most floppy disk controller operations are performed in three stages: the Command Phase, the Execution Phase and the Result Phase. Each command is initiated by a multi-byte transfer from the processor, after which the BP-2190 executes the command in true asynchronous fashion. It signals completion of the command via an interrupt to the processor, which then reads the information presented in the FDC's Result Status registers.

As an example, the reading of a sector on one of four drives into a specific block of on-board RAM would involve the following:

PHASE	PROCESSOR READ/WRITE	FUNCTION OF INSTRUCTION(S)
Command	W	Specify memory starting address and block length to DMA.
	W	Specify a Sector Read, select drive
	W	Specify (current) track, head, sector number and bytes/sector
	W	Declare track's final sector number and gap length
Execution	—	Head is loaded, specified sector is located, data is recovered, reassembled and written into specified memory block — all with no further intervention by processor. Completion is signaled by an interrupt.
Result	R	Read status registers to determine success of execution phase, source of error if execution failed.
	R	Read post-execution track, head and sector numbers.

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BP-2190

FDC STATUS REGISTERS

The FDC on the BP-2190 contains five status registers which supply the processor with extensive information about disk transfers. One of these, the Main Status Register, may be read by the processor at any time. It indicates whether any of the FDDs are in Seek Mode (FDD0, 1, 2 or 3 Busy), whether the FDC has a Read/Write operation in process (FDC Busy), and whether the FDC is ready to transfer commands from or results to the processor.

The other four status registers are only available after an FDC operation has been completed. Three of these are presented after each Read or Write operation and supply detailed information on how the data transfer progressed. The fourth indicates the condition of the FDD itself.

COMMAND SUMMARY

Memory

- Memory Read (processor reads a single byte of data from memory)
- Memory Write (processor writes a single byte of data into memory)

Disk

- Read Data
- Read Deleted Data
- Read Track
- Read ID
- Seek
- Recalibrate
- Write Data
- Write Deleted Data
- Format Track
- Scan Equal
- Scan High or Equal
- Scan Low or Equal
- Sense Interrupt Status
- Sense Drive Status
- Specify (Head Load and Unload Times, Step Rates)
- Set/Reset Auxiliary Outputs (e.g., Motor On/Off)

I/O

- DMA Data Channel
- DMA RAM Refresh Channel
- DMA Mode
- External Control
- FDC Status
- FDC Data

MULTIBUS™ COMPATIBILITY

The BP-2190 is fully compatible with all mechanical and electrical requirements of Intel iSBC™ and National BLC Multibus™ systems. It will also operate as a low-order 8-bit slave on the expanded Multibus™ (such as required by the 16-bit Intel iSBC™ 86/12). The BP-2190 conforms to all Multibus™ voltage level, current level and timing requirements, and is ready to plug in and run as supplied.

TM: iSBC is a trademark of Intel Corporation

SPECIFICATIONS

Media

- Flexible diskette, 8" standard or 5¼" mini
- One or two surfaces per diskette
- 77 tracks per surface (8"), 35 tracks per surface (5¼")
- 128/256/512/1024/2048/4096 bytes per sector single-density
- 256/512/1024/2048/4096/8192 bytes per sector double-density

Transfer Rate: Rates are in kilobits per second

DENSITY	DIAMETER	
	5¼	8
Single	125	250
Double	250	500

Physical Characteristics

- Mounting — occupies one chassis or card cage slot
- Height — 6.75 in (171.5 mm)
- Width — 12.00 (304.8 mm)
- Depth — 0.5 in (12.7 mm)

DC Power Requirements

- +12V ± 5%; 150 mA
- +5V ± 5%; 1.3 Amps
- -5V ± 5%; 6 mA

Environment

- Operating: 0°C to 50°C
- Non-operating: -55°C to +85°C
- Humidity — up to 90% RH, non-condensing

Documentation Supplied

- UM-2190 Users' Manual

DRIVES

The BP-2190 directly interfaces with the following drives. Other types may require modification or additional interface circuitry and/or software.

MANU-FACTURER	8" FLOPPY DRIVES	5.25" MINI-FLOPPY DRIVES
BASF	–	6106,6108
Caldisk	143M	–
Memorex	550/552	–
MFE	500/700 Series	–
Micropolis	–	1015-1,2,4;1016-2,4;
Persci	70,270,288	–
Pertec	FD5x4,FD650	FD200,FD250
Qume	Datatrak-8	
Siemens	FDD 200-8,100-8	FD200-5, FD100-5
Shugart Assoc.	SA800,850	SA400,SA450

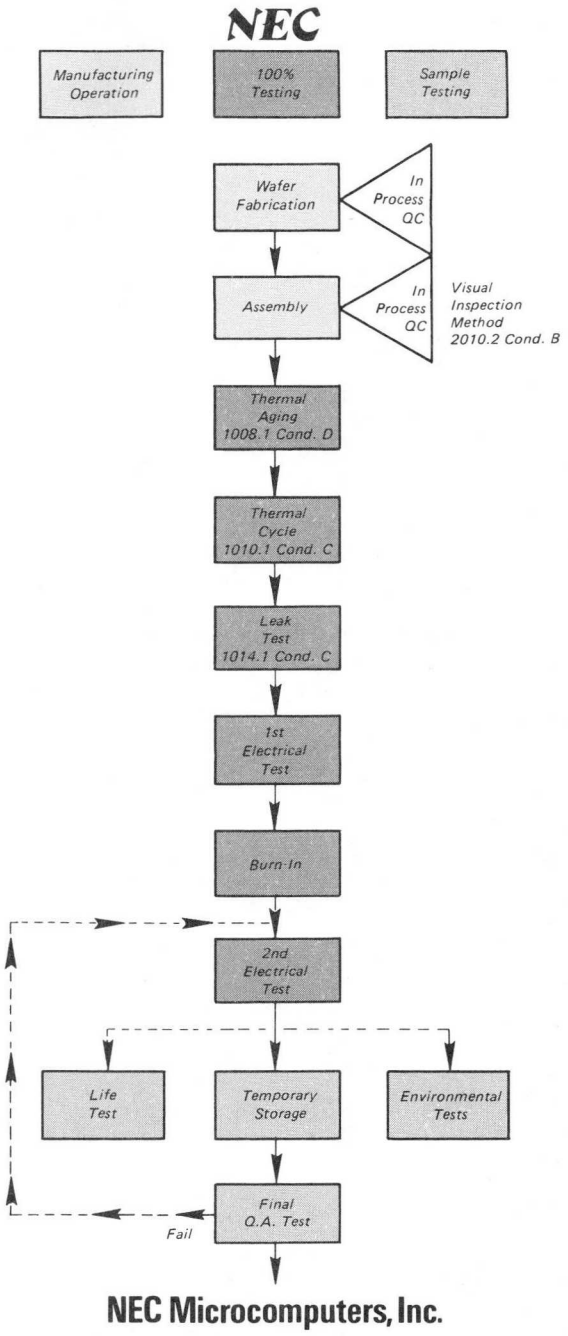
NEC Quality Assurance Procedures

One of the important factors contributing to the final quality of our memory and microcomputer components is the attention given to the parts during the manufacturing process. All Production Operations in NEC follow the procedures of MIL Standard 883A. Of particular importance to the reliability program are three areas that demonstrate NEC's commitment to the production of components of the highest quality.

I. Burn-In – All memory and microcomputer products are dynamically burned in at an ambient temperature sufficient to bring the junction to a temperature of 150°C. The duration of the burn-in is periodically adjusted to reflect the production history and experience of NEC with each product. 100% of all NEC memory and microcomputer products receive an operational burn-in stress.

II. Electrical Test – Memory and microcomputer testing at NEC is not considered a statistical game where the device is subjected to a series of pseudo random address and data patterns. Not only is this unnecessarily time consuming, but it does not effectively eliminate weak or defective parts. NEC's test procedures are based on the internal physical and electrical organization of each device and are designed to provide the maximum electrical margin for solid board operation. For further information on NEC's testing procedures see your local NEC representative.

III. After completion of all 100% test operations, production lots are held in storage until completion of two groups of extended sample testing: an operating life test and a series of environmental tests. Upon successful completion of these tests, the parts are released from storage and sent to final Q.A. testing.



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